Application Note

Power Sub-System Design Using PV88080

AN-PV-001

Abstract

This application note illustrates PMIC power supply design using the PV88080.

Contents

1 Terms and Definitions

CPU	Central Processing Unit
DDR	Dual Data Rate Memory
DVC	Dynamic Voltage Control
FET	Field Effect Transistor
NMOS	N-Type Metal Oxide Semiconductor
PMIC	Power Management Integrated Circuit
PMOS	P-Type Metal Oxide Semiconductor
QFN	Quad Flat (Package) – no leads
RMS	Root Mean Squared
VDS	Voltage Drain to Source

2 Introduction

The PV88080 power management integrated circuit (PMIC) provides one PWM buck controller and three adjustable synchronous buck regulators. The high voltage buck controller can optionally be used to generate the supply for the other three buck converters. Two pass devices (NMOS FET) for the high side and low side of the high voltage buck controller are external which allows the majority of the buck controller power dissipation to be outside the PV88080. This high voltage buck controller uses a constant on-time control scheme with integrated bootstrap PMOS switch. In certain applications, multiple PV88080s can be used together to provide enough power rails to power the larger systems. There are three buck converters that can be used to generate the supplies for CPUs, DDR memory, and other auxiliary functions in a typical application. The pass devices of these buck converters are fully integrated, so no external FETs or Schottky diodes are needed. This results in optimized power efficiency and a reduced external component count. PV88080 provides dynamic voltage control (DVC) via I^2C command to support adaptive adjustment of the supply voltage based on the processor. All power blocks have over-current circuit protection and the start-up timing can be controlled through the I^2C interface. Soft start-up limits the inrush current from the input node and secures a slope controlled activation of the rail. The PV88080 is available in a 32-pin QFN package and is specified from –40 °C to 85 °C ambient temperature.

3 Design Example

PV88080 provides one PWM buck controller (HVBuck) and three adjustable synchronous buck regulators (Buck1, Buck2, Buck3). This example describes the design process for the following:

- HVBuck regulating a 5 V output at a load current of 20 A
- Buck1 regulating a 1 V output at a load current of 5 A
- Buck2 regulating a 1.5 V output at a load current of 2 A
- Buck3 regulating a 3.3 V output at a load current of 2 A

Table 1: PV88080 Design Example Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HVBuck						
Supply voltage	V_{DD}		4.75		5.25	V
Input voltage	V_{IN}			12		V
Output voltage	V_{OUT}	DC V_{OUT} for the first PV88080 FB = V_{OUT}*(1/5)		5		V
Output voltage accuracy	V_{OUT_ACC}	V_{IN} = 12 V V_{OUT} = FB = 1 V T_A = 25 °C	-1		1	%
Output ripple	V_{OUT_PP}	I_{OUT} = 25 %*I_{MAX}/I_{MAX} V_{IN} = 12 V +/-10 % V_{OUT} = 1 V L=1.5 µH C = 470 µF t_{RISE} = t_{FALL} = 25 µs			50	mV
Output current	I_{OUT}				5000	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching frequency	fsw	V_{IN} = 12 V V_{OUT} = FB = 1 V		500		kHz
Minimum off time	t_{OFF} (Min)			200		ns
Buck1						
Input voltage	V_{DD}		4.75		5.25	V
Output voltage	V_{BUCK1}			1		V
Output voltage accuracy	V_{BUCK1_ACC}		-3		3	%
Load regulation	V_{OUT_LD}	V_{DD} = 5 V V_{OUT} = 1.2 V, I_{OUT} = 0A~5 A PWM operation		1.67		%/A
Line regulation	V_{OUT_LINE}	V_{DD} = 4.75 V ~ 5.25 V V_{OUT}=1.2 V I_{OUT}= 0 A PWM operation		0.33		%/V
Output current	I_{OUT}				5000	mA
Switching frequency	fsw			1		MHz
Buck2						
Input voltage	V_{DD}		4.75		5.25	V
Output voltage	V_{BUCK2}			1.5		V
Output voltage accuracy	V_{BUCK2_ACC}		-3		3	%
Load regulation	V_{OUT_LD}	V_{DD} = 5 V V_{OUT} = 1.8 V I_{OUT} = 0 A~2 A PWM operation		1.11		%/A
Line regulation	V_{OUT_LINE}	V_{DD} = 4.75 V ~ 5.25 V V_{OUT}=1.8 V I_{OUT}= 0 A PWM operation		0.22		%/V
Output current	I_{OUT}				2000	mA
Switching frequency	fsw			1		MHz
Buck3						
Input voltage	V_{DD}		4.75		5.25	V
Output voltage	V_{BUCK3}			3.3		V
Output voltage accuracy	V_{BUCK3_ACC}		-3		3	%
Load regulation	V_{OUT_LD}	V_{DD} = 5 V V_{OUT} = 3.3 V I_{OUT} = 0 A~2 A PWM operation		1.21		%/A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line regulation	V_{OUT_LINE}	V_{DD} = 4.75 V ~ 5.25 V V_{OUT} = 3.3 V I_{OUT} = 0 A PWM operation		0.6		%/V
Output current	I_{OUT}				2000	mA
Switching frequency	fsw			1		MHz

3.1 Inductor Selection

For most applications, HVBuck power inductors are generally chosen to let peak-to-peak ripple current be 30 % to 40 % of the nominal current. Given a target ripple current of 40 %, the required inductor can be calculated using the following equation:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{5V \times (26V - 5V)}{26V \times 20A \times 0.4 \times 500kHz} = 1.01uH \quad (1)$$

Choose a 1.5 µH inductor for HVBuck converter.

For LVBuck converter, the same criteria for inductor selection, the required inductor can be calculated using the following equations:

Buck1:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{1V \times (5V - 1V)}{5V \times 5A \times 0.4 \times 1Mhz} = 0.4uH \quad (2)$$

Buck2:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{1.5V \times (5V - 1.5V)}{5V \times 2A \times 0.4 \times 1Mhz} = 1.31uH \quad (3)$$

Buck3:

$$L = \frac{V_{OUT} \times \left(V_{IN(\max)} - V_{OUT}\right)}{V_{IN(\max)} \times \Delta I_L \times f_{sw}} = \frac{3.3V \times (5.V - 3.3V)}{5V \times 2A \times 0.4 \times 1Mhz} = 1.4uH \quad (4)$$

Choose a 1.5 µH inductor for all LVBuck converters to optimize cost and performance.

3.2 Output Capacitor Selection

The criteria for the output capacitor selection is determined by the output load transient response current step size. Use the following equation to calculate the required output capacitance.

$$V_{out,step} = \frac{I_{STEP}}{C_{OUT}} \times \Delta T = \frac{I_{STEP}}{C_{OUT}} \times \frac{I_{STEP} \times L}{V_{OUT}} = \frac{{I_{STEP}}^2 \times L}{C_{OUT} \times V_{OUT}} \quad (5)$$

HVBuck:

$$150mV = \frac{15A^2 \times 1.5uH}{C_{OUT} \times 5V} \quad (6)$$

$$C_{OUT} = 450uF$$

For LVBucks, consider the stability of each buck converter. The minimum capacitor requirement should at least 60 µF, therefore two 2012, 47 µF, 10 V, X5R ceramic capacitors are used for LVBucks output capacitors.

3.3 Input Capacitor Selection

3.3.1 12 V Input Voltage and 600 mV Voltage Ripple

Using the typical 12 V input voltage and a 600 mV voltage ripple (5 % of the typical input voltage), the minimum input capacitor of HVBuck can be derived from the following equation.

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{20A \times 5V}{600mV \times 12V \times 500kHz} = 27.78uF \quad (7)$$

Also the RMS current flow into the input capacitor can be derived from the following equation.

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 9.86Arms \quad (8)$$

Choose four 3225, 10 µF, 35 V, X7R ceramic capacitors, 2.5 A RMS current rating per capacitor. Higher voltage rating for input capacitor could decrease the derating effect of the ceramic capacitor and ensure the sufficient capacitance during HVBuck operation. High-frequency decoupling capacitors should be placed as close to the MOSFET as possible.

3.3.2 250 mV Input Voltage Ripple

For the 250 mV input voltage ripple requirement (5% of the input voltage), the minimum input capacitor of LVBucks can be derived from the following equation.

Buck1:

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{5A \times 1V}{250mV \times 5V \times 1mHz} = 4uF \quad (9)$$

Buck2:

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{2A \times 1.5V}{250mV \times 5V \times 1mHz} = 2.4uF \quad (10)$$

Buck3:

$$C_{IN(\min)} = \frac{Iout \times Vout}{V_{in,ripple} \times V_{IN} \times f_{sw}} = \frac{2A \times 3.3V}{250mV \times 5V \times 1mHz} = 5.28uF \quad (11)$$

Also the RMS current flow into the input capacitor could be derived from the following equation.

Buck1:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 2Arms \quad (12)$$

Buck2:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 0.92Arms \quad (13)$$

Buck3:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left[I_{OUT}{}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right]} = I_{OUT} \times \sqrt{D \times (1-D)} = 0.95Arms \quad (14)$$

Choose one 2012, 10 µF, 35 V, X5R ceramic capacitors, 2.5 A RMS current rating per capacitor. Higher voltage rating for input capacitor could decrease the derating effect of the ceramic capacitor, ensure the sufficient capacitance during LVBucks operation.

3.4 MOSFET Selection

Since the HVBuck input voltage range is up to 26 V, output current is 20 A, and the VDS of MOSFET should be higher than the input voltage, choose at least the 40 V VDS, IDRIVER of the MOSFET should be at least 30 A.

MOSFET losses are the sum of its switching loss (P_{SW}) and conduction loss (P_{COND}). Detailed calculations are shown below:

High-Side MOSFET

$$P_{SW} = \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times f_{sw} \left(\frac{Q_G}{I_{DRIVER(L-H))}} + \frac{Q_G}{I_{DRIVER(H-L))}}\right) \quad (15)$$

$$P_{COND} = D \times {I_{OUT}}^2 \times R_{DS(ON)} \quad (16)$$

Low-Side MOSFET

$$P_{SW} = \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times f_{sw} \left(\frac{Q_G}{I_{DRIVER(L-H))}} + \frac{Q_G}{I_{DRIVER(H-L))}}\right) \quad (17)$$

$$P_{COND} = (1-D) \times {I_{OUT}}^2 \times R_{DS(ON)} \quad (18)$$

Where Q_G is the parameter of gate charge and is specified in the MOSFET datasheets. IDRIVER is the driving capability of the controller. The characteristic between $R_{DS(ON)}$ and Q_G is trade off. For applications with high input voltage and low output voltage (low duty cycle), the high-side MOSFET is mostly off so the switching loss will be dominant. In that case, the lower Q_G with higher $R_{DS(ON)}$ could be chosen. Also, since the conduction loss is dominated by the loss of the low-side MOSFET, the higher Q_G with lower $R_{DS(ON)}$ MOSFET could be chosen.

On the other hand, under the lower input voltage and higher output voltage (high duty cycle), the criteria for choosing high-side MOSFET is characterized by minimizing conduction loss. If the output voltage is close to half of the input voltage (duty cycle is close to 50 %), then both high- and low-side MOSFETs could choose the same part.

When selecting the $R_{DS(ON)}$ of the low-side MOSFET, the positive current limit threshold also needs to be considered.

$$P_{OS\_OC\_TH} = I_{OC} \times R_{DS(ON)} \quad (19)$$

POS_OC_TH could be set from 90 mV to 210 mV in the HVBUCK_CONF4 register.

Note
If the $R_{DS(ON)}$ of the MOSFET is too small, the positive over-current threshold might be too high to be triggered

4 Component Selection Summary

The components in this example are listed as below.

4.1 Capacitors

Ref	Value	Tol.	Size (mm)	Height (mm)	Temp. Char.	Rating (V)	Part Number
AVDD	1 x 10 µF	±10 %	2012	1.45	X7R	10	C2012X7R1A106K125AC
AVDD_HVBK	1 x 10 µF	±10 %	2012	1.45	X7R	10	C2012X7R1A106K125AC
LDO5V	1 x 4.7 µF	±10 %	2012	1	X7R	10	C2012X7R1A475K085AC
LDO2P5V	1 x 1 µF	±10 %	1608	0.9	X7R	6.3	GRM188R70J105KA01D
VIN_Supply	1 x 100 nF	±10 %	1608	0.9	X7R	50	GRM188R71H104KA93D
	1 x 10 µF	±10 %	2012	1.45	X5R	35	C2012X5R1V106K125AC
VBuck1, VBuck2, VBuck3,	1 x 100 nF	±10 %	1608	0.9	X7R	50	GRM188R71H104KA93D
	1 x 10 µF	±10 %	2012	1.45	X5R	35	C2012X5R1V106K125AC
	2 × 47 µF	±20 %	2012	1.45	X5R	10	GRM21BR61A476ME15
HVBuck	2 x 100 nF	±10 %	1608	0.9	X7R	50	GRM188R71H104KA93D
	1 x 100 nF	±10 %	1608	0.9	X7R	16	GRM188R71C104KA01D
	4 x 10 µF	±20 %	3225	2.8	X7R	35	GJ832ER7YA106KA12
	10 × 47 µF	±20 %	2012	1.45	X5R	10	GRM21BR61A476ME15

4.2 Inductors

Ref	Value	ISAT (A)	IRMS (A)	DCR (Typ) (mΩ)	Size (W×L×H) (mm)	Part Number
Buck1, Buck2, Buck3	1.5 µH	11.5	11	9.7	7.1×6.5×3	TDK SPM6530T -1R5M
		11.5	11	9.7	7.1×6.5×3	TDK SPM6530T -1R5M
		11.5	11	9.7	7.1×6.5×3	TDK SPM6530T -1R5M
HVBuck	1.5 µH	51	28	2.3	12.8x13.8x6.5	Cyntec CMLS136E-1R5MS

4.3 Resistors

Ref	Value	Tol.	Size (mm)	Height (mm)	Temp. Char.	Rating (W)	Part Number
HVBuck	0R	Jumper	1608	0.55	Jumper	0.1	RC0603JR-070RL
	24.9K	±1 %	1608	0.55	±100 ppm/°C	0.1	RC0603FR-0724K9L
	100K	±1 %	1608	0.55	±100 ppm/°C	0.1	RC0603FR-07100K9L

4.4 MOSFET

Ref	RDSON at VGS = 4.5 V (mΩ)	Size (W×L×H) (mm)	VDS Rating (V)	Part Number
HVBuck	3.6	5.3x6.15x1	40	AON6232
	3.0			SiR644DP

5 Conclusions

With its unique features and flexibility, the PV88080 supports many different applications with varying voltage and current requirements. Using the guidelines discussed in this application note the designer can select the appropriate discrete components easily to implement a robust PMIC design using the PV88080.

Revision History

Revision	Date	Description
1.0	23-Jul-2017	Initial version.

Disclaimer

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including without limitation the specification and the design of the related semiconductor products, software and applications.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Customer notes that nothing in this document may be construed as a license for customer to use the Dialog Semiconductor products, software and applications referred to in this document. Such license must be separately sought by customer with Dialog Semiconductor.

All use of Dialog Semiconductor products, software and applications referred to in this document are subject to Dialog Semiconductor's Standard Terms and Conditions of Sale, available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

Dialog and the Dialog logo are trademarks of Dialog Semiconductor plc or its subsidiaries. All other product or service names are the property of their respective owners.

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Singapore
Dialog Semiconductor Singapore
Phone: +65 64 8499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 3769 5200

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.