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April 1st, 2010
Renesas Electronics Corporation

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H8SX Family
Pulse Output (8-bit Timer)

Introduction
As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

Target Device
H8SX/1638, H8SX/1648, H8SX/1650, H8SX/1658R, H8SX/1668R Groups

Preface
Although the writing of this application note is in accord with the hardware manual for the H8SX/1650 Group, the program covered in this application note can be run on the target devices indicated above. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device.

Contents
1. Overview .......................................................................................................................... 2
2. Configuration .................................................................................................................. 3
3. Sample Program .......................................................................................................... 5
1. Overview

The TMR (8-bit timer) of the H8SX series is used to output a desired number of pulses at a 50% duty cycle. When the H8SX series operates at 25 MHz (Figure 1), you can set any pulse cycle between 0.96 and 81.92 µs in units of 0.32 µs. You can also set any number between 1 and 256 as the number of pulses to be output.

![Figure 1 Pulse Output Timing](image-url)
2. Configuration

Figure 2 is a block diagram of the 8-bit timer used in this sample task.

![Block Diagram of Output Pulse Count](image-url)

**Figure 2  Block Diagram of Output Pulse Count**
Table 1 lists the function allocation of this sample task. As listed in Table 1, the H8SX series functions are allocated and the pulse is output.

### Table 1 Function Allocation for H8SX Series

<table>
<thead>
<tr>
<th>H8SX series function</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCNT_0</td>
<td>For generating compare matches A and B</td>
</tr>
<tr>
<td>TCORA_0</td>
<td>For generating compare match A</td>
</tr>
<tr>
<td>TCORB_0</td>
<td>For generating compare match B</td>
</tr>
<tr>
<td>TCSR_0</td>
<td>Outputs 1 for each compare match A or 0 for each compare match B.</td>
</tr>
<tr>
<td>TMO0</td>
<td>Timer output pin (compare match output)</td>
</tr>
<tr>
<td>TCR_0</td>
<td>Clears the counter when compare match A occurs and selects the input clock ($\phi/8$).</td>
</tr>
<tr>
<td>TCNT_1</td>
<td>Counts the number of occurrences of compare match A in unit 0.</td>
</tr>
<tr>
<td>TCORA_1</td>
<td>For generating compare match A</td>
</tr>
<tr>
<td>TCR_1</td>
<td>Clears the counter when compare match A occurs and enables compare match (A) interrupts.</td>
</tr>
</tbody>
</table>

Figure 3  Description of Operation of Pulse Output
3. Sample Program

3.1 Function

This sample program counts the number of compare matches in channel 0 with the timer in channel 1 in the 8-bit timer with these two channels cascaded. This program generates an interrupt when the specified number of compare matches occurs and terminates pulse output processing.

This sample program generates seven pulses and then stops output.

3.2 Function Specifications

```c
void pulse(unsigned char pulse_cycle,unsigned char pulse_count )
```

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pulse_cycle</td>
<td>Sets the pulse cycle.</td>
</tr>
<tr>
<td>pulse_count</td>
<td>Sets the pulse count.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Return value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>—</td>
</tr>
</tbody>
</table>

Example)

```c
eextern void pulse( unsigned char, unsigned char );
void main( void )     // Main routine
{
    unsigned char cycle;
    unsigned char count;
    cycle = 255;
    count = 7;
    pulse(cycle, count);   // Outputs pulses.
    while(1) ;
}
```
3.3 Flowchart

- **Start**
  - Cancel 8-bit timer module stop mode
  - Set timer counter TCORA in channel 0, as follows:
    - Channel 0: pulse_cycle
  - Set timer counter TCORB in channel 0, as follows:
    - Channel 0: pulse_cycle/2
  - Set timer counter TCORA in channel 1, as follows:
    - Channel 1: pulse_count
  - Set clock in channel 0, as follows:
    - ICKS1,0=B'00
  - Set timer counter output select for channel 0, as follows:
    - Channel 0: Outputs 1 for each CMFA
    - Channel 0: Outputs 0 for each CMFB
  - Set output in channel 1, as follows:
    - No TMO1 output
  - For channel 0
    - Interrupt request of timer counter enables CMFA interrupt
    - Timer counter clock select
      - Internal clock φ/8
  - For channel 1
    - Interrupt request of timer counter enables CMFA interrupt
    - Timer counter clear factor for channel 1
      - Cleared by CMFA
    - Timer counter clock select for channel 1
      - Count with TCNT_0 CMFA
  - Reset channel 0 and channel 1 counters
  - Clear I flag and enable interrupts
  - **End**

- **Start**
  - Clear status flag (CMFA) of channel 1 and enable next interrupt
  - Disable pulse output of channel 0
  - **End**
3.4 Program Listing

/** Include File */
#include <machine.h>
#include "iodefine.h"

/** Function Prototype */
void pulse(unsigned char pulse_cycle,unsigned char pulse_count);

/** Function Definition(Main Program) */
void pulse(unsigned char pulse_cycle,unsigned char pulse_count)
{
    set_imask_ccr(1);
    P_MSTPCRA.WORD = 0xFEFF; // disable module stop mode
    P_TMR0.TCORA = pulse_cycle; // set pulse cycle time
    P_TMR0.TCORB = pulse_cycle/2; // set "low"pulse time
    P_TMR1.TCORA = pulse_count; // set pulse counter
    P_TMR0.TCCR.BYTE = 0x08; // Initialize TCCR2
    P_TMR0.TCSR.BYTE = 0x06; // initialize TCSR2
    P_TMR1.TCSR.BYTE = 0x10; // initialize TCSR3
    P_TMR1.TCR.BYTE = 0x4c; // initialize TCR3
    P_TMR0.TCNT = 0; // reset counter
    P_TMR1.TCNT = 0; // reset counter
    set_imask_ccr(0);
}

/** Function Definition(Interrupt Handler) */
#pragma interrupt (inthdr_pulend (vect=119))
void inthdr_pulend(void) // Comperemcth interrupt Handler
{
    P_TMR1.TCSR.BIT.CMFA = 0; // Interrupt Clear
    P_TMR0.TCSR.BYTE = 0; // output disable
}
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Revision Record

<table>
<thead>
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<td>1.00</td>
<td>Sept.19.03</td>
<td>First edition issued</td>
<td>—</td>
<td>Page 1: Target devices added</td>
</tr>
<tr>
<td>2.00</td>
<td>Mar.07.08</td>
<td>Page 1: Target devices added Pages 1, and 3 to 7: Unit 1 changed to unit 0 (corrections made associated with this change)</td>
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