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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group
Protect Operation

1.0 Abstract
The following explains the protect operation.

2.0 Introduction
Operation

(1) Setting “1” in the write-enable bit of system clock control registers 0 and 1 causes system clock control register 0 and system clock control register 1 to be in write-enabled state.

(2) The contents of system clock control register 0 and that of system clock control register 1 are changed.

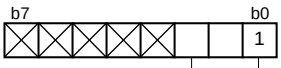
(3) Setting “0” in the write-enable bit of system control registers 0 and 1 causes system clock control register 0 and system control register 1 to be in write-inhibited state.

(4) To change the contents of processor mode register 0 and that of processor mode register 1, follow the same steps as in dealing with system clock control registers.

(5) The write-enable bit of port 9 direction register and SI/Oi control register (i=3,4) goes to “0” when the next write instruction is executed after write-enabled state is readied. Make changes in input/output and SI/Oi control register (i=3,4) immediately after the instruction that sets “1” in the write-enable bit of port P9 direction register and SI/Oi control register (i=3,4)(avoid causing an interrupt). Also take measures to prevent DMA transfer from being executed.

3.0 Set-up procedure

(1) Clearing the protect (set to write-enabled state)



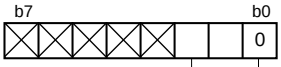
Protect register [Address 000A16]
PRCR

Enables writing to system clock control registers 0 and 1 (addresses 000616 and 000716)
1 : Write-enabled

Enables writing to port P9 direction register (address 03F316) and SI/Oi control register (i=3,4) (addresses 036216 and 036616)
0 : Write-inhibited
1 : Write-enabled

(2) Setting system clock control register i (i = 0, 1)

(3) Setting the protect (set to write-inhibited state)

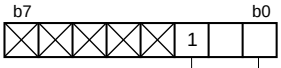


Protect register [Address 000A16]
PRCR

Enables writing to system clock control registers 0 and 1 (addresses 000616 and 000716)
0 : Write-inhibited

Enables writing to port P9 direction register (address 03F316) and SI/Oi control register (i=3,4) (addresses 036216 and 036616)
0 : Write-inhibited
1 : Write-enabled

(4) Clearing the protect (set to write-enabled state)



Protect register [Address 000A16]
PRCR

Enables writing to system clock control registers 0 and 1 (addresses 000616 and 000716)
0 : Write-inhibited
1 : Write-enabled

Enables writing to port P9 direction register (address 03F316) and SI/Oi control register (i=3,4) (addresses 036216 and 036616)
1 : Write-enabled

(5) Changes in port P9 or changes in SI/Oi control register (i=3,4)

4.0 Programming Code

```
;******************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0029_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Protect Operation
;   HISTORY   : 2003.05.16  Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;******************************************************************************
;******************************************************************************
;       Include
;******************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;******************************************************************************
;       Symbol definition
;******************************************************************************
ROM_TOP         .EQU    0F8000H     ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFDCH     ;Start address of fixed vector
;
M_PM0    .EQU    00000000B    ;Processor mode register 0
;                |||||++-----;Processor mode bit
;                ||||||        (00:Single-chip mode)
;                |||||+-------;R/W mode select bit
;                ||||+--------;Software reset bit
;                ||++---------;Multiplexed bus space select
;                ||            (00:Multiplexed bus is not used)
;                |+-----------;Port P40 to P43 function select bit
;                |             (Valid in microprocessor and memory expansion modes)
;                +------------;BCLK output disable bit
;                              (0:BCLK is output)
M_PM1    .EQU    00000000B    ;Processor mode register 1
;                |||||||+-----;Reserved bit (Must always be set to "0")
;                |||||++------;Nothing is assigned (write to these bits, write "0")
;                ||||+--------;Internal reserved area expansion bit
;                ||||          (0:The internal RAM area is 15K bytes or
;                ||||             less and the internal ROM area is 192K bytes or less)
;                |+++---------;Reserved bit (Must always be set to "0")
;                +------------;Wait bit
;                              (0:No wait state)
```

```
M_CM0    .EQU    00001010B    ;System clock control register 0
;                |||||++-----;Clock output function select bit (Valid only in single-chip mode)
;                |||||        (10:f8 output to P57/CLKout pin)
;                |||||+-------;WAIT peripheral function clock stop bit
;                |||||         (0:Do not stop peripheral function clock in wait mode)
;                ||||+--------;Xcin-Xcout drive capacity select bit (1:HIGH)
;                |||+---------;Port Xc select bit (0:I/O port)
;                ||+----------;Main clock (Xin-Xout) stop bit (0:On)
;                |+-----------;Main clock division select bit0
;                |             (0:CM16 and CM17 valid)
;                +------------;System clock select bit
;                              (0:Xin, Xout)
M_CM1    .EQU    01100000B    ;System clock control register 1
;                |||||||+-----;All clock stop control bit (Clock on)
;                |||++++------;Reserved bit (Must always be set to "0")
;                ||+----------;Xin-Xout drive capacity select bit
;                ||            (1:HIGH)
;                ++-----------;Main clock division select bit 1
;                              (01:Division by 2 mode)
;
;*****************************************************************************
;       Program area
;*****************************************************************************
;=============================================================================
;       Start up
;=============================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
;
;=============================================================================
;       Protect Operation
;=============================================================================
        MOV.B    #00000001B, prcr  ;Clearing the protect (set to write-enabled state)
;                          +---------;Enables writing to system clock control registers 0 and 1
        MOV.B    #M_CM0,     cm0   ;Main clock division selectting
        MOV.B    #M_CM1,     cm1   ;Main clock Division by 2 mode
        MOV.B    #00000000B, prcr  ;Setting the protect (set to write-inhibited state)
;                          +---------;write-inhibited (cm0,cm1)
        MOV.B    #00H,       p9    ;Clear port P9_0 to P9_7
        MOV.B    #00000100B, prcr  ;Clearing the protect (set to write-enabled state)
;                        +-----------;Enables writing to port P9 direction register and
;                                     SI/O control register
        MOV.B    #0FH,       pd9   ;Change in port P9 register (Set P9_0-P9_3 are output port)
;
MAIN:
        JMP      MAIN
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
```

```
;*******************************************************************************
;       Setting of fixed vector
;*******************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    dummy    ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

http://www.renesas.com/

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
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User's Manual

M16C/62A group Rev. 1.0
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