To our customers,

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# H8SX Family

## Producing a Specified Number of Pulses

### Introduction

The 8-bit timer (TMR) is used to produce a desired number (1 to 255) of pulses having a 50% duty cycle.

### Target Device

H8SX/1653F

### Contents

## 1. Specifications

- An example of the pulse output timing is shown in figure 1.
- The 8-bit timer (TMR) is used to produce a desired number (1 to 255) of pulses having a 50% duty cycle.
- At Pϕ = 16 MHz, the period of the pulse is settable within the range from 1.0 to 128 µs in 0.5-µs steps.
- The number of pulses can be specified within the range from 1 to 255.

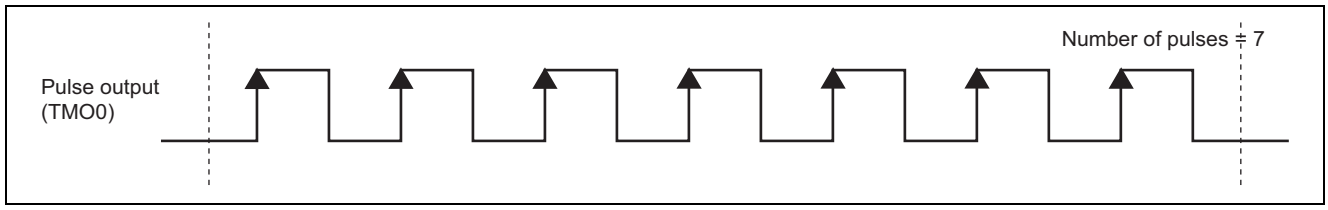



**Figure 1 Example of Pulse Output Timing**

## 2. Conditions for Application

**Table 1 Conditions for Application**

| Item | Contents | |
|---|---|---|
| Operating frequency | Input clock: | 16 MHz |
| | System clock (Iϕ): | 16 MHz |
| | Peripheral module clock (Pϕ): | 16 MHz |
| | External bus clock (Bϕ): | 16 MHz |
| Operating mode | Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)<br>MD_CLK = 0 | |
| Development tool | High-performance Embedded Workshop Version 4.00.02 | |
| C/C++ compiler | H8S, H8/300 Series C/C++ Compiler Version 6.01.00<br>(from Renesas Technology Corp.) | |
| Compile option | -cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3,<br>-speed = (register, shift, struct, expression) | |

**Table 2 Section Settings**

| Address | Section Name | Description |
|---|---|---|
| H'001000 | P | Program area |
| H'FF2000 | B | Non-initialized data area (RAM area) |

## 3. Description of Modules Used

Figure 2 shows a block diagram of the 8-bit timer. This sample task uses the following features of the 8-bit timer.

— The compare-match counter mode, in which two channels of the 8-bit timer are cascaded and the occurrences of compare match on channel 0 are counted by the channel 1 timer.
— Generation of an interrupt upon reaching a set count value.

This sample task uses these functions as shown in figure 2 and counts the rising edges of the pulses.

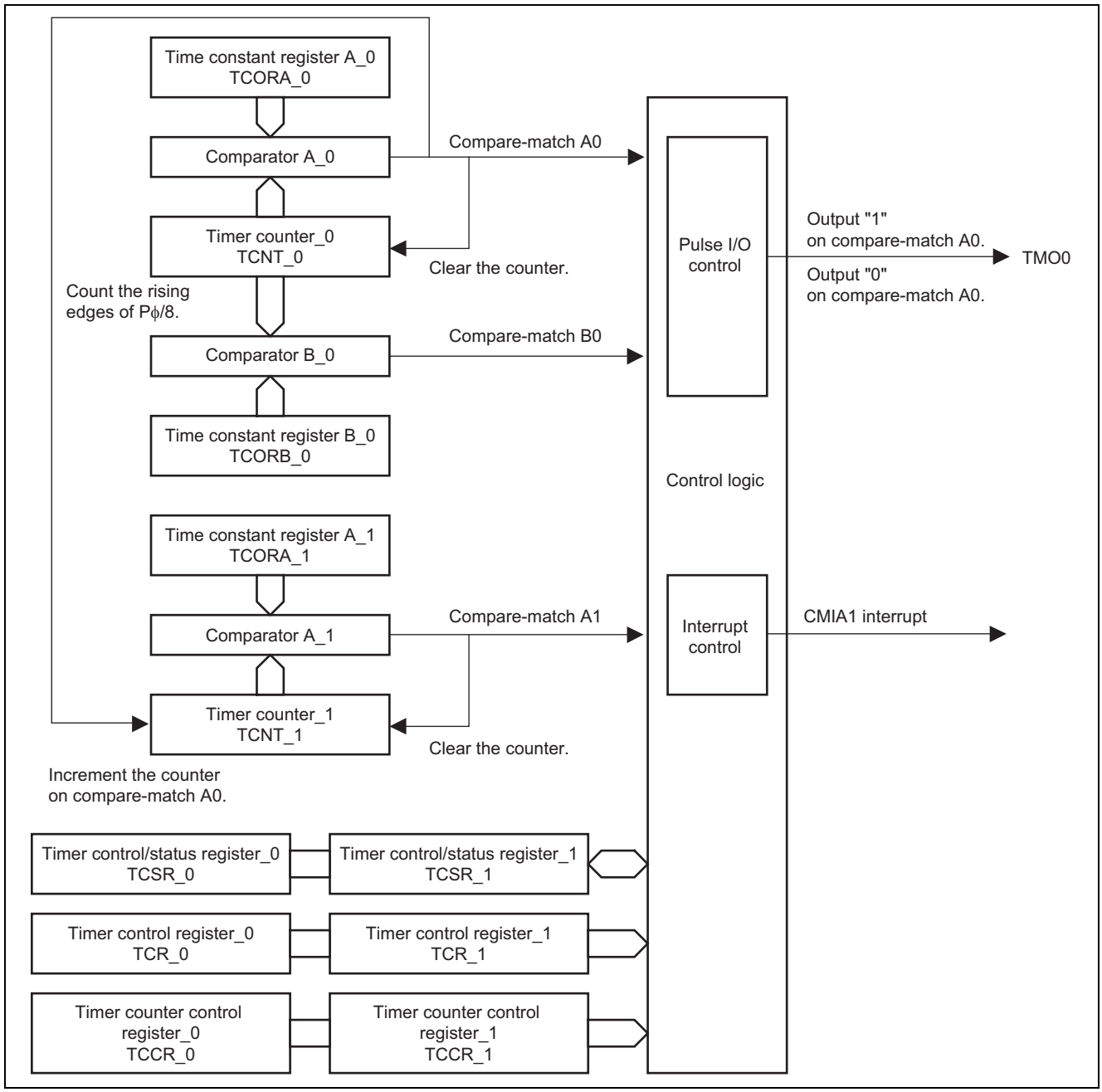



**Figure 2 Block Diagram of 8-Bit Timer**

## 4. Description of Operation

Figure 3 illustrates the principles of operation for the case when the value for the pulse period is set to H'09 and the number of pulses is set to H'07. The hardware processing and software processing of figure 3 are explained in table 3.

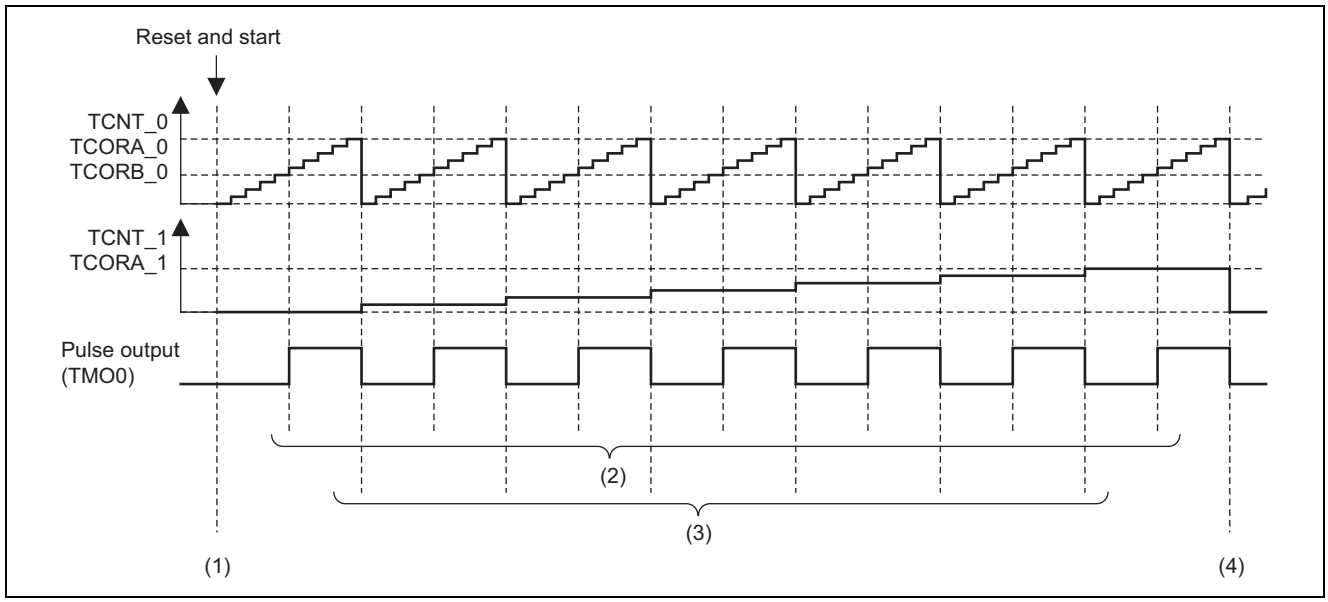



**Figure 3 Operation Principles of Pulse Train Output**

**Table 3 Hardware and Software Processing**

| | Hardware Processing | Software Processing |
|---|---|---|
| (1) | No processing | Initial settings<br>(a) Set the value for the pulse period in TCORA_0 and half the pulse period in TCORB_0.<br>(b) Configure TMR_0.<br>(c) Configure TMR_1.<br>(d) Clear TCNT_0 and TCNT_1.<br>(e) Enable the interrupt. |
| (2) | (a) Generate compare match B0 on TMR_0.<br>(b) Output a high level from the TMO0 pin. | No processing |
| (3) | (a) Generate compare match A0 on TMR_0.<br>(b) Clear TCNT_0.<br>(c) Output a low level from the TMO0 pin.<br>(d) Increment TCNT_1. | No processing |
| (4) | (a) Generate compare match A0 on TMR_0.<br>(b) Clear TCNT_0.<br>(c) Output a low level from the TMO0 pin.<br>(d) Clear TCNT_1.<br>(e) Generate a CMIA1 interrupt. | CMIA1 interrupt processing<br>(a) Disable the pulse output. |

# 5. Description of Software

## 5.1 List of Functions

**Table 4 List of Functions**

| Function Name | Functions |
|---|---|
| init | Initialization routine:<br>Cancels module stop mode, makes clock settings, and calls the main function. |
| main | Main routine:<br>Initializes the 8-bit timer. |
| cmia1_int | CMIA1 interrupt handling routine:<br>Interrupt handling routine for the TCORA_1 compare match interrupt that performs processing necessary to stop the pulse output. |

## 5.2 RAM Usage

**Table 5 RAM Usage**

| Label | Description | Size | Used In |
|---|---|---|---|
| flg | Flag indicating occurrence of the CMIA1 interrupt<br>0: CMIA1 interrupt has not occurred.<br>1: CMIA1 interrupt has occurred. | 1 byte | main, cmia1_int |

## 5.3 Constants

**Table 6 List of Constants**

| Label | Description | Used In |
|---|---|---|
| PULSE_CYCLE | Value for the pulse period<br>Setting value: H'09 | main |
| PULSE_COUNT | Number of pulses<br>Setting value: H'07 | main |

## 5.4 Description of Functions

### 5.4.1 init Function

(1) Functional Overview

Initialization routine that cancels module stop mode, makes clock settings, and calls the main function.

(2) Arguments

None

(3) Return value

None

(4) Internal Registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- System Clock Control Register (SCKCR) Address: H'FFFDC4

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 10 | ICK2 | 0 | R/W | System clock (Iϕ) select |
| 9 | ICK1 | 1 | R/W | These bits select the system clock frequency. The CPU, DMAC, and DTC modules are driven by the system clock. |
| 8 | ICK0 | 0 | R/W | 010: Input clock × 1 when MD_CLK = 0 |
| 6 | PCK2 | 0 | R/W | Peripheral clock (Pϕ) select |
| 5 | PCK1 | 1 | R/W | These bits select the frequency of the peripheral module clock. |
| 4 | PCK0 | 0 | R/W | 010: Input clock × 1 when MD_CLK = 0 |
| 2 | BCK2 | 0 | R/W | External bus clock (Bϕ) select |
| 1 | BCK1 | 1 | R/W | These bits select the frequency of the external bus clock. |
| 0 | BCK0 | 0 | R/W | 010: Input clock × 1 when MD_CLK = 0 |

- STPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module Stop Control Register A (MSTPCRA) Address: H'FFFDC8

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 15 | ACSE | 0 | R/W | All-module-clock-stop mode enable<br>Enables or disables transition to all-module-clock-stop mode.<br>If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current.<br>0: Disables transition to all-module-clock-stop mode.<br>1: Enables transition to all-module-clock-stop mode. |
| 13 | MSTPA13 | 1 | R/W | DMA controller (DMAC) |
| 12 | MSTPA12 | 1 | R/W | Data transfer controller (DTC) |
| 9 | MSTPA9 | 1 | R/W | 8-bit timer (TMR_3, TMR_2) |
| 8 | MSTPA8 | 0 | R/W | 8-bit timer (TMR_1, TMR_0) |
| 5 | MSTPA5 | 1 | R/W | D/A converter (channels 1, 0) |
| 3 | MSTPA3 | 1 | R/W | A/D converter (unit 0) |
| 0 | MSTPA0 | 1 | R/W | 16-bit timer pulse unit (TPU channels 5 to 0) |

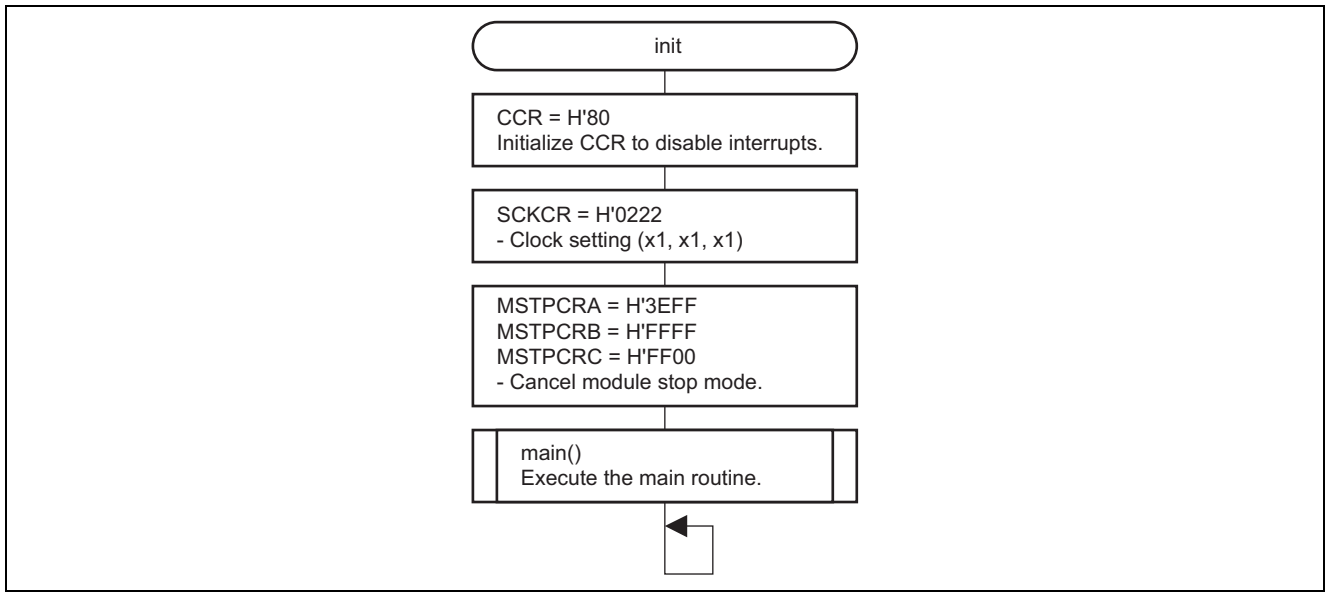
- Module Stop Control Register B (MSTPCRB) Address: H'FFFDCA

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 15 | MSTPB15 | 1 | R/W | Programmable pulse generator (PPG) |
| 12 | MSTPB12 | 1 | R/W | Serial communication interface_4 (SCI_4) |
| 10 | MSTPB10 | 1 | R/W | Serial communication interface_2 (SCI_2) |
| 9 | MSTPB9 | 1 | R/W | Serial communication interface_1 (SCI_1) |
| 8 | MSTPB8 | 1 | R/W | Serial communication interface_0 (SCI_0) |
| 7 | MSTPB7 | 1 | R/W | $I^2C$ bus interface_1 (IIC_1) |
| 6 | MSTPB6 | 1 | R/W | $I^2C$ bus interface_0 (IIC_0) |

- Module Stop Control Register C (MSTPCRC) Address: H'FFFDCC

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 15 | MSTPC15 | 1 | R/W | Serial communication interface_5 (SCI_5), (IrDA) |
| 14 | MSTPC14 | 1 | R/W | Serial communication interface_6 (SCI_6) |
| 13 | MSTPC13 | 1 | R/W | 8-bit timer (TMR_4, TMR_5) |
| 12 | MSTPC12 | 1 | R/W | 8-bit timer (TMR_6, TMR_7) |
| 11 | MSTPC11 | 1 | R/W | Universal serial bus interface (USB) |
| 10 | MSTPC10 | 1 | R/W | CRC unit |
| 4 | MSTPC4 | 0 | R/W | On-chip RAM_4 (H'FF2000 to H'FF3FFF) |
| 3 | MSTPC3 | 0 | R/W | On-chip RAM_3 (H'FF4000 to H'FF5FFF) |
| 2 | MSTPC2 | 0 | R/W | On-chip RAM_2 (H'FF6000 to H'FF7FFF) |
| 1 | MSTPC1 | 0 | R/W | On-chip RAM_1 (H'FF8000 to H'FF9FFF) |
| 0 | MSTPC0 | 0 | R/W | On-chip RAM_0 (H'FFA000 to H'FFBFFF) |

(5) Flowchart




### 5.4.2 main Function

(1) Functional Overview

Main routine that initializes the 8-bit timer.

(2) Arguments

None

(3) Return value

None

(4) Internal Registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in the sample task and differ from their initial values.

- Timer Control Register_0 (TCR_0) Address: H'FFFFB0

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 4 | CCLR1 | 0 | R/W | Counter clear 1, 0 |
| 3 | CCLR0 | 1 | R/W | 01: TCNT_0 is cleared upon compare match with TCORA_0. |
| 2 | CKSC2 | 0 | R/W | Clock select 2 to 0 |
| 1 | CKSC1 | 0 | R/W | See table 7. |
| 0 | CKSC0 | 1 | R/W | CKSC2 to CKSC0 = B'001 and ICKS1 and ICKS = B'00: TCNT counts rising edges of Pϕ/8. |

- Timer Control Register_1 (TCR_1) Address: H'FFFFB1

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | CMIEA | 1 | R/W | Compare match interrupt enable A<br>0: Disables interrupt request generation by CMFA_1 (CMIA_1).<br>1: Enables interrupt request generation by CMFA_1 (CMIA_1). |
| 4 | CCLR1 | 0 | R/W | Counter clear 1, 0 |
| 3 | CCLR0 | 1 | R/W | 01: TCNT_1 is cleared upon compare match with TCORA_1. |
| 2 | CKSC2 | 1 | R/W | Clock select 2 to 0 |
| 1 | CKSC1 | 0 | R/W | See table 7. |
| 0 | CKSC0 | 0 | R/W | CKSC2 to CKSC0 = B'100: TCNT_1 counts the occurrences of compare match A0. |

- Timer Control/Status Register_0 (TCSR_0) Address: H'FFFFB2

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | CMFA | 1 | R/W | Compare match flag A<br>0: TCNT_0 does not match the value in TCORA_0.<br>1: TCNT_0 matches the value in TCORA_0. |
| 3 | OS3 | 0 | R/W | Output select 3, 2 |
| 2 | OS2 | 1 | R/W | Selects the mode of output on the TMO_0 pin upon compare match B (i.e., TCNT_0 matches TCORB_0).<br>01: TMO_0 outputs 0. |
| 1 | OS1 | 1 | R/W | Output select 1, 0 |
| 0 | OS0 | 0 | R/W | Selects the mode of output on the TMO_0 pin upon compare match A (i.e., TCNT_0 matches TCORA_0).<br>10: TMO_0 outputs 1. |

- Timer Control/Status Register_1 (TCSR_1) Address: H'FFFFB3

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | CMFA | 0 | R/W | Compare match flag A<br>0: TCNT_1 does not match the value in TCORA_1.<br>1: TCNT_1 matches the value in TCORA_1. |

- Timer Constant Register A_0 (TCORA_0) Address: H'FFFFB4
  Function: 8-bit readable/writable register. The value in this register is always compared with TCNT_0, and if they match the CMFA flag in TCSR_0 is set.
  Setting: PULSE_CYCLE

- Timer Constant Register A_1 (TCORA_1) Address: H'FFFFB5
  Function: 8-bit readable/writable register. The value in this register is always compared with TCNT_1, and if they match the CMFA flag in TCSR_1 is set.
  Setting: PULSE_ COUNT

- Timer Constant Register B_0 (TCORB_0) Address: H'FFFFB6
  Function: 8-bit readable/writable register. The value in this register is always compared with TCNT_0, and if they match the CMFB flag in TCSR_0 is set.
  Setting: PULSE_CYCLE/2

- Timer Counter_0 (TCNT_0) Address: H'FFFFB8
  Function: 8-bit readable/writable register. In this sample task, TCNT_0 is cleared by the compare-match A signal of TMR_0.
  Setting: H'00

- Timer Counter_1 (TCNT_1) Address: H'FFFFB9
  Function: 8-bit readable/writable register. In this sample task, TCNT_0 is cleared by the compare-match A signal of TMR_1.
  Setting: H'00

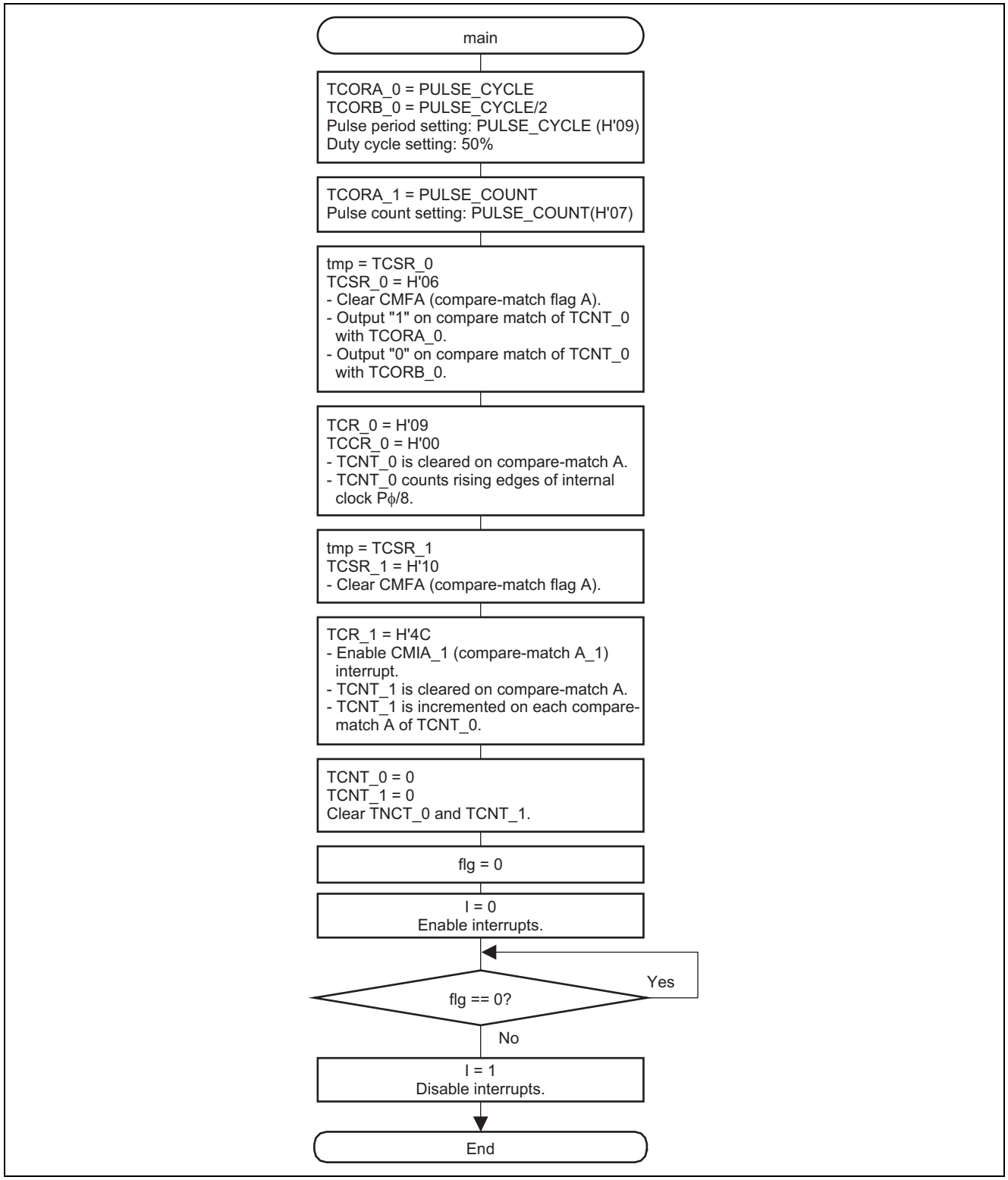
- Timer Counter Control Register_0 (TCCR_0) Address: H'FFFFBA

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 1 | ICKS1 | 0 | R/W | Internal clock select 1, 0 |
| 0 | ICKS0 | 0 | R/W | See table 7. |

**Table 7 Input Clock of TCNT and Conditions for Counting (Unit 0)**

| | TCR | | | TCCR | | |
|---|---|---|---|---|---|---|
| **Channel** | **CKS2** | **CKS1** | **CKS0** | **ICKS1** | **ICKS0** | **Description** |
| TMR_0 | 0 | 0 | 0 | — | — | Clock input is disabled. |
| | 0 | 0 | 1 | 0 | 0 | TCNT_0 counts rising edges of internal clock Pϕ/8. |
| | | | | 0 | 1 | TCNT_0 counts rising edges of internal clock Pϕ/2. |
| | | | | 1 | 0 | TCNT_0 counts falling edges of internal clock Pϕ/8. |
| | | | | 1 | 1 | TCNT_0 counts falling edges of internal clock Pϕ/2. |
| | 0 | 1 | 0 | 0 | 0 | TCNT_0 counts rising edges of internal clock Pϕ/64. |
| | | | | 0 | 1 | TCNT_0 counts rising edges of internal clock Pϕ/32. |
| | | | | 1 | 0 | TCNT_0 counts falling edges of internal clock Pϕ/64. |
| | | | | 1 | 1 | TCNT_0 counts falling edges of internal clock Pϕ/32. |
| | 0 | 1 | 1 | 0 | 0 | TCNT_0 counts rising edges of internal clock Pϕ/8192. |
| | | | | 0 | 1 | TCNT_0 counts rising edges of internal clock Pϕ/1024. |
| | | | | 1 | 0 | TCNT_0 counts falling edges of internal clock Pϕ/8192. |
| | | | | 1 | 1 | TCNT_0 counts falling edges of internal clock Pϕ/1024. |
| | 1 | 0 | 0 | — | — | TCNT_0 is incremented by the TCNT_1 overflow signal. |
| TMR_1 | 0 | 0 | 0 | — | — | Clock input is disabled. |
| | 0 | 0 | 1 | 0 | 0 | TCNT_1 counts rising edges of internal clock Pϕ/8. |
| | | | | 0 | 1 | TCNT_1 counts rising edges of internal clock Pϕ/2. |
| | | | | 1 | 0 | TCNT_1 counts falling edges of internal clock Pϕ/8. |
| | | | | 1 | 1 | TCNT_1 counts falling edges of internal clock Pϕ/2. |
| | 0 | 1 | 0 | 0 | 0 | TCNT_1 counts rising edges of internal clock Pϕ/64. |
| | | | | 0 | 1 | TCNT_1 counts rising edges of internal clock Pϕ/32. |
| | | | | 1 | 0 | TCNT_1 counts falling edges of internal clock Pϕ/64. |
| | | | | 1 | 1 | TCNT_1 counts falling edges of internal clock Pϕ/32. |
| | 0 | 1 | 1 | 0 | 0 | TCNT_1 counts rising edges of internal clock Pϕ/8192. |
| | | | | 0 | 1 | TCNT_1 counts rising edges of internal clock Pϕ/1024. |
| | | | | 1 | 0 | TCNT_1 counts falling edges of internal clock Pϕ/8192. |
| | | | | 1 | 1 | TCNT_1 counts falling edges of internal clock Pϕ/1024. |
| | 1 | 0 | 0 | — | — | TCNT_1 is incremented upon compare match A of TCNT_0. |

(5) Flowchart


main
TCORA_0 = PULSE_CYCLE
TCORB_0 = PULSE_CYCLE/2
Pulse period setting: PULSE_CYCLE (H'09)
Duty cycle setting: 50%
TCORA_1 = PULSE_COUNT
Pulse count setting: PULSE_COUNT(H'07)
tmp = TCSR_0
TCSR_0 = H'06
- Clear CMFA (compare-match flag A).
- Output "1" on compare match of TCNT_0 with TCORA_0.
- Output "0" on compare match of TCNT_0 with TCORB_0.
TCR_0 = H'09
TCCR_0 = H'00
- TCNT_0 is cleared on compare-match A.
- TCNT_0 counts rising edges of internal clock Pϕ/8.
tmp = TCSR_1
TCSR_1 = H'10
- Clear CMFA (compare-match flag A).
TCR_1 = H'4C
- Enable CMIA_1 (compare-match A_1) interrupt.
- TCNT_1 is cleared on compare-match A.
- TCNT_1 is incremented on each compare-match A of TCNT_0.
TCNT_0 = 0
TCNT_1 = 0
Clear TNCT_0 and TCNT_1.
flg = 0
I = 0
Enable interrupts.
flg == 0?
Yes
No
I = 1
Disable interrupts.
End

### 5.4.3 cmia1_int Function

(1) Functional Overview

TCORA_1 compare-match interrupt handling routine that performs the processing necessary to stop the pulse output.

(2) Arguments

None

(3) Return value

None

(4) Internal Registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in the sample task and differ from their initial values.

- Timer Control Register_1 (TCR_1) Address: H'FFFFB1

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | CMIEA | 0 | R/W | Compare match interrupt enable A<br>0: Disables interrupt request (CMI1A) generation by CMFA in TCSR_1.<br>1: Enables interrupt request (CMI1A) generation by CMFA in TCSR_1. |

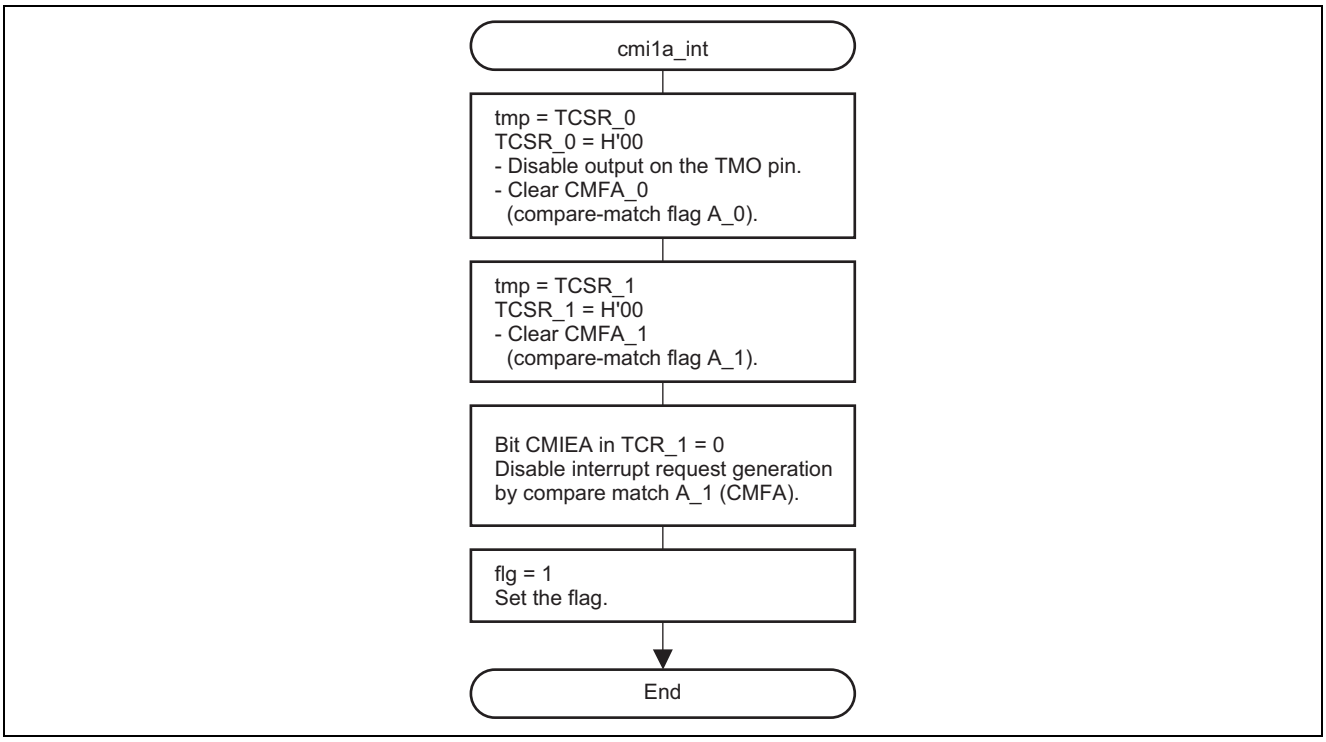
- Timer Control/Status Register_0 (TCSR_0) Address: H'FFFFB2

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | CMFA | 0 | R/W | Compare match flag A<br>0: TCNT_0 does not match the value in TCORA_0.<br>1: TCNT_0 matches the value in TCORA_0. |
| 3 | OS3 | 0 | R/W | Output select 3, 2 |
| 2 | OS2 | 0 | R/W | Selects the mode of output on the TMO_0 pin upon compare match B (i.e., TCNT_0 matches TCORB_0).<br>00: No change |
| 1 | OS1 | 0 | R/W | Output select 1, 0 |
| 0 | OS0 | 0 | R/W | Selects the mode of output on the TMO_0 pin upon compare match A (i.e., TCNT_0 matches TCORA_0).<br>00: No change |

- Timer Control/Status Register_1 (TCSR_1) Address: H'FFFFB3

| Bit | Bit Name | Setting | R/W | Function |
|---|---|---|---|---|
| 6 | CMFA | 0 | R/W | Compare match flag A<br>0: TCNT_1 does not match the value in TCORA_1.<br>1: TCNT_1 matches the value in TCORA_1. |

(5) Flowchart


cmi1a_int
tmp = TCSR_0
TCSR_0 = H'00
- Disable output on the TMO pin.
- Clear CMFA_0
(compare-match flag A_0).
tmp = TCSR_1
TCSR_1 = H'00
- Clear CMFA_1
(compare-match flag A_1).
Bit CMIEA in TCR_1 = 0
Disable interrupt request generation
by compare match A_1 (CMFA).
flg = 1
Set the flag.
End

## Revision Record

| | | Description | |
|---|---|---|---|
| Rev. | Date | Page | Summary |
| 1.00 | Mar.10.06 | — | First edition issued |
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