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H8SX Family

Producing a Pulse Output

Introduction

The 16-bit timer pulse unit (TPU) is used to produce a pulse signal with a period of 25.6 µs and a 50% duty cycle.

Target Device

H8SX/1582F

Contents

1. Specifications

- An example of the output pulse is shown in figure 1.
- Pulses with a period of 25.6 µs and a 50% duty cycle are output.

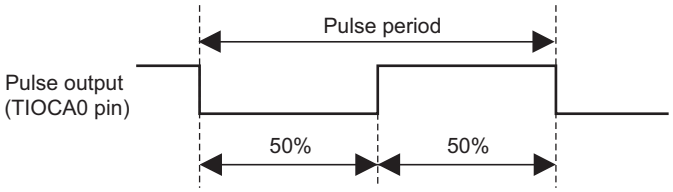


Figure 1 Example of Output Pulse

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	5 MHz
	System clock (Iϕ):	40 MHz
	Peripheral module clock (Pϕ):	20 MHz
	External bus clock (Bϕ):	20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)	
Development tool	High-performance Embedded Workshop Version 4.00.02	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 2 Section Setting

Address	Section Name	Description
H'001000	P	Program area

3. Description of Modules Used

In this sample task, the 16-bit timer pulse unit (TPU) is used to output pulses with a period of 25.6 µs and a 50% duty cycle. Figure 2 shows a block diagram of channel 0 of the TPU (TPU_0). This sample task uses the following features of the TPU.

— Automatic generation of pulses by hardware, without software intervention (output compare)
— Counter clearing on compare match
— Output toggling on compare match

The TPU registers are described below.

- Timer start register (TSTR)
  TSTR starts or stops the TCNT counters on channels 0 to 5 individually. TCNT must be stopped before setting the operating mode in the TMDR register or setting the clock source for TCNT in the TCR register.

- Timer control register_0 (TCR_0)
  TCR controls TCNT on each channel. The TPU has one TCR for each channel; i.e., a total of six TCR registers. TCR must be set while the corresponding TCNT is stopped.

- Timer I/O control register H_0 (TIORH_0)
  TIOR controls the TGR registers. The TPU has two TIOR registers each for channels 0 and 3, and one each for channels 1, 2, 4, and 5, for a total of eight TIOR registers. Note that TIOR is affected by the setting of TMDR.
  The initial output specified by TIOR takes effect while the counter is stopped (the corresponding CST bit in TSTR is clear). In PWM mode 2, TIOR specifies the output at the point when the counter is cleared to 0. However, if TGRC or TGRD is specified for buffer operation, this setting has no effect and TGRC or TGRD operates as a buffer register.

- Timer counter_0 (TCNT_0)
  TCNT is a 16-bit readable/writable counter. One TCNT is provided for each channel, which makes a total of six TCNT counters. TCNT is initialized to H'0000 when the chip is reset or enters hardware standby mode. Access to TCNT in 8-bit units is not allowed; always access in 16-bit units.

- Timer general register A_0 (TGRA_0)
  TGR is a 16-bit readable/writable register that can be used as either an output compare or input capture register. The TPU has four TGR registers each for channels 0 and 3 and two each for channels 1, 2, 4, and 5, for a total of 16 TGR registers. Access to TGR in 8-bit units is not allowed; always access in 16-bit units.
  TGRC and TGRD of channels 0 and 3 can be configured as buffer registers for buffer operation, in which TGRC and TGRD act as the buffer register for TGRA and TGRB, respectively.

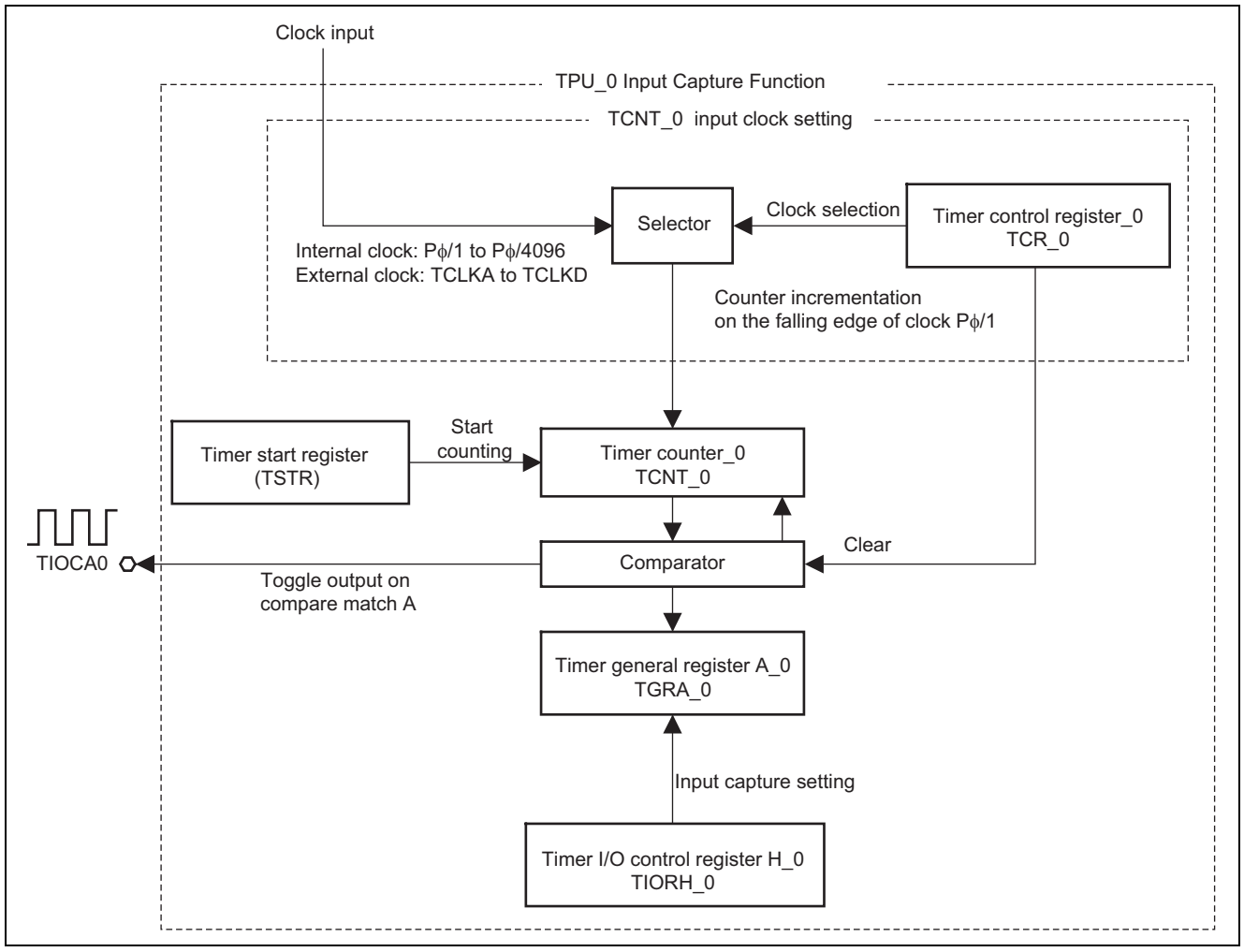


Figure 2 Block Diagram of TPU Channel 0 (TPU_0)

4. Description of Operation

Figure 3 illustrates the principles of operation for the pulse output. The hardware processing and software processing of figure 3 are explained in table 3.

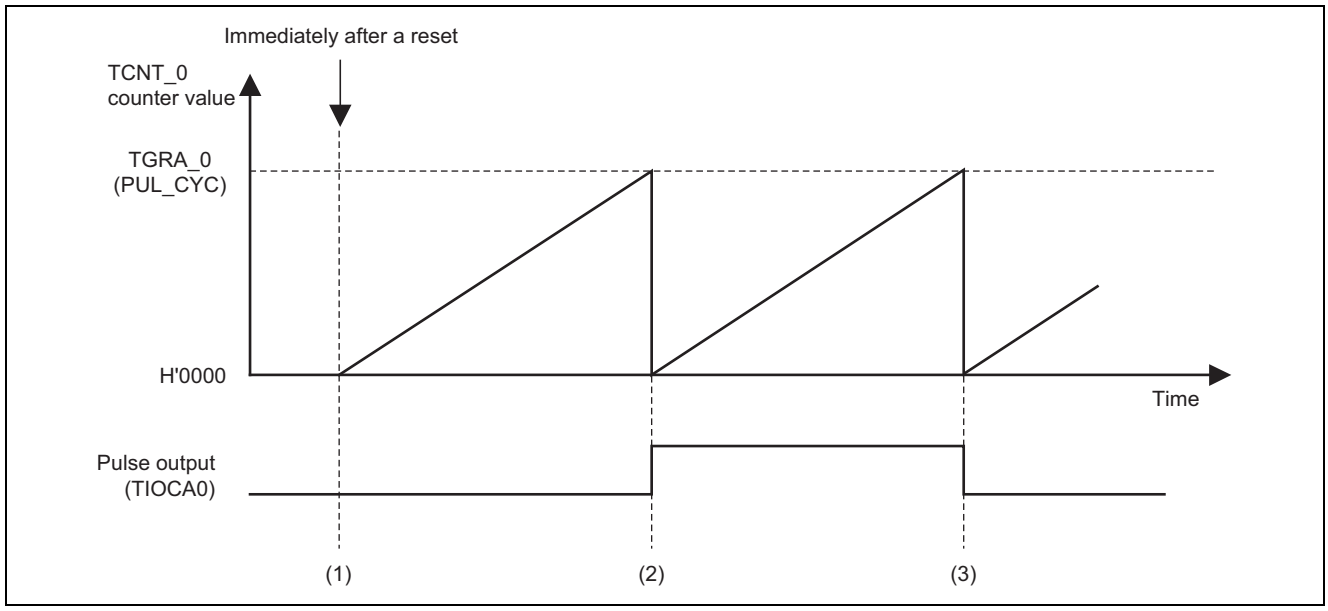


Figure 3 Operation Principles of Pulse Output

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings (a) Select Pϕ/1 as the input clock for TCNT_0. (b) Select clearing of TCNT_0 by compare match A. (c) Set so that the output is toggled by compare match A of TPU_0. (d) Set half the pulse period (PUL_CYC) in TGRA_0. (e) Start the counter.
(2)	(a) Generate compare match A in TPU_0. (b) Clear the counter. (c) Output a high level from TIOCA_0.	No processing
(3)	(a) Generate compare match A in TPU_0. (b) Clear the counter. (c) Output a low level from TIOCA_0.	No processing

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
main	Main routine • Makes settings for toggle output upon compare match A • Produces pulse output

5.2 Vector Table

Table 5 Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main

5.3 Constants

Table 6 Description of Constant

Label	Setting	Description	Used In
PUL_CYC	H'00FF	Counter value for half the pulse period	main

5.4 RAM Usage

This sample task does not use RAM.

5.5 Formula for Pulse Period Calculation

The following formula is used to calculate the period of the pulse.

Pulse period = (value set in TGRA_0 + 1) × 2 × period of Pϕ

Since TGRA_0 = PUL_CYC in this sample task, the period is 25.6 μs as calculated below.

Pulse period = (H'FF + 1) × 2 × 1/20 MHz
= 256 × 2 × 0.05 μs = 25.6 μs

5.6 Internal Registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in the sample task and differ from their initial values.

- System Clock Control Register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System clock (Iϕ) select
9	ICK1	0	R/W	These bits select the system clock frequency. The CPU, DMAC, and DTC modules are driven by the system clock.
8	ICK0	0	R/W	000: Input clock × 8
6	PCK2	0	R/W	Peripheral clock (Pϕ) select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 4
2	BCK2	0	R/W	External bus clock (Bϕ) select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module Stop Control Register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

- Module Stop Control Register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module Stop Control Register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM (H'FFF9000 to H'FFFBFFF)
0	MSTPC0	0		The values written to MSTPC1 and MSTPC0 should always be the same.

- Timer Start Register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	0	R/W	Counter start 5 to 0
4	CST4	0	R/W	Each of these bits starts or stops operation of the corresponding TCNT counter of the TPU.
3	CST3	0	R/W	
2	CST2	0	R/W	0: Stops counting by TCNT_5 to TCNT_0.
1	CST1	0	R/W	1: Starts counting by TCNT_5 to TCNT_0.
0	CST0	1	R/W	

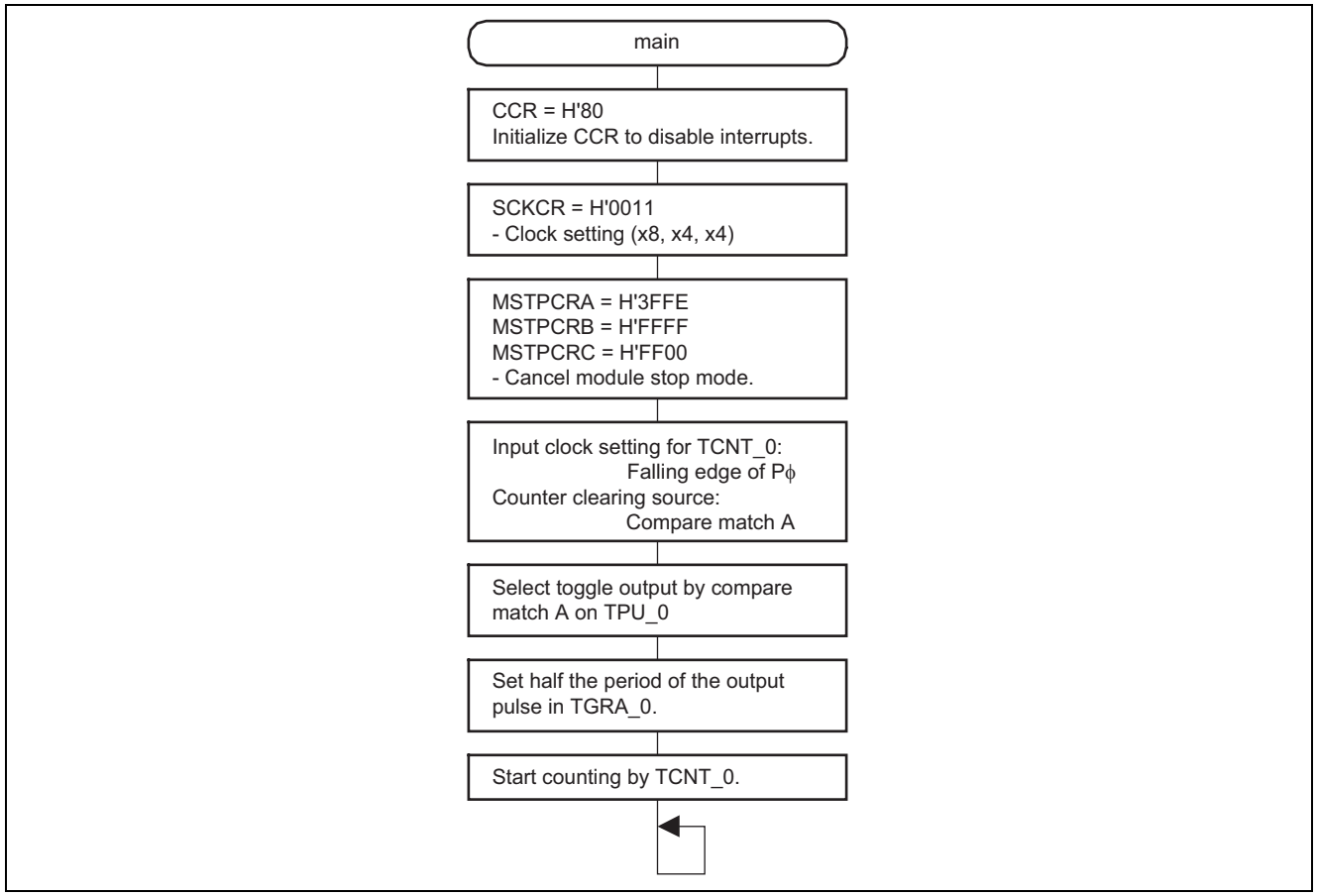
- Timer Control Register_0 (TCR_0) Address: H'FFFFC0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter clear 2 to 0
6	CCLR1	0	R/W	These bits select the counter clearing source
5	CCLR0	1	R/W	001: Clear TCNT_0 upon compare match or input capture by TGRA.
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	These bits select the edge of the input clock. 00: TCNT_0 counts falling edges.
2	TPSC2	0	R/W	Timer prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the counter clock source.
0	TPSC0	0	R/W	000: TCNT_0 is driven by Pϕ/1.

- Timer I/O Control Register H_0 (TIORH_0) Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Function
3	IOA3	0	R/W	I/O control A3 to A0
2	IOA2	0	R/W	These bits set the function of TGRA_0.
1	IOA1	1	R/W	0011: TGRA_0 operates as an output compare register. TIOCA0
0	IOA0	1	R/W	pin output is toggled upon compare match with TGRA_0; the initial output is 0.

6. Flowchart


main
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0011
- Clock setting (x8, x4, x4)
MSTPCRA = H'3FFE
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
- Cancel module stop mode.
Input clock setting for TCNT_0:
Falling edge of Pϕ
Counter clearing source:
Compare match A
Select toggle output by compare match A on TPU_0
Set half the period of the output pulse in TGRA_0.
Start counting by TCNT_0.

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.10.06	—	First edition issued

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