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# M16C/28, 29 Group

## Precautions for Timer S

## 1. Abstract

The timer S in the M16C/28,29 group microcomputers has two functions: a time measurement function and a waveform generation function. This application note describes precautions to be taken for each function.

## 2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/28, 29 Group

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## 3. Precautions for Time Measurement Function

The following explains the device operation when using the time measurement function of timer S.

### 3.1 About Initialization

If timer S is initialized using a program similar to the one shown in the example below, a problem may occur that if an active edge of time measurement occurs at the channel pin before an instruction in the ICOC Interrupt 0 Control Register is executed after the Interrupt Enable Register was enabled, the ICOC interrupt request bit may not be set to “1”. Please change the program to the one shown in the example program with corrective measures incorporated.

- Example program

```
        •
        •
        •
mov.b   #001h,g1fs      ; Function select register
                        ;       Select the channel 0 time measurement function
mov.b   #001h,g1fe      ; Function enable register
                        ;       Channel 0 function enabled
mov.b   #000h,g1ir      ; Interrupt request register
mov.b   #001h,g1ie0     ; Interrupt enable register 0
                        ;       Channel 0 interrupt enabled
mov.b   #004h,icoc0ic   ;ICOC interrupt 0 control register
bset    bts             ;       Base timer starts counting
        •
        •
        •
```

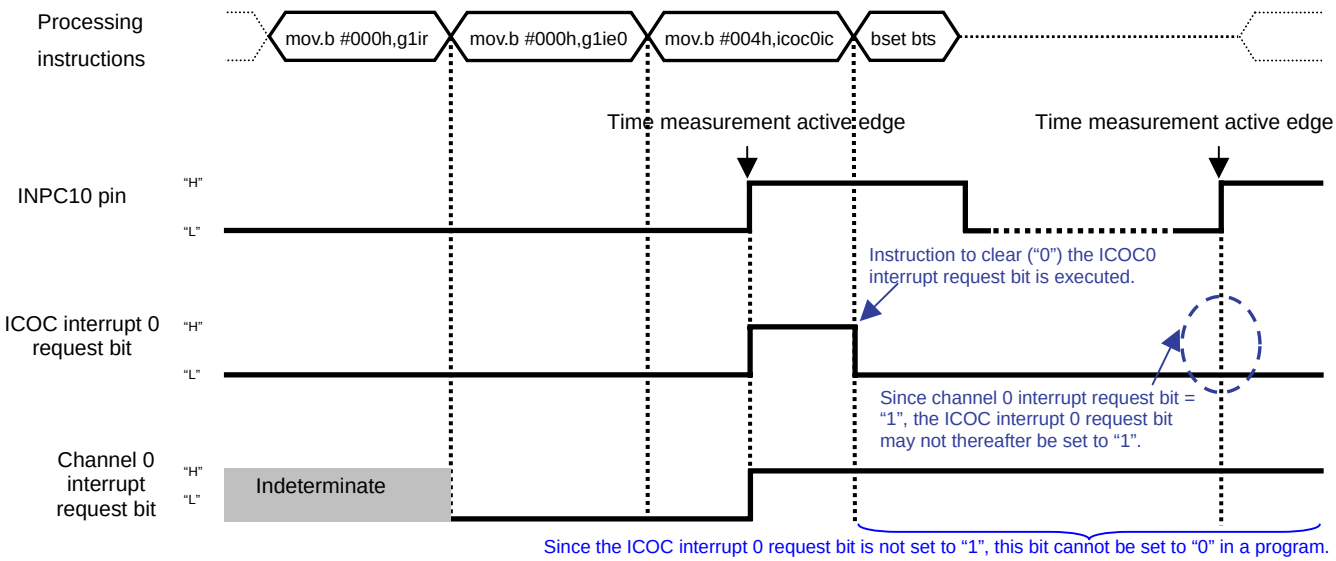


**Figure 3.1 Timer Initialization (without Corrective Measures) and Input Timing of the Time Measurement Active Edge**

• Example program with corrective measures incorporated

```
        •
        •
        •
mov.b   #001h,g1fs      ; Function select register
                        ;       Select the channel 0 time measurement function
mov.b   #001h,g1fe      ; Function enable register
                        ;       Channel 0 function enabled
mov.b   #000h,g1ir      ; Interrupt request register
mov.b   #001h,g1ie0     ; Interrupt enable register 0
                        ;       Channel 0 interrupt enabled
or.b    #004h,icoc0ic   ; ICOC interrupt 0 control register
bset    bts             ;       Base timer starts counting
        •
        •
        •
```

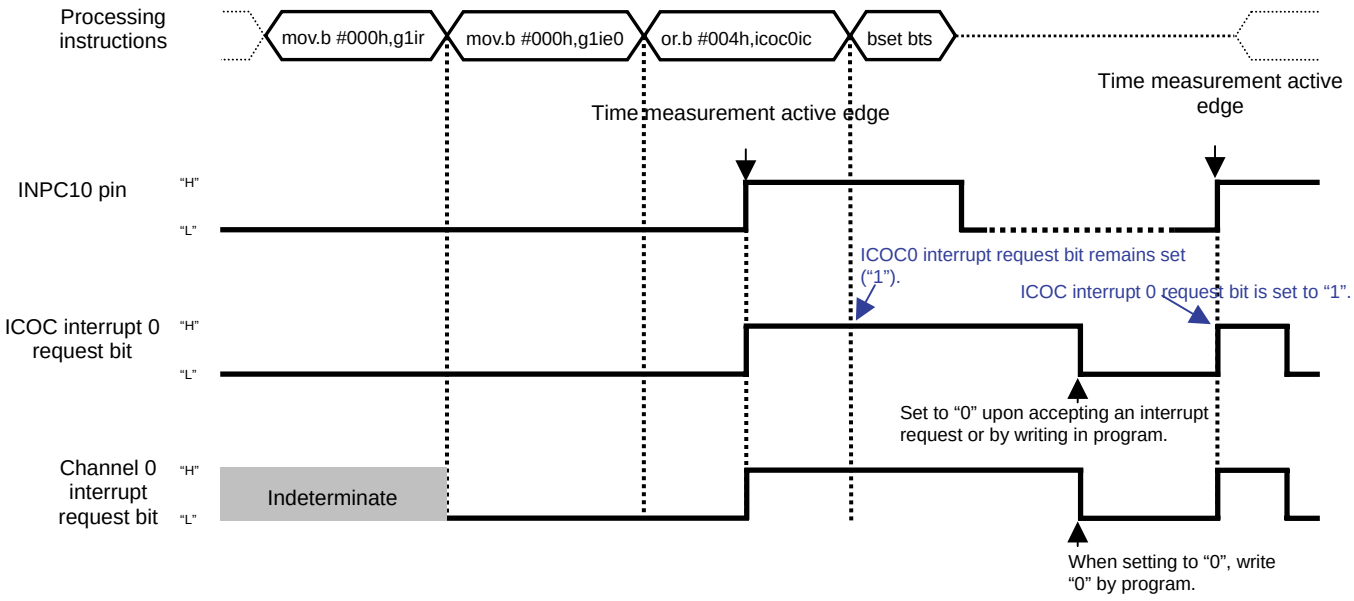


**Figure 3.2 Timer Initialization (with Corrective Measures) and Input Timing of the Time Measurement Active Edge**

## 4. Precautions for Waveform Generation Function

The following explains the device operation when using the waveform generation function of timer S while single-phase waveform output mode is selected.

### 4.1 Stopping the Base Timer

The base timer count can be made to stop by setting bit 4 (BTS) in the Base Timer Control Register (G1BCR1) to “0” (= base timer reset) while the base timer count is in progress. When the base timer count stops, the output level on each channel is held intact as is. Even after the base timer count has restarted, the output level is retained intact until the waveform generation register and the count values match next time.

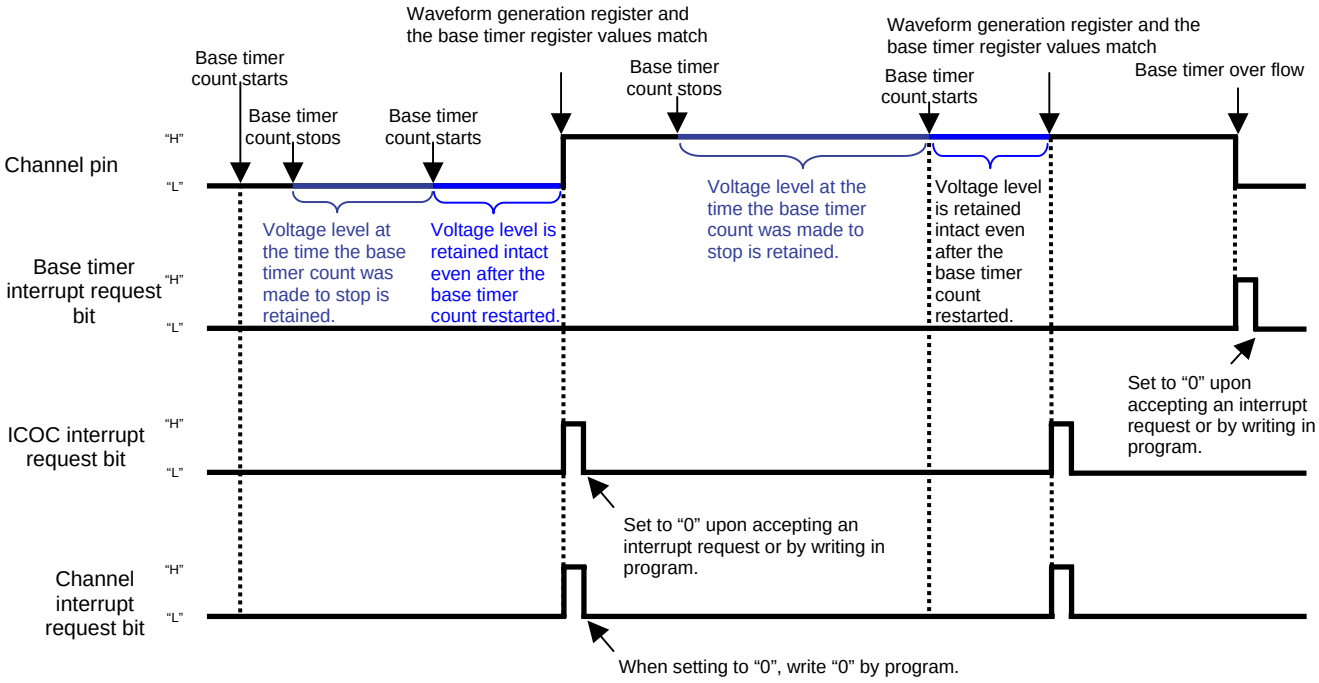


**Figure 4.1 Output Waveform Changes as the Base Timer Stops and Restarts**

## 4.2 Disabling/Enabling the Channel Function

When the channel function is disabled with the function enable register (G1FE: $0326_{16}$), the target channel pin is changed for port function. Figure 4.2 shows how the output level at the channel pin will change when the channel function is disabled while active and when reenabled while inactive. The output level on the channel is retained when the base timer count is made to stop, but when the channel function is disabled, the port function is enabled and the output level at the port changes. When the channel function is reenabled while inactive, the output level at the channel pin returns to the one that was being output before the base timer count was made to stop.

While the port function is on, port settings are reflected at the output simultaneously with a write operation executed, regardless of whether the base timer count is on or off. When the channel function is enabled and remains enabled, the pin cannot be used as a port because the ICOC function is active.

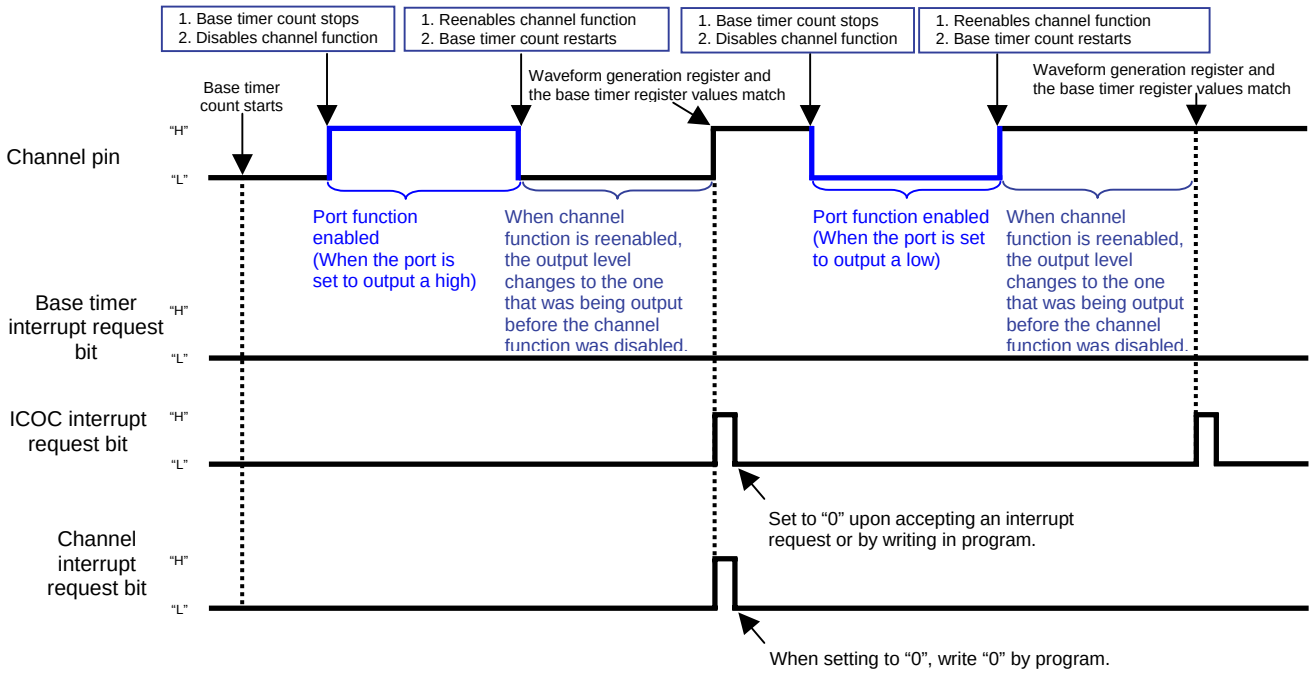


**Figure 4.2 Output Waveform Changes as the Channel Function is Disabled and Reenabled**

## 4.3 Output Initial Value Select Bit

The output level at the channel pin is made to change by setting the output initial value select bit (bit 4: IVL) in the Waveform Generation Control Register j (j = 0 to 7). When the channel function is enabled (= "1"), the pin outputs the voltage level that has been set by the output initial value select bit.

Be aware that if the initial output value select bit is rewritten while the channel function is active and the base timer count is on, as shown in Figure 4.3, the changed value will be output from the pin. Since the same symptom is derived by writing to the Waveform Generation Control Register j (j = 0 to 7), make sure the Waveform Generation Control Register j (j = 0 to 7) is not refreshed during that time. Furthermore, if the output initial value select bit is changed by writing to it while the channel function is inactive, the changed value is output from the channel pin the next time the channel function is enabled.

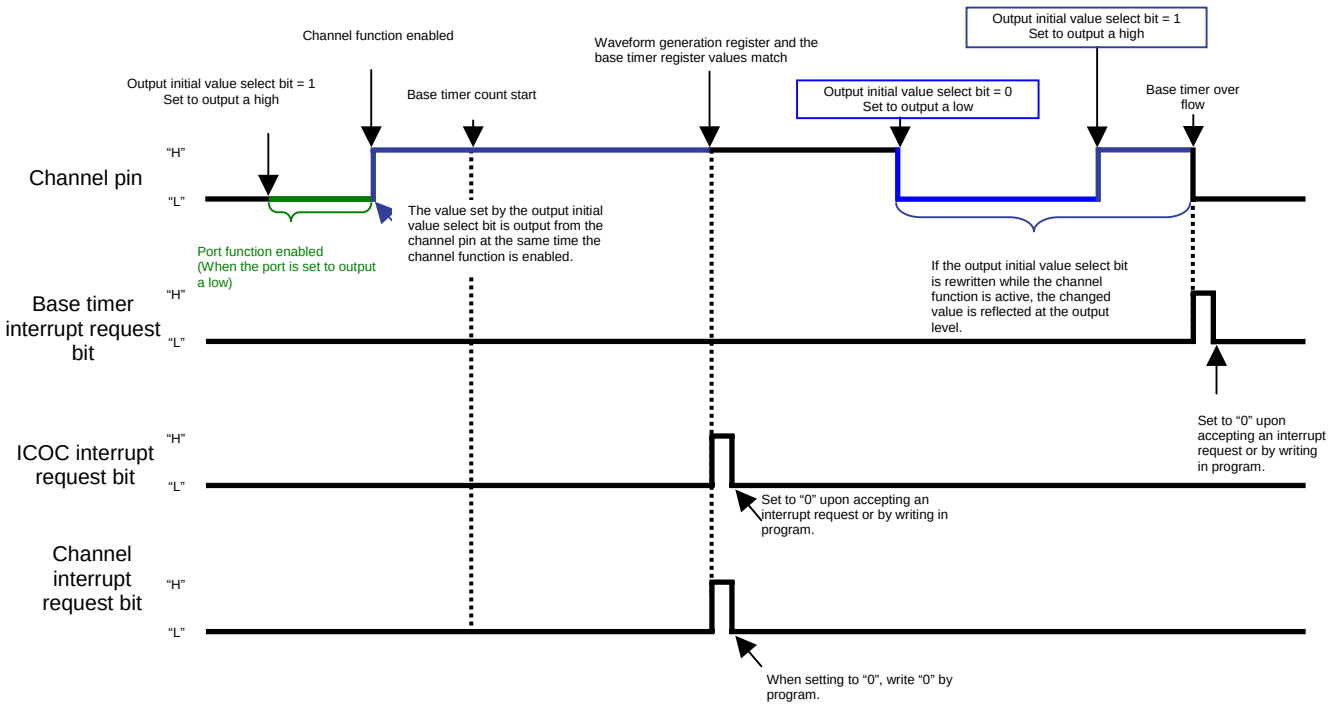


**Figure 4.3 Output Waveform Changes as the Output Initial Value Select Bit is Rewritten**

## 4.4 Base Timer Reset

### 4.4.1 Overview

The period of the pulses output from the channel pin can be changed by using the base timer reset function. The cause for which the base timer is reset can be selected from the following three. The following explains the base timer reset function for the case where the reset cause (2) is selected.
(1) Base Timer Reset Register (G1BTRR)
(2) Waveform Generation Register 0 (G1PO0)
(3) Low-level input to the INT1 pin

### 4.4.2 Regarding the Use of Waveform Generation Register 0 (G1POCR0)

When Waveform Generation Register 0 is used as the cause of base timer reset, the base timer count is reset when the value of the base timer count and that of Waveform Generation Register 0 have matched. When the base timer is thus reset, the OUTC10 pin is pulsed high for a duration equal to 2 count source cycles of the base timer. Be aware that the pulses output from the OUTC10 pin cannot be disabled in software.
Furthermore, when the value of the base timer count and that of Waveform Generation Register 0 match, the channel 0 interrupt request bit (G1IR0) is set to “1”, and the ICOC interrupt 0 request bit (IR_ICOC0IC) or ICOC interrupt 1 request bit (IR_ICOC1IC) is set to “1”. The base timer interrupt request bit is not set to “1” and cannot therefore be used.
Note that unless the channel 0 interrupt request bit (G1IR0) is set to “0” in a program, the ICOC interrupt 0 request bit (IR_ICOC0IC) or ICOC interrupt 1 request bit (IR_ICOC1IC) will not be set to “1”.

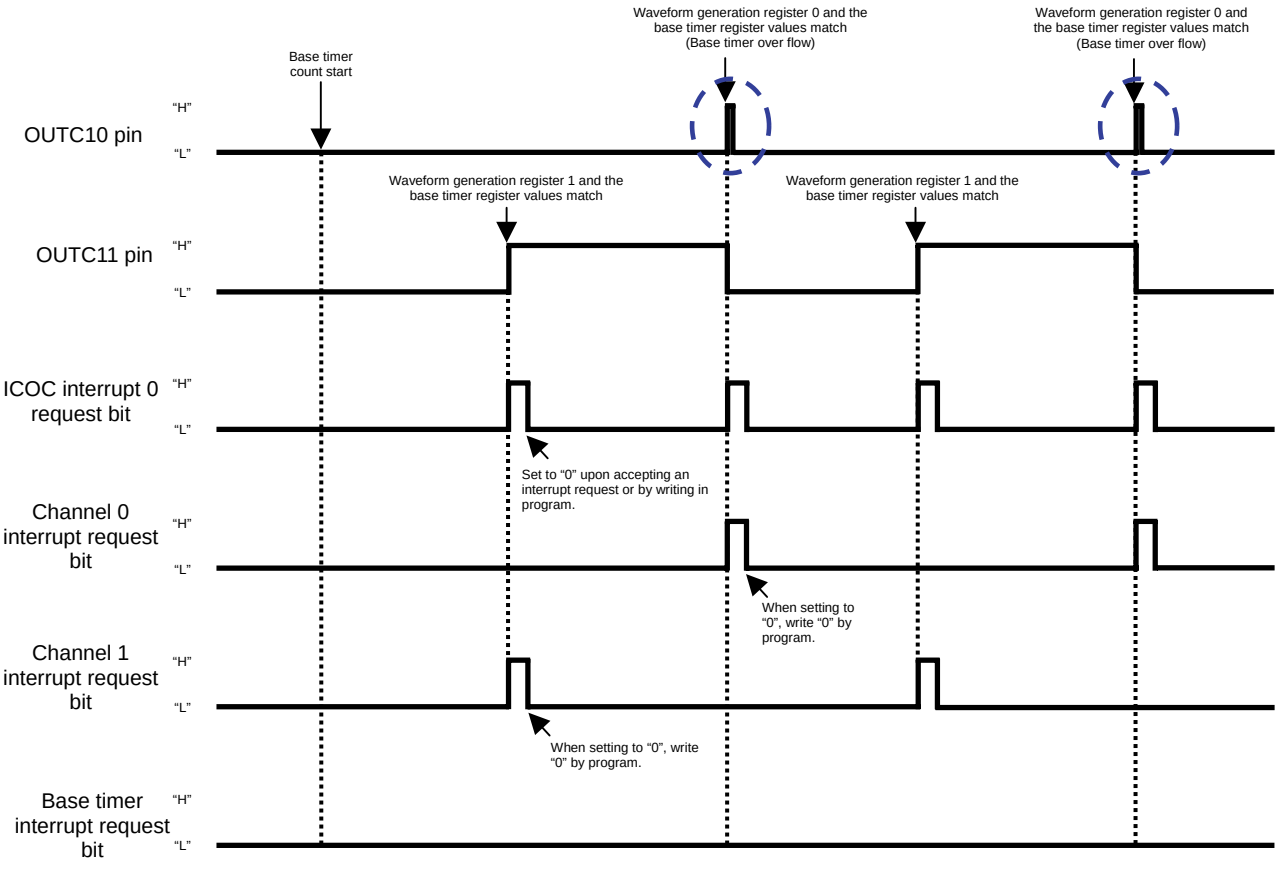


**Figure 4.4 Timing Diagram when Waveform Generation Register 0 is Used for Base Timer Reset**

## 4.5 Timing with which the Waveform Generation Register

### 4.5.1 Overview

If during initialization, the timing with which the waveform generation register will be reloaded is set by bit 5 (RLD) in the waveform generation control register in a manner similar to the example program shown below, the waveforms output at the time the base timer count starts will vary depending on the set value of RLD, as shown in Figure 4.5 and Figure 4.6.

- Example program 1: RLD = 0 (reloaded upon write)

```
mov.b    #000h,g1pocr0        ; Waveform generation control register 0
                              ;RLD = 0 (reloaded upon write)
mov.w    #5000-1,g1po0        ; Waveform generation register 0
         •
         •
         •
bset bts                      ; Base timer starts counting
```

- Example program 2: RLD = 1 (reloaded upon base timer reset)

```
mov.b    #020h,g1pocr0        ; Waveform generation control register 0
                              ;RLD = 1 (reloaded upon base timer reset)
mov.w    #5000-1,g1po0        ; Waveform generation register 0
         •
         •
         •
bset     bts                  ; Base timer starts counting
```

### 4.5.2 When Waveform Generation Control Register Bit 5 (RLD) is Set to “0” (Reloaded Upon Write)

When the set value of the waveform generation register and the base timer count value have matched first time after the base timer count started, the level being output from the channel changes and the ICOC interrupt request bit is set to “1”. Since the waveform generation register is reloaded simultaneously with a write to it, the waveform generation register value that matches the base timer count value first time is the one that has been set in it.

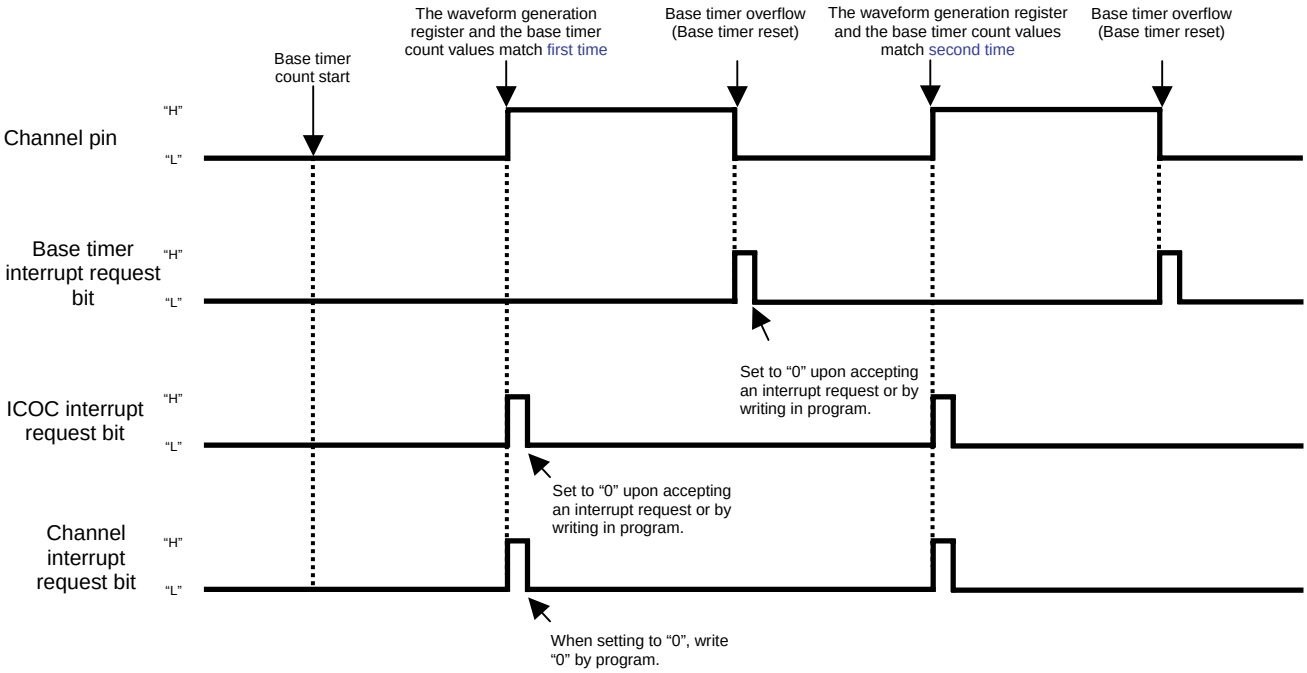


**Figure 4.5 Reloaded Upon Write (RLD=0)**

### 4.5.3 When Waveform Generation Control Register Bit 5 (RLD) is Set to “1” (Reloaded Upon Base Timer Reset)

It is not the value set for the waveform generation register, but an indeterminate value present in it at reset that matches the timer count value first time after the base timer count has started. When an indeterminate value in the waveform generation register and the base timer count value have matched, a high-level signal is output from the channel, but the ICOC interrupt request bit is not set to “1”. Since the waveform generation register is not reloaded with the value set for it unless the base timer is reset once, the value of the waveform generation register that matches the timer count value first time is indeterminate. The waveform generation register is reloaded with its set value when the base timer is reset, so that when the base timer and the waveform generation register match second time and onward, the output pulse from the channel changes with the value set in the waveform generation register and the ICOC interrupt request bit is set to “1” each time.

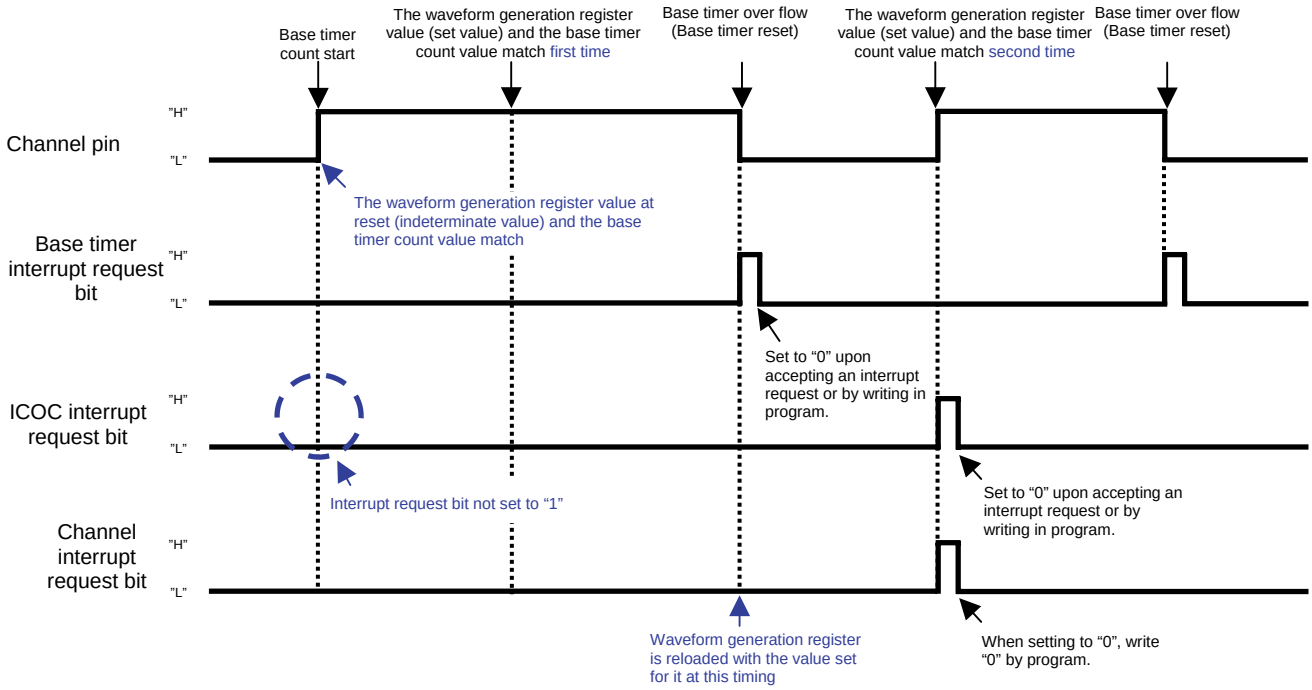


**Figure 4.6 Reloaded Upon Base Timer Reset (RLD=1)**

- About the corrective measures in software

If when bit 5 (RLD) in the waveform generation control register is set to “1” (reloaded upon base timer reset) the indeterminate value that is first output from the channel presents a problem, the program may be changed to the one shown below. That way, a device operation similar to the one shown in Figure 4.5 will be guaranteed.

```
mov.b   #000h,g1pocr0       ; Waveform generation control register 0
                            ;RLD = 0 (reloaded upon reload)
mov.w   #5000-1,g1po0       ; Waveform generation register 0
mov.b   #020h,g1pocr0       ; Waveform generation control register 0
                            ;RLD = 1 (reloaded upon base timer reset)
        •
        •
        •
bset    bts                 ; Base timer starts counting
```

## 5. Reference

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