MOSFET

Precautions for parallel connection of power MOSFETs

Introduction

In this application note, we will explain the precautions for parallel connection of power MOSFETs.

Contents

1. Overview

In some cases, multiple devices may be connected in parallel to achieve higher power system or lower power MOSFET losses. In this case, it is important to balance the current flowing through each device, as if the current becomes unbalanced and concentrated on some devices, they may suffer excessive losses and be destroyed. Therefore, sufficient consideration is required for device characteristics variation, substrate layout symmetry, gate drive circuit, etc. Also, the problems that occur when using parallel connection can be classified into those that occur during the conduction period (steady state) of the power MOSFET and those that occur during the switching period (transient state) of the power MOSFET. These have different causes and require different countermeasures. The precautions for parallel connection are shown in Table 1-1.

Table 1-1. precautions for parallel connection of power MOSFETs

	During conduction (steady state)	During switching (transient state)
Circuit factors	▪ Symmetry of board layout (resistance component)	▪ Symmetry of board layout (resistance component) ▪ Avoid avalanche operation ▪ Gate oscillation
Power MOSFET factors	▪ Variation of $R_{DS(on)}$	▪ Variation of $V_{GS(th)}$

2. Precautions during conduction (steady state)

When power MOSFETs are turned on, the difference in $R_{DS(on)}$ of the parallel-connected devices and the resistance of the substrate and wiring cause an imbalance in the drain current. This current imbalance not only affects the loss of the devices during conduction, but also changes the current value during switching, affecting the transient loss. Therefore, it is necessary to take measures such as selecting devices from the same lot and minimizing the difference in $R_{DS(on)}$, and designing the parallel paths symmetrically. The $R_{DS(on)}$ of power MOSFETs has a positive temperature coefficient. Therefore, the current imbalance that occurs will self-balance to equalize, and the risk of failure due to heat generation during conduction is low.

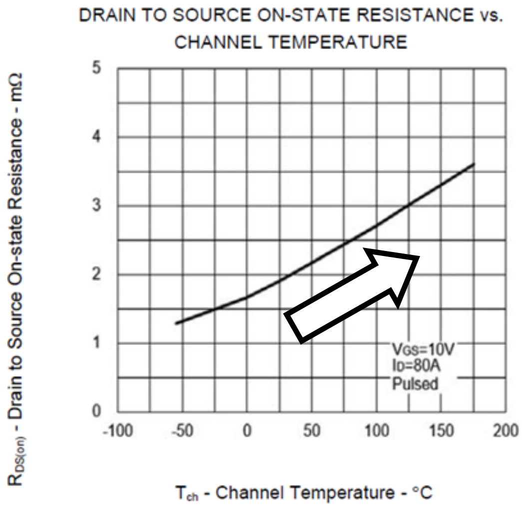

Fig. 2-1 $R_{DS(on)}$ Temperature characteristics

3. Precautions during switching (transient state)

When power MOSFETs are switching (transient state), the difference in $V_{GS(th)}$ of the parallel-connected devices and the difference in the inductance components of the substrate and wiring cause an imbalance in the drain current. Therefore, it is necessary to take measures such as selecting devices from the same lot and minimizing the difference in $V_{GS(th)}$, and designing the layout of the parallel paths symmetrically. When operating in avalanche mode in parallel connection, there is a possibility of destroying the device with low drain withstand voltage by concentrating all the current on it, so be careful.

3.1 Example of current imbalance during switching when samples with different $V_{GS(th)}$ are connected in parallel

The following figure shows the operation waveforms when samples with intentionally different $V_{GS(th)}$ are connected in parallel and switched. At turn-on, MOSFET2 with smaller $V_{GS(th)}$ turns on first, and at turn-off, MOSFET1 with larger $V_{GS(th)}$ turns off first, causing current imbalance. The current imbalance caused by the difference in $V_{GS(th)}$ can be prevented by using devices from the same lot and minimizing the difference in $V_{GS(th)}$ between MOSFETs.

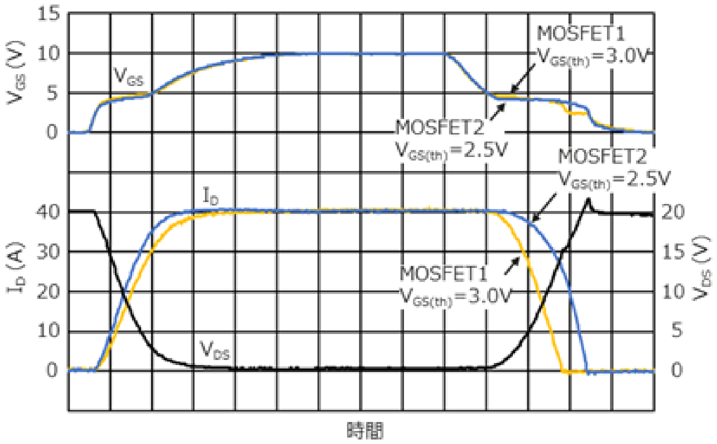

Fig. 3-1　Current imbalance waveforms during switching

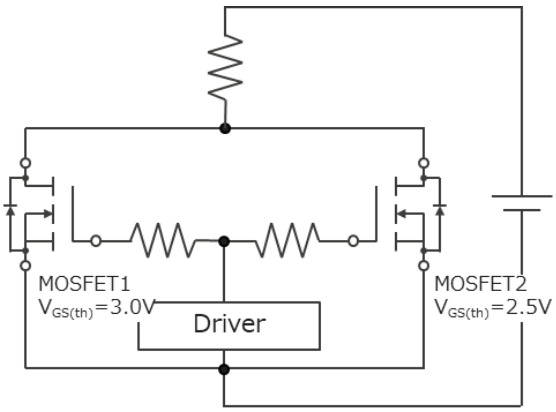

Fig. 3-2　Evaluation circuit

4. Regarding parasitic oscillation

When using power MOSFETs in parallel, parasitic oscillations are more likely to occur than when using a single power MOSFET. If the gates of the power MOSFETs are connected directly without resistance, oscillating waveforms may be seen on the gates because of parasitic parameters. These oscillating waveforms are caused by the voltage oscillation due to the drain wiring inductance (Ld) during switching (especially turn-off) and the resonant circuit composed of the gate-drain capacitance (Cgd) and the gate wiring inductance (Lg). Therefore, when there is no gate resistance, the Q factor (sharpness) of the resonant circuit becomes large, and when the resonance condition is met, a large oscillating voltage is generated between the gate-drain and the gate-source, causing parasitic oscillation. As a countermeasure, parasitic oscillation is suppressed by connecting a resistance (RG) to the gate of each device.

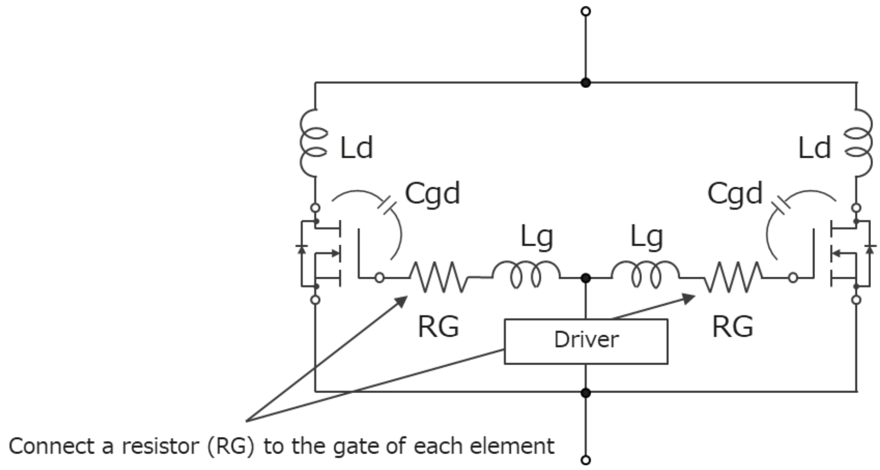

Fig. 4-1 Measures against gate oscillation

Revision History

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Feb.29 2024	-	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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