RX65N/RX651 Group RX62N Group

Points of Difference Between RX65N Group and RX62N Group

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Introduction

This application note is intended as a reference for confirming the points of difference between the overview of functions, the I/O registers, the pin functions of the RX65N Group and RX62N Group, and notes on migration.

Unless specifically otherwise noted, the information in this application note applies to the 144-/145-pin package version of the RX65N Group and the 144-/145-pin package version of the RX62N Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Devices

RX65N Group and RX62N Group

Contents

1. Comparison of Functions of RX65N Group and RX62N Group

A comparison of the functions of the RX65N Group and RX62N Group is provided below. For details of the functions, see section 2, Comparative Overview of Functions and section 5, Reference Documents.

Table 1.1 is a Comparison of Functions of RX65N and RX62N.

Table 1.1 Comparison of Functions of RX65N and RX62N

Function	RX62N	RX65N
CPU	△	
Operating Modes	△	
Reset	△	
Option-Setting Memory	×	○
Voltage Detection Circuit (LVD):RX62N,(LVDA):RX65N	△	
Clock Generation Circuit	△	
Clock Frequency Accuracy Measurement Circuit(CAC)	×	○
Low Power Consumption	△	
Battery Backup Function	×	○
Register Write Protection Function	×	○
Exceptions	△	
Interrupt Controller(ICUa):RX62N,(ICUB):RX65N	△	
Buses	△	
Memory Protection unit(MPU)	△	
DMA Controller (DMACA):RX62N,(DMACAa):RX65N	△	
EXDMA Controller (EXDMAC):RX62N,(EXDMACa):RX65N	△	
Data Transfer Controller(DTCa):RX62N,(DTCb):RX65N	△	
Event Link Controller(ELC)	×	○
IO Ports	△	
Multi-Function Pin Controller(MPC)	×	○
Multi-Function Timer Pulse Unit 2(MTU2)	○	×
Multi-Function Timer Pulse Unit 3(MTU3a)	×	○
Port Output Enable 2(POE2)	○	×
Port Output Enable 3(POE3a)	×	○
16-BitTimer Pulse Unit(TPUa)	×	○
Programmable Pulse Generator(PPG)	△	
8-Bit Timer(TMR)	△	
Compare Match Timer(CMT)	△	
Compare Match Timer W(CMTW)	×	○
Real Time Clock(RTC):RX62N,(RTCd):RX65N	△	
Watchdog Timer(WDT):RX62N,(WDTA):RX65N	△	
Independent Watchdog Timer (IWDT):RX62N,(IWDTa):RX65N	△	
Ethernet Controller(ETHERC)	△	
DMA Controller for the Ethernet Controller (EDMAC):RX62N,(EDMACa):RX65N	△	
USB2.0FSHost/Function Module(USB):RX62N,(USBb):RX65N	△	
Serial Communication Interface(SCIa):RX62N,(SCIg,SCIi,SCIh):RX65N	△	
I²C-bus Interface(RIIC):RX62N,(RIICa):RX65N	△	
CAN Module(CAN)	△	
Serial Peripheral Interface(RSPI):RX62N,(RSPIc):RX65N	△	
Quad Serial Peripheral Interface (QSPI)	×	○
CRC Caluculator(CRC):RX62N,(CRCA):RX65N	△	
SD Host Interface(SDHI)	×	○

Function	RX62N	RX65N
SD Slave Interface (SDSI)	×	○
Multi Media Card Interface (MMCIF)	×	○
Parallel Data Capture Unit (PDC)	×	○
Boundary Scan	△	
AESa	×	○
RNGa	×	○
12-bit A/D Converter(S12AD):RX62N,(S12ADFa):RX65N	△	
10-bir A/D Converter(ADa)	○	×
D/A Converter:RX62N 12-bit DA Converter(R12DA):RX65N	△	
Temperature Sensor(TEMPS)	×	○
Data Operation Circuit(DOC)	×	○
RAM	△	
Standby RAM	×	○
ROM(Code Flash) : RX62N Flash Memory : RX65N	△	
Flash Memory(E2 Data Flash)	○	×

Note: ○: Function implemented, x: Function not implemented, △: Differences exist between implementation of function on RX62N and RX65N.

2. Comparative Overview of Functions

2.1 CPU

Table 2.1 shows a Comparative Listing of CPU Specifications, and Table 2.2 shows a Comparative Listing of CPU Registers.

Table 2.1 Comparative Listing of CPU Specifications

Item	RX62N	RX65N
CPU	• Maximum operating frequency : 100MHz • 32-bit RX CPU • Minimum instruction execution time : One instruction per state (cycle of the system clock) • Address space : 4-Gbyte linear • Register set of the CPU General purpose : Sixteen 32-bit registers Control : Nine 32bit registers Accumulator : One 64-bit registers • Basic instructions : 73 • Floating-point instructions : 8 • DSP instructions : 9 • Addressing modes : 10 • Data arrangement Instructions : Little endian Data : Selectable as little endian or big endian • On-chip 32-bit multiplier : 32×32 →bits • On-chip divider: : 32/32→32bits • Barrel shifter : 32bits • Memory protection unit (MPU)	• Maximum operating frequency : 120MHz • 32-bit RX CPU(RXv2) • Minimum instruction execution time : ne instruction per state (cycle of the system clock) • Address space : 4-Gbyte linear • Register set of the CPU General purpose : Sixteen 32-bit registers Control : Ten 32-bit registers Accumulator : Two 72-bit registers • Basic instructions : 75 • Floating-point instructions : 11 • DSP instructions : 23 • Addressing modes : 11 • Data arrangement Instructions : Little endian Data : Selectable as little endian or big endian • On-chip 32-bit multiplier : 32×32→64bits • On-chip divider: : 32/32→32bits • Barrel shifter : bits • Memory protection unit (MPU)
FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard

Table 2.2 Comparative Listing of CPU Registers

Register	Bit	RX62N	RX65N
EXTB	-	-	Exception Table Register
ACC		ACC : 64bits(DSP,multiply,multiply-and-accumulate)	ACC0 : 72bits(DSP,multiply,multiply-and-accumulate) ACC1 : 72bits(DSP)

2.2 Operating Modes

Table 2.3 shows a Comparative Listing of Operating Modes Specifications, and Table 2.4 shows a Comparative Listing of Operating Modes Registers.

Table 2.3 Comparative Listing of Operating Modes Specifications

Item	RX62N	RX65N
Mode Setting Pin	MD1,MD0 MD1 MD0 0 1 Boot mode 1 0 USB boot mode 1 1 Single-chip mode	MD,UB MD UB 0 0 Boot mode(SCI interface) 0 1 Boot mode(USBI interface) 0->1 0 Boot mode(FINE interface) 1 - Single-chip mode
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	-	Boot mode (FINE interface)
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.4 Comparative Listing of Operating Modes Registers

Register	Bit	RX62N	RX65N
MDMONR	MD0 MD	MD0 Status Flag	MD Pin Status Flag
	MD1	MD1 Status Flag (b1)	-
	MDE	MDE Status Flag (b7)	-
MDSR	-	Mode Status Register	-
SYSCR1	SBYRAME	-	Standby RAM Enable (b7)
		The Value after reset is different.	

2.3 Reset

Table 2.3Table 2.5shows a Comparative Listing of Reset Specifications and Table 2.6shows a Comparative Listing of Operating Modes Registers.

Table 2.5 Comparative Listing of Reset Specifications

Item	RX62N	RX65N
RES# pin reset	Voltage input to the RES# pin is driven low	Voltage input to the RES# pin is driven low
Power-on reset	Vcc rises or falls (voltage detection: VPOR)	VCC rises (voltage detection: VPOR)
Voltage-monitoring reset	- VCC falls (voltage detection: Vdet1) VCC falls (voltage detection: Vdet2)	VCC falls (voltage detection: Vdet0) VCC falls (voltage detection: Vdet1) VCC falls (voltage detection: Vdet2)
Deep software standby reset	Deep software standby mode is canceled by an interrupt	Deep software standby mode is canceled by an interrupt
Independent watchdog timer reset	The independent watchdog timer underflows	The independent watchdog timer underflows, or a refresh error occurs
Watchdog timer reset	The watchdog timer overflows	The watchdog timer underflows, or a refresh error occurs
Software reset	-	Register setting

Table 2.6 Comparative Listing of Reset Registers

Register	Bit	RX62N	RX65N
RSTSR * RSTSR0	LVD0RF	-	Voltage-Monitoring 0 Reset Detect Flag (b1)
	LVD1F LVD1RF	LVD1 Detection Flag (b1)	Voltage-Monitoring 1 Reset Detect Flag (b2)
	LVD2F LVD2RF	LVD2 Detection Flag (b2)	Voltage-Monitoring 2 Reset Detect Flag (b3)
RSTSR1	-	-	Reset Status Register 1
RSTSR2	-	-	Reset Status Register 2
SWRR	-	-	Software Reset Register
RSTCSR*	-	Reset Control/Status Register	-
IWDTSR*	REFEF	-	Refresh Error Flag (b15)

*In the User's Manual: Hardware of RX62N Group, RSTSR is described in section 9. Low Power Consumption.
In the User's Manual: Hardware of RX62N Group, RSTCSR is described in section 24. Watchdog Timer.
In the User's Manual: Hardware of RX62N Group, IWDTSR is described in section 25. Independent Watchdog Timer.

2.4 Voltage Detection Circuit

Table 2.7 shows a Comparative Listing of Voltage Detection Circuit Specifications, and Table 2.8 shows a Comparative Listing of Voltage Detection Circuit Registers.

Table 2.7 Comparative Listing of Voltage Detection Circuit Specifications

Item		RX62N(LVD)			RX65N(LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	-	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detected event	-	Less than Vdet1	Less than Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	-	Fix	Fix	Selectable from among three different levels by using OFS1.VDSEL[1:0] bits	Selectable from among three different levels by using LVDLVLR.LVD1LVL[3:0] bits	Selectable from among three different levels by using LVDLVLR.LVD2LVL[3:0] bits
	Monitoring flag	-	-	-	-	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			-	-		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Process upon voltage detection	**Reset**	**-** -	**Voltage monitoring 1 reset**	**Voltage monitoring 1 reset**	**Voltage monitoring 0 reset**	**Voltage monitoring 1 reset**	**Voltage monitoring 1 reset**
			Reset when Vdet1 > VCC CPU restart timing after specified time with VCC > Vdet1	Reset when Vdet2 > VCC CPU restart timing after specified time with VCC > Vdet2	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	No interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt		Non-maskable interrupt or maskable interrupt selectable	Non-maskable interrupt or maskable interrupt selectable

Item		RX62N(LVD)			RX65N(LVDA)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
			Interrupt request issued when Vdet1 > VCC	Interrupt request issued when Vdet2 > VCC		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enable/Disable switching	Digital filter function not available	Digital filter function not available	Digital filter function not available	Digital filter function not available	Available	Available
	Sampling time	Digital filter function not available	Digital filter function not available	Digital filter function not available	-	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)
Event linking		-	-	-	-	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.8 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX62N(LVD)	RX65N(LVDA)
RSTSR:* RSTSR0*	-	Reset Status Register	Reset Status Register 0
	LVD0RF	-	Voltage-Monitoring 0 Reset Detect Flag (b1)
	LVD1F LVD1RF	LVD1 Detection Flag (b1)	Voltage-Monitoring 1 Reset Detect Flag (b2)
	LVD2F LVD2RF	LVD2 Detection Flag (b2)	Voltage-Monitoring 2 Reset Detect Flag(b3)
LVDKEYR	-	Key Code Register for Low-Voltage Detection Control Register	-
LVDCR	-	Low-Voltage Detection Control Register	-
LVD1CR1	-	-	Voltage Monitoring 1 Circuit Control Register 1
LVD1SR	-	-	Voltage Monitoring 1 Circuit Status Register
LVD2CR1	-	-	Voltage Monitoring 2 Circuit Control Register 1
LVD2SR	-	-	Voltage Monitoring 2 Circuit Status Register
LVCMPCR	-	-	Voltage Monitoring Circuit Control Register
LVDLVLR	-	-	Voltage Detection Level Select Register
LVD1CR0	-	-	Voltage Monitoring 1 Circuit Control Register 0
LVD2CR0	-	-	Voltage Monitoring 2 Circuit Control Register 0

*In the User's Manual: Hardware of RX62N Group, RSTSR is described in section 9. Low Power Consumption.

In the User's Manual: Hardware of RX65N Group, RSTSR0 is described in section 6. Reset.

2.5 Clock Generation Circuit

Table 2.9 shows a Comparative Listing of Clock Generation Circuit Specifications, and Table 2.10 shows a Comparative Listing of Clock Generation Circuit Registers.

Table 2.9 Comparative Listing of Clock Generation Circuit Specifications

Item	RX62N	RX65N
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, DMACA, ETHERC,EDMAC, ROM, and RAM. • Generates the peripheral module clock (PCLK) to be supplied to peripheral modules. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to SDRAM • Generates the dedicated USB clock (UCLK) to be supplied to the USB • Generates the dedicated RTC clock (SUBCLK) to be supplied to the RTC • Generates the on-chip oscillator clock (IWDTCLK) to be supplied to the IWDT	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC,RSPI, SCIi, MTU3, and AES. • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD:unit 1) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX62N	RX65N
Operating frequency	• ICLK: 8 to 100 MHz • PCLK: 8 to 50 MHz • BCLK: 8 to 100 MHz*1 • BCLK pin output: 8 to 50 MHz*2 • SDCLK: 8 to 50 MHz • SDCLK pin output: 8 to 50 MHz • UCLK: 48 MHz (only when EXTAL = 12 MHz) • SUBCLK: 32.768 kHz • IWDTCLK: 125 kHz (Typ.)*1 Restrictions for setting clock frequencies: ICLK ≧ PCLK and ICLK ≧ BCLK	• ICLK: 120 MHz (max)*3 • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 60 MHz (max) • PCLKD: 60 MHz (max) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory) • BCLK: 120 MHz (max) • BCLK pin output: 60 MHz (max) • SDCLK pin output: 60 MHz (max) • UCLK: 48 MHz (max) • • CACCLK: Same as the clock from respective oscillators. • CANMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max)
Main clock oscillator	• Resonator frequency: 8MHz to 14MHz • External clock input frequency: 14MHz (max) • Connectable resonator or additional circuit:: crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU output can be forcedly driven to the high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to the high-impedance.
Sub-clock oscillator	• Resonator frequency:32.768kHz • External Clock input : 32.768kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT

Item	RX62N	RX65N
PLL frequency synthesizer	• Input clock source: Main clock, Internal Oscillator • Input frequency: 4MHz to 14MHz • Frequency multiplication ratio: 8 遙倍	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	-	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	-	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency:125kHz	Oscillation frequency: 120kHz
JTAG external clock input (TCK)	-	Input clock frequency:10MHz (max)
Control of output on the BCLK pin	• BCLK clock output or high-level output is selectable • BCLK or BCLK/2 is selectable (When EXTAL 1 is selected for BCLK, BCLK/2 cannot be selected.)	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Control of output on the SDCLK pin	SDCLK output or a constant high-level output is selectable	SDCLK clock output or high output is selectable
Event linking (output)	-	Detection of stopping of the main clock oscillator
Event linking (input)	-	Switching of the clock source to the low-speed on-chip oscillator

*1. For products in the 100-pin LQFP and 85-pin TFLGA, the frequency of BCLK is from 8 to 50 MHz
*2. For products in the 100-pin LQFP and 85-pin TFLGA, output on the BCLK pin is at 8 to 25 MHz

Table 2.10 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX62N	RX65N
SCKCR	PCKD[3:0]	-	Peripheral Module Clock D (PCLKD) Select*1 (b3-b0)
	PCKC[3:0]	-	Peripheral Module Clock C (PCLKC) Select (b7-b4)
	PCK[3:0] PCKB[3:0]	Peripheral Module Clock Select b11 b8 0 0 0 0 : ×8 0 0 0 1 : ×4 0 0 1 0 : ×2 0 0 1 1 : ×1 Settings other than those listed above are prohibited	Peripheral Module Clock B (PCLKB) Select b11 b8 0 0 0 0 : x1/1 0 0 0 1 : x1/2 0 0 1 0 : x1/4 0 0 1 1 : x1/8 0 1 0 0 : x1/16 0 1 0 1 : x1/32 0 1 1 0 : x1/64 Settings other than above are prohibited
		The Value after reset is different.	
	PCKA[3:0]	-	Peripheral Module Clock A (PCLKA) Select (b15-b12)
	BCK[3:0]	External Bus Clock and SDRAM Clock Select b19 b16 0 0 0 0 : ×8 0 0 0 1 : ×4 0 0 1 0 : ×2 0 0 1 1 : ×1 Settings other than those listed above are prohibited	External Bus Clock (BCLK) Select b19 b16 0 0 0 0 : x1/1 0 0 0 1 : x1/2 0 0 1 0 : x1/4 0 0 1 1 : x1/8 0 1 0 0 : x1/16 0 1 0 1 : x1/32 0 1 1 0 : x1/64 Settings other than above are prohibited
		The Value after reset is different.	
	ICK[3:0]	System Clock Select b27 b24 0 0 0 0 : ×8 0 0 0 1 : ×4 0 0 1 0 : ×2 0 0 1 1 : ×1 Settings other than those listed above are prohibited	System Clock (ICLK) Select b27 b24 0 0 0 0 : x1/1 0 0 0 1 : x1/2 0 0 1 0 : x1/4 0 0 1 1 : x1/8 0 1 0 0 : x1/16 0 1 0 1 : x1/32 0 1 1 0 : x1/64 Settings other than above are prohibited
		The Value after reset is different.	
	FCK[3:0]	-	Flash-IF Clock (FCLK) Select (b31-b28)

Register	Bit	RX62N	RX65N
ROMWT	-	-	ROM Wait Cycle Setting Register
SCKCR2	-	-	System Clock Control Register 2
SCKCR3	-	-	System Clock Control Register 3
PLLCR	-	-	PLL Control Register
PLLCR2	-	-	PLL Control Register 2
MOSCCR	-	-	Main Clock Oscillator Control Register
SUBOSCCR: SOSCCR	-	Sub-Clock Oscillator Control Register	Sub-Clock Oscillator Control Register
	SUBSTOP SOSTP	Sub-Clock Oscillator Control	Sub-Clock Oscillator Stop
LOCOCR	-	-	Low-Speed On-Chip Oscillator Control Register
ILOCOCR	-	-	IWDT-Dedicated On-Chip Oscillator Control Register
HOCOCR	-	-	High-Speed On-Chip Oscillator Control Register
HOCOCR2	-	-	High-Speed On-Chip Oscillator Control Register 2
OSCOVFSR	-	-	Oscillation Stabilization Flag Register
OSTDCR RX62N:16bits RX65N:8bits	OSTDIE	-	Oscillation Stabilization Flag Register (b0)
	OSTDF	Oscillation Stop Detection Flag (b6)	-
	OSTDE	Oscillation Stop Detection Function Enable (b7)	Oscillation Stop Detection Function Enable (b7)
		The Value after reset is different.	
	KEY[7:0]	OSTDCR Key Code (b15-b8)	-
OSTDSR	-	-	Oscillation Stop Detection Status Register
MOSCWTCR	-	-	Main Clock Oscillator Wait Control Register
SOSCWTCR	-	-	Sub-Clock Oscillator Wait Control Register
MOFCR	-	-	Main Clock Oscillator Forced Oscillation Control Register
HOCOPCR	-	-	High-Speed On-Chip Oscillator Power Supply Control Register

Note 1. The setting for division by one is prohibited if the frequency of the clock signal from the PLL circuit is higher than 120 MHz while the SCKCR3.CKSEL[2:0] bits are selecting the PLL.

2.6 Low Power Consumption

Table 2.11 shows a Comparative Listing of Low Power Consumption Specifications, and Table 2.12 shows a Comparative Listing of Low Power Consumption Registers.

Table 2.11 Comparative Listing of Low Power Consumption Specifications

Item	RX62N	RX65N
Reducing power consumption by switching clock signals	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLK), and external bus clock (BCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected	BCLK output or high-level output can be selected
SDCLK output control function	SDCLK output or high-level output can be selected	SDCLK output or high-level output can be selected
Module-stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	Transition to low power consumption mode is enabled to stop the CPU, peripheral modules, and oscillator.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled..
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	-	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range. • Three operating power control modes High-speed operating mode Low-speed operating mode 1 Low-speed operating mode 2 There is no difference in power consumption when the same conditions (frequency and voltage) are set in low-speed operating modes 1 and 2.

Table 2.12 Comparative Listing of Low Power Consumption Registers

Register	Bit	RX62N	RX65N
SBYCR	STS[4:0]	Standby Timer Select (b12-b8) b12 b8 0 0 1 0 1 : Waiting time = 64 states 0 0 1 1 0 : Waiting time = 512 states 0 0 1 1 1 : Waiting time = 1024 states 0 1 0 0 0 : Waiting time = 2048 states 0 1 0 0 1 : Waiting time = 4096 states 0 1 0 1 0 : Waiting time = 16384 states 0 1 0 1 1 : Waiting time = 32768 states 0 1 1 0 0 : Waiting time = 65536 states 0 1 1 0 1 : Waiting time = 131072 states 0 1 1 1 0 : Waiting time = 262144 states 0 1 1 1 1 : Waiting time = 524288 states Settings other than above are prohibited.	-
		The Value after reset is different.	
MSTPCRA	MSTPA0	-	Compare Match Timer W (Unit 1) Module Stop (b0)
	MSTPA1	-	Compare Match Timer W (Unit 0) Module Stop (b1)
	MSTPA8	Multifunction Timer Pulse Unit (Unit 1) Module Stop (b8) Target module: MTU unit 1 (MTU6 to MTU11)	-
	MSTPA9	Multifunction Timer Pulse Unit (Unit 0) Module Stop Target module: MTU unit 0 (MTU0 to MTU5)	Multifunction Timer Pulse Unit 3 Module Stop Target module: MTU3
	MSTPA13	-	16-Bit Timer Pulse Unit 0 (Unit 0) Module Stop(b13) Target module: TPU unit 0 (TPU0 to TPU5)
	MSTPA16	-	12-bit A/D Converter (Unit 1) Module Stop(b16) Target module: S12AD unit 1
	MSTPA17	12-bit A/D Converter Module Stop *1 Target module: S12AD	12-bit A/D Converter (Unit 0) Module Stop Target module: S12AD unit 0
	MSTPA19	D/A Converter Module Stop Target module: DA	12-bit D/A Converter Module Stop Target module: 12-bit D/A
	MSTPA22	10-bit A/D Converter (Unit 1) Module Stop*1 (b22)	-

Register	Bit	RX62N	RX65N
	MSTPA23	10-bit A/D Converter (Unit 0) Module Stop*1 (b23)	-
	MSTPA24	-	Module Stop A24(b24)
		The Value after reset is different.	
	MSTPA27	-	Module Stop A27 (b27)
MSTPCRB	MSTPB0	CAN Module Stop Target module: CAN	CAN Module 0 Module Stop*2 Target module: CAN0
	MSTPB1	-	CAN Module1 Module Stop*2 (b1)
	MSTPB4	-	Serial Communication Interface SCIh(SCI12) Module Stop (b4)
	MSTPB6	-	Data Operation Circuit Module Stop(b6)
	MSTPB8	-	Temperature Sensor Module Stop (b8)
	MSTPB9	-	Event Link Controller Module Stop (b9)
	MSTPB15	Ethernet Controller DMAC Module Stop Target module: EDMAC	Ethernet Controller and Ethernet Controller DMA Controller (Channel 0) Modules Stop Target modules: ETHER and EDMAC (channel 0)
	MSTPB18	Universal Serial Bus Interface (Port 1) Module Stop (b18)	-
	MSTPB19	Universal Serial Bus Interface (Port 0) Module Stop Target module: USB0	Universal Serial Bus 2.0 FS Interface Module Stop Target module: USB0
	MSTPB20	I^2C Bus Interface 1 Module Stop (b20)	-
	MSTPB22	-	Parallel Data Capture Unit Module Stop (b22)
	MSTPB24	-	Serial Communication Interface 7 Module Stop (b24)
	MSTPB27	-	Serial Communication Interface 4 Module Stop (b27)
MSTPCRC	MSTPC1	RAM1 Module Stop (b1)	-
	MSTPC7	-	Standby RAM Module Stop (b7)
	MSTPC17	-	I^2C Bus Interface 2 Module Stop (b17)
	MSTPC19	-	CAC Module Stop (b19)
	MSTPC22	-	Serial Peripheral Interface 2 Module Stop (b22)
	MSTPC23	-	Quad Serial Peripheral Interface Module Stop (b23)
	MSTPC24	-	Serial Communications Interface 11 Module Stop (b24)
	MSTPC25	-	Serial Communications Interface 10 Module Stop (b25)
	MSTPC26	-	Serial Communications Interface 9 Module Stop (b26)

Register	Bit	RX62N	RX65N
	MSTPC27	-	Serial Communications Interface 8 Module Stop (b27)
MSTPCRD	-	-	Module Stop Control Register D
OPCCR	-	-	Operating Power Control Register
RSTCKCR	-	-	Sleep Mode Return Clock Source Switching Register
DPSBYCR	RAMCUT0 DEEPCUT[1:0]	On-Chip RAM Off 0 (b5,b4,b0) b5 b4 b0 0 0 0 : Power is supplied to the on-chip RAM (RAM0*) and USB resume detecting unit in deep software standby mode 1 1 1 : Power is not supplied to the on-chip RAM (RAM0*) and USB resume detecting unit in deep software standby mode Settings other than above are prohibited.	Deep Cut (b1-b0) b1 b0 0 0 : Power is supplied to the standby RAM and USB resume detecting unit in deep software standby mode 0 1 : Power is not supplied to the standby RAM and USB resume detecting unit in deep software standby mode 1 0 : Setting prohibited 1 1 : Power is not supplied to the standby RAM and USB resume detecting unit in deep software standby mode. In addition, LVD is stopped and the low power consumption function in a power-on reset circuit is enabled.
DPSBYCR	RAMCUT1	On-Chip RAM Off 1 Refer the RAMCUT0 function(b4)	-
		The Value after reset is different.	
	RAMCUT2	On-Chip RAM Off 2 Refer the RAMCUT0 function(b5)	-
		The Value after reset is different.	
DPSWCR	-	Deep Standby Wait Control Register	-
DPSIER DPSIER0	DLVDE DIRQ4E	LVD Deep Standby Cancel Signal Enable	IRQ4-DS Pin Enable
	DRTCE DIRQ5E	RTC Deep Standby Cancel Signal Enable	IRQ5-DS Pin Enable
	DUSBE DIRQ6E	USB Suspend/Resume Deep Standby Cancel Signal Enable	IRQ6-DS Pin Enable
	DNMIE DIRQ7E	NMI Pin Enable	IRQ7-DS Pin Enable
DPSIER1	-	-	Deep Standby Interrupt Enable Register 1
DPSIER2	-	-	Deep Standby Interrupt Enable Register 2

Register	Bit	RX62N	RX65N
DPSIER3	-	-	Deep Standby Interrupt Enable Register 3
DPSIFR DPSIFR0	DLVDF DIRQ4F	LVD Deep Standby Cancel Flag	IRQ4-DS Pin Deep Standby Release Flag
	DRTCF DIRQ5F	RTC Deep Standby Cancel Flag	IRQ5-DS Pin Deep Standby Release Flag
	DUSBF DIRQ6F	USB Suspend/Resume Deep Standby Cancel Flag	IRQ6-DS Pin Deep Standby Release Flag
	DNMIF DIRQ7F	NMI Deep Standby Cancel Flag	IRQ7-DS Pin Deep Standby Release Flag
DPSIFR1	-	-	Deep Standby Interrupt Flag Register 1
DPSIFR2	-	-	Deep Standby Interrupt Flag Register 2
DPSIFR3	-	-	Deep Standby Interrupt Flag Register 3
DPSIEGR DPSIEGR0	DIRQ4EG	-	IRQ4-DS Pin Edge Select (b4)
	DIRQ5EG	-	IRQ5-DS Pin Edge Select (b5)
	DIRQ6EG	-	IRQ6-DS Pin Edge Select (b6)
	DNMIEG DIRQ7EG	NMI Edge Select	IRQ7-DS Pin Edge Select
DPSIEGR1	-	-	Deep Standby Interrupt Edge Register 1
DPSIEGR2	-	-	Deep Standby Interrupt Edge Register 2
DPSIEGR3	-	-	Deep Standby Interrupt Edge Register 3
RSTSR RSTSR0*	LVD0RF	-	Voltage-Monitoring 0 Reset Detect Flag (b1)
	LVD1F LVD1RF	LVD1 Detection Flag(b1)	Voltage-Monitoring 1 Reset Detect Flag (b2)
	LVD2F LVD2RF	LVD2 Detection Flag(b2)	Voltage-Monitoring 2 Reset Detect Flag (b3)

Note 1. Simultaneously using a 10-bit A/D converter and the 12-bit A/D converter is not possible. Do not make the settings of the MSTPA17 and MSTPA22 bits or the MSTPA17 and MSTPA23 bits that release converters of both widths from the module-stop state at the same time.

Note2 while the oscillation of the clock controlled by the MSTPBi bit is stabilized. For entering software standby mode after writing a new value to the MSTPBi bit, wait for two cycles of the CAN clock (CANMCLK) to elapse after writing the new value, and then execute a WAIT instruction (i = 0, 1).

*In the User's Manual: Hardware of RX65N Group, RSTSR0 is described in section 6. Reset.

2.7 Exceptions

Table 2.13 shows a Comparative Listing of Exceptions Vector, and Table 2.14 shows a Comparative Listing of Return from Exception Handling Routine.

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Table 2.13 Comparative Listing of Exceptions Vector

Exception		RX62N	RX65N
Undefined instruction exception		Fixed vector table	Exception vector table(EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table(EXTB)
Access exceptions		Fixed vector table	Exception vector table(EXTB)
Floating-point exceptions		Fixed vector table	Exception vector table(EXTB)
Reset		Fixed vector table	Exception vector table(EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table(EXTB)
Interrupts	Fast interrupt	FINTV	FINTV
	Other than the above	Relocatable vector table(INTB)	Interrupt vector table(INTB)
Unconditional trap		Relocatable vector table(INTB)	Interrupt vector table(INTB)

Table 2.14 Comparative Listing of Return from Exception Handling Routine

Exception		RX62N	RX65N
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exceptions		RTE	RTE
Floating-point exceptions		RTE	RTE
Reset		Return is impossible	Return is impossible
Non-maskable interrupt		Return is impossible	Prohibited
Interrupts	Fast interrupt	RTFI	RTFI
	Other than the above	RTE	RTE
Unconditional trap		RTE	RTE

2.8 Interrupt Controller

Table 2.15 shows a Comparative Listing of Interrupt Controller Specifications, and Table 2.16 shows a Comparative Listing of Interrupt Controller Registers.

Table 2.15 Comparative Listing of Interrupt Controller Specifications

Item		RX62N(ICUa)	RX65N(ICUB)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is determined for each source of connected peripheral modules. • Number of sources: 146	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX62N(ICUa)	RX65N(ICUB)
Interrupts	External pin interrupts	• Interrupts from pins IRQ15 to IRQ0 • Number of sources: 16 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges • One of these detection methods can be set for each source.	• Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Number of sources: 16 • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.
	Software interrupt	• Interrupt generated by writing to a register • One interrupt source	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Interrupt priority	Specified by registers	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC/DMACA control	The DTC and DMACA can be activated by interrupt sources. Number of DTC activating sources: 102 (85 peripheral function interrupts + 16 external pin interrupts + 1 software interrupt) Number of DMACA activating sources: 45 (41 peripheral function interrupts + 4 external pin interrupts)	Interrupt sources can be used to start the DTC and DMAC
	EXDMAC control	-	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Nonmaskable interrupts	NMI pin interrupts	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge	• Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.

Item		RX62N(ICUa)	RX65N(ICUB)
	Oscillation stop detection interrupt	Interrupt during oscillation stop detection	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/refresh error interrupt	-	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	-	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring interrupt	Interrupt during power-voltage fall detection	Interrupt from voltage detection circuit 1 (LVD1) Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	-	This interrupt occurs when a parity check error is detected in the RAM.
Return from power-down modes	Sleep mode	Return is initiated by non-maskable interrupts or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Return is initiated by non-maskable interrupts, IRQ15 to IRQ0 interrupts, WDT interrupts, TMR interrupts, USB interrupts (USBR), or RTC alarm interrupts.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).
	Software standby mode	Return is initiated by non-maskable interrupts, IRQ15 to IRQ0 interrupts, USB interrupts (USBR), or RTC alarm interrupts.	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	-	Exit all-module clock stop mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.16 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX62N(ICUa)	RX65N(ICUB)
IRi IRn	-	Interrupt Request Register i (i = interrupt vector number)	Interrupt Request Register n (n = 016 to 255)
IPRm IPRr	-	Interrupt Priority Register m (m=0 to 8Fh)	Interrupt Priority Register r (r=0 to 255)
SWINT2R	-	-	Software Interrupt 2 Generation Register
DTCERn	-	DTC Activation Enable Register n (n = interrupt vector number)	DTC Transfer Request Enable Register n (n=026 to 255)
DMRSRn DMRSRm	-	DMACA Activation Source Select Register n (n = DMACA channel number)	DMAC trigger Select Register m (m = DMAC channel number)
	DMRS[7:0] -	DMACA Activation Request Select	None
IRQFLTE0	-	-	IRQ Pin Digital Filter Enable Register 0
IRQFLTE1	-	-	IRQ Pin Digital Filter Enable Register 1
IRQFLTC0	-	-	IRQ Pin Digital Filter Setting Register 0
IRQFLTC1	-	-	IRQ Pin Digital Filter Setting Register 1
NMISR	LVDST	Voltage Monitoring Interrupt Status Flag (b1)	-
	OSTST	Oscillation Stop Detection Interrupt Status Flag (b2)	Oscillation Stop Detection Interrupt Status Flag (b1)
	WDTST	-	WDT Underflow/Refresh Error Status Flag (b2)
	IWDTST	-	IWDT Underflow/Refresh Error Status Flag (b3)
	LVD1ST	-	Voltage Monitoring 1 Interrupt Status Flag (b4)
	LVD2ST	-	Voltage Monitoring 2 Interrupt Status Flag (b5)
	RAMST	-	RAM Error Interrupt Status Flag (b6)
NMIER	LVDEN	Voltage Monitoring Interrupt Enable (b1)	-
	OSTEN	Oscillation Stop Detection Interrupt Enable (b2)	Oscillation Stop Detection Interrupt Enable (b1)
	WDTEN	-	WDT Underflow/Refresh Error Enable (b2)
	IWDTEN	-	IWDT Underflow/Refresh Error Enable (b3)
	LVD1EN	-	Voltage Monitoring 1 Interrupt Enable (b4)
	LVD2EN	-	Voltage Monitoring 2 Interrupt Enable (b5)
	RAMEN	-	RAM Error Interrupt Enable (b6)
NMICLR	-	Non-Maskable Interrupt Clear Register	Non-Maskable Interrupt Status Clear Register

Register	Bit	RX62N(ICUa)	RX65N(ICUB)
	OSTCLR	OST Clear (b2)	OST Clear (b1)
	WDTCLR	-	WDT Clear (b2)
	IWDTCLR	-	IWDT Clear (b3)
	LVD1CLR	-	LVD1 Clear (b4)
	LVD2CLR	-	LVD2 Clear (b5)
NMIFLTE	-	-	NMI Pin Digital Filter Enable Register
NMIFLTC	-	-	NMI Pin Digital Filter Setting Register
GRPBE0	-	-	Group BE0 Interrupt Request Register
GRPBL0/1/2	-	-	Group BL0/BL1/BL2 Interrupt Request Register
GRPAL0/1	-	-	Group AL0/AL1 Interrupt Request Register
GENBE0	-	-	Group BE0 Interrupt Request Enable Register
GENBL0/1/2	-	-	Group BL0/BL1/BL2 Interrupt Request Enable Register
GENAL0/1	-	-	Group AL0/AL1 Interrupt Request Enable Register
GCRBE0	-	-	Group BE0 Interrupt Clear Register
PIBRk	-	-	Software Configurable Interrupt B Request Register k (k=0h to Ah)
PIARk	-	-	Software Configurable Interrupt A Request Register k (k=0h to 5h,Bh)
SLIBXRn	-	-	Software Configurable Interrupt B Source Select Register Xn (n=128 to 143)
SLIBRn	-	-	Software Configurable Interrupt B Source Select Register n (n=144 to 207)
SLIARn	-	-	Software Configurable Interrupt A Source Select Register n (n=208 to 255)
SELEXDR	-	-	EXDMAC Trigger Select Register
SLIPRCR	-	-	Software Configurable Interrupt Source Select Register Write Protect Register

2.9 Buses

Table 2.17 shows a Comparative Listing of Bus Specifications, Table 2.18 shows a Comparative Listing of External Bus Specifications, and Table 2.19 shows a Comparative Listing of Bus Registers.

Table 2.17 Comparative Listing of Bus Specifications

Bus Type		RX62N	RX65N
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to on-chip RAM	Connected to on-chip RAM
	Memory bus 2	Connected to on-chip ROM	Connected to code flash memory
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMACA, DTC, and EDMAC • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, EDMAC, and SDSI • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules, on-chip ROM (for programming and erasure), and data-flash memory • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)

Bus Type		RX62N	RX65N
	Internal peripheral bus 3	• Connected to peripheral modules (USB) • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC and ETHERC) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	• Connected to peripheral modules • Operates in synchronization with the system clock (ICLK)	Reserved area
	Internal peripheral bus 6	• Connected to on-chip ROM (for programming and erasure) and data-flash memory • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to code flash (in P/E) • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to the SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to the SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

Table 2.18 Comparative Listing of External Bus Specifications

Item	RX62N	RX65N
External address space	• An external address space is divided into eight areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • An 8/16/32-bit bus space is selectable for each area. • An endian mode can be specified for each area.	• An external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. Separate bus: An 8 or 16-bit bus space is selectable. Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each are
CS area controller	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. Timing of assertion and negation for chip-select signals (CS0# to CS7#) The timing of assertion of the read signal (RD#) and write signals (WR#, WR0# to WR3#) The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following. Timing of assertion and negation for chip-select signals (CS0# to CS7#) The timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR1#) The timing with which data output starts and ends • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
SDRAM area controller	• Multiplexing output of row address/column address (8, 9, 10, or 11 bits) • Self-refresh and auto-Refresh selectable • CAS latency can be specified from one to three cycles	• Multiplexing output of row address/column address (8, 9, 10, or 11 bits) • Self-refresh and auto-Refresh selectable • CAS latency can be specified from one to three cycles
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed	When write data from the bus master has been written to the write buffer, write access by the bus master is completed
Frequency	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK)*. • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).* • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).

Note: * The BCLK and the SDCLK should be operated with the same frequency when the SDRAM is in use.

Table 2.19 Comparative Listing of Bus Registers

Register	Bit	RX62N	RX65N
CSnCR	BSIZE[1:0]	External Bus Width Select b5 b4 0 0: A 16-bit bus space is selected*3 0 1: A 32-bit bus space is selected*4 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	External Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited 1 0: An 8-bit bus space is selected 1 1: Setting prohibited
	MPXEN	-	Address/Data Multiplexed I/O Interface Select (b12)
CSRECEN	-	-	CS Recovery Cycle Insertion Enable Register
CSnWCR2	AWAIT[1:0]	-	Address Cycle Wait Select (b13-b12)
SDCCR	BSIZE[1:0]	SDRAM Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: A 32-bit bus space is selected 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	SDRAM Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited 1 0: An 8-bit bus space is selected 1 1: Setting prohibited
BERSR1	MST[2:0]	Bus Master Code b6 b4 0 0 0: CPU 0 0 1: Setting prohibited 0 1 0: Setting prohibited 0 1 1: DTC/DMACA 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: EDMAC 1 1 1: EXDMAC	Bus Master Code b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: EDMAC/SDSI 1 1 1: EXDMAC
BUSPRI	-	-	Bus Priority Control Register

2.10 Memory-Protection Unit

Table 2.20 shows a Comparative Listing of Memory-Protection Unit Registers.

Table 2.20 Comparative Listing of Memory-Protection Unit Registers

Register	Bit	RX62N(MPU)	RX65N(MPU)
MPESTS	IA IMPER	Instruction Memory-Protection Error Generated Bit	Instruction Memory-Protection Error Generation
	DA: DMPER	Data Memory-Protection Error Generated Bit	Data Memory-Protection Error Generation

2.11 DMA Controller

Table 2.21 shows a Comparative Listing of DMA Controller Specifications, and Table 2.22 shows a Comparative Listing of DMA Controller Registers.

Table 2.21 Comparative Listing of DMA Controller Specifications

Item		RX62N(DMACA)	RX65N(DMACAa)
Number of channels		4(DMACm (m = 0 to 3))	8(DMACm(m = 0 to 7))
Transfer space		512Mbytes (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh excluding reserved areas)	512Mbytes (0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas)
Maximum transfer volume		1023Kdata (Maximum number of transfers in block transfer mode: 1023 data × 1024 blocks)	64Mdata (Maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMA request source		Activation source selectable for each channel Software trigger Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel Software trigger Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: Highest)	Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: Highest
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1023	Number of data: 1 to 1024
Transfer mode	Normal transfer mode	One data transfer by one DMA transfer request Free running mode (setting in which total number of data transfers is not specified) settable	One data transfer by one DMA transfer request Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	One data transfer by one DMA transfer request Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. Maximum settable repeat size: 1024	One data transfer by one DMA transfer request Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. Maximum settable repeat size: 1024
	Block transfer mode	One block data transfer by one DMA request Maximum settable block size: 1023 data	One block data transfer by one DMA request Maximum settable block size: 1024 data

Item		RX62N(DMACA)	RX65N(DMACAa)
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of two bytes to 128 Mbytes separately	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed Area of two bytes to 128 Mbytes separately
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter	Generated on completion of transferring data volume specified by the transfer counter
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows	Generated when the repeat size of data transfer is completed or the extended repeat area overflows
Event link function		-	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Power consumption reduction function		Module-stop state can be set.	Module-stop state can be set.

Table 2.22 Comparative Listing of DMA Controller Registers

Register	Bit	RX62N(MPU)	RX65N(MPU)
DMCRA	DMCRAL	Lower bits of transfer count Block Transfer Mode(DMTMD.MD[1:0] = 10b) The number of transfers is one when the setting is 001h and 1023 when it is 3FFh. In block transfer mode, a value in the range of 001h to 3FFh can be set for DMCRAH and DMCRAL. Setting a value of 000h is prohibit	Lower bits of transfer count Block Transfer Mode(DMTMD.MD[1:0] = 10b) The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In block transfer mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.
	DMCRAH	Upper bits of transfer count Block Transfer Mode(DMTMD.MD[1:0] = 10b) The number of transfers is one when the setting is 001h and 1023 when it is 3FFh. In block transfer mode, a value in the range of 001h to 3FFh can be set for DMCRAH and DMCRAL. Setting a value of 000h is prohibit	Upper bits of transfer count Block Transfer Mode(DMTMD.MD[1:0] = 10b) The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In block transfer mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.
DMCRB	-	Specifies the number of block transfer operations or repeat transfer operations (b9-b0) In normal transfer mode, a value of 3FFh should be set.	Specifies the number of block transfer operations or repeat transfer operations. (b15-b0) In normal transfer mode, DMCRB is not used. The setting is invalid.
DMINT	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable	Source Address Extended Repeat Area Overflow Interrupt Enable When setting 1 in the DTE bit in DMACm.DMCNT of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped
DMIST	-	-	DMAC74 Interrupt Status Monitor Register

2.12 EXDMA Controller

Table 2.23 shows a Comparative Listing of EXDMA Controller Specifications ,and Table 2.24 shows a Comparative Listing of EXDMA Controller Registers.

Table 2.23 Comparative Listing of EXDMA Controller Specifications

Item		RX62N(EXDMAC)	RX65N(EXDMACa)
Number of channels		2 (EXDMACn (n = 0, 1))	2 (EXDMAC0 and EXDMAC1)
Transfer space		512 Mbytes (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh excluding reserved areas)	512 Mbytes (External areas at addresses 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas)
Maximum transfer volume		1M data (Maximum number of transfer operations in block transfer mode: 1023 data × 1024 blocks)	1 M data (Maximum number of transfer operations in block transfer mode: 1,024 data × 1,024 blocks)
DMA request source		• Activation source selectable from the following three sources for each channel Software trigger Pins for external DMA transfer requests DMA transfer request from peripheral modules (compare match of MTU1)	• Request source selectable from the following three sources for each channel Software trigger External DMA transfer request input DMA transfer request from peripheral modules (TPU1.TRGA or MTU1.TRGA) (Channel 0: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR144 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR208; Channel 1: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR145 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR209)
Channel priority		Channel 0 > Channel 1(Channel 0: Highest)	Channel 0 > Channel 1(Channel 0: Highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1023 data	Number of data: 1 to 1,024 data
	Cluster size	Number of data: 1 to 7 data	Number of data: 1 to 8 data

Item		RX62N(EXDMAC)	RX65N(EXDMACa)
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfer operations is not specified) settable	• One data transfer by one DMA transfer request • Free running mode (setting in which total number of data transfer operations is not specified) settable
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1023 data	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data
	Block transfer mode	• One block data transfer by one DMA request • Maximum settable block size: 1023 data	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data
	Cluster transfer mode	• One cluster data transfer by one DMA request • Maximum settable cluster size: 7 data (28 bytes)	• One cluster data transfer by one DMA transfer request • Maximum settable cluster size: 8 data (32 bytes)
Address mode	Single address mode	• Transfers data by accessing the transfer source or destination peripheral device with the • EDACKn signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.	• Transfers data by accessing the transfer source or destination peripheral device with the • EDACKn signal (n = 0, 1) and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.
	Dual address mode	• Transfers data by specifying the addresses of transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.	• Transfers data by specifying the addresses of transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the • specified range with the upper bit values in the transfer address register fixed • Area of two bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination	• Function in which data can be transferred by repeating the address values in the specified • range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination

Item		RX62N(EXDMAC)	RX65N(EXDMACa)
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Low-power consumption function		The module-stop state can be set.	The module-stop state can be set.

Table 2.24 Comparative Listing of EXDMA Controller Registers

Register	Bit	RX62N(EXDMA)	RX65N(EXDMAa)
EDMCRA	-	EXDMA Transfer Count Register Repeat transfer mode MD[1:0] bits in EXDMACn.EDMTMD = 01b The number of transfer operations is one when the setting is 001h and 1023 when it is 3FFh. In repeat transfer mode, a value in the range of 001h to 3FFh can be set for EDMCRAH and EDMCRAL. Setting a value of 000h is prohibited. Block transfer mode MD[1:0] bits in EXDMACn.EDMTMD = 10b The number of transfers is one when the setting is 001h and 1023 when it is 3FFh. In block transfer mode, a value in the range of 001h to 3FFh can be set for EDMCRAH and EDMCRAL. Setting a value of 000h is prohibited. Cluster transfer mode MD[1:0] bits in EXDMACn.EDMTMD = 11b) The number of transfers is one when the setting is 001h and seven when it is 007h. In cluster transfer mode, a value in the range of 001h to 007h can be set for EDMCRAH and EDMCRAL. Setting a value of 000h is prohibited.	EXDMA Transfer Count Register Repeat transfer mode EXDMACn.EDMTMD.MD[1:0] bits = 01b) The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In repeat transfer mode, a value in the range of 000h to 3FFh (the number of transfer operations: 1 to 1024) can be set for EDMCRAH and EDMCRAL. Block transfer mode EXDMACn.EDMTMD.MD[1:0] bits = 10b The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In block transfer mode, a value in the range of 000h to 3FFh (the number of transfer operations: 1 to 1024) can be set for EDMCRAH and EDMCRAL. Cluster transfer mode EXDMACn.EDMTMD.MD[1:0] bits = 11b The number of transfer operations is one when the setting is 001h, seven when it is 007h, and eight when it is 000h. In cluster transfer mode, a value in the range of 000h to 007h (the number of transfer operations: 1 to 8) can be set for EDMCRAH and EDMCRAL.
EDMCRB	-	EXDMA Block Transfer Count Register In normal transfer mode, a value of 3FFh should be set.	EXDMA Block Transfer Count Register In normal transfer mode, EDMCRB is not used and setting this register is invalid.

EDMTMD	DCTG[1:0]	DMA Request Source Select b1 b0 0 0: Software 0 1: Setting prohibited 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from the on-chip peripheral modules (compare match of MTU1)	Transfer Request Source Select b1 b0 0 0: Software 0 1: Setting prohibited 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer request from peripheral modules (TPU1.TRGA or MTU1.TRGA)
EDMOMD	DACKSEL	-	EDACKn Pin Toggling Select (b0)
CLSBRi CLSBRy		Cluster Buffer Register i (i = 0 to 6)	Cluster Buffer Register y (y = 0 to 7)

2.13 Data Transfer Controller

Table 2.25 shows a Comparative Listing of Data Transfer Controller Specifications, and Table 2.26 shows a Comparative Listing of Data Transfer Controller Registers.

Table 2.25 Comparative Listing of Data Transfer Controller Specifications

Item	RX62N(DTCa)	RX65N(DTCb)
Number of transfer channels	The same number as all interrupt sources that can start the DTC transfer.	The same number as all interrupt sources that can start the DTC transfer.
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address is returned to the transfer start address after the number of data transfers corresponding to "repeat size". The maximum repeat size is 256 data. • Block transfer mode A single activation leads to the transfer of a single block. The maximum block size is 255 data.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode A single transfer request leads to a single data transfer. The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes. • Block transfer mode A single transfer request leads to the transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh excepting reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh excepting reserved areas)	• In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Length of a single data: 8, 16, or 32 bits • Number of data for a single block: 1 to 255 data	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data

Item	RX62N(DTCa)	RX65N(DTCb)
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Event link function	-	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Transfer data read skip can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When "fixed" is selected for transfer source address and/or transfer destination address, write-back skip execution is provided.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	-	Allows disabling the write-back of transfer information.
Sequence transfer	-	A series of complicated transfers can be registered as a sequence. . • Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).
Displacement addition	-	The displacement value can be added to the transfer source address (for each transfer information)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.26 Comparative Listing of Data Transfer Controller Registers

Register	Bit	RX62N(DTCa)	RX65N(DTCb)
MRA	WBDIS	-	Write-back Disable (b0)
MRB	SQEND	-	Sequence Transfer End (b0)
	INDX	-	Index Table Reference (b1)
	CHNS	DTC Chain Transfer Select 0: Chain transfer is performed continuously 1: Chain transfer is performed only when the transfer counter is 0	DTC Chain Transfer Select 0: Chain transfer is performed on completion of each transfer. 1: Chain transfer is performed only when the transfer counter is changed from 1 to 0 or 1 to CRAH.
MRC	-	-	DTC Mode Register C
DTCVBR	-	DTC Vector Base Register The lower 12 bits (b11 to b0) are always 0 and cannot be modified. The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27.	DTC Vector Base Register Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 10 bits are reserved and the values are fixed to 0. Write 0 to the lower 10 bits if necessary. It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-Kbyte units.
CRA	CRAL	Transfer Counter A Lower Register Block transfer mode (MRA.MD[1:0] bits = “10b”) The transfer count is 1 and 255 when the set value is 01h and FFh, respectively. Setting a value of 00h is prohibited.	Transfer Counter A Lower Register Block transfer mode (MRA.MD[1:0] bits = “10b”) The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.
	CRAH	Transfer Counter A Upper Register Block transfer mode (MRA.MD[1:0] bits = “10b”) The transfer count is 1 and 255 when the set value is 01h and FFh, respectively. Setting a value of 00h is prohibited.	Transfer Counter A Upper Register Block transfer mode (MRA.MD[1:0] bits = “10b”) The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.
CRB	-	DTC Transfer Count Register B When normal transfer mode or repeat transfer mode is selected, set a value of FFFFh to the CRB.	DTC Transfer Count Register B When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.
DTCIBR	-	-	DTC Index Table Base Register
DTCOR	-	-	DTC Operation Register
DTCSQE	-	-	DTC Sequence Transfer Enable Register

Register	Bit	RX62N(DTCa)	RX65N(DTCb)
DTCDISP	-	-	DTC Address Displacement Register

2.14 I/O Ports

Table 2.27 shows a Comparative Listing of I/O Ports Specifications, and Table 2.28 shows a Comparative Listing of I/O Port Registers.

Note that the register comparison is described for the 145/144-pin packages.

Table 2.27 Comparative Listing of I/O Ports Specifications

Port Symbol	RX62N		RX65N	
	145pin,144pin	100pin	145 pin,144 pin	100 pin
PORT0	P00 to P03, P05, P07	P05, P07	P00 to P03, P05, P07	P05, P07
PORT1	P12 to P17	P12 to P14,P16	P12 to P17	P12 to P14,P15,P16,P17
PORT2	P20 to P27	P20 to P27	P20 to P27	P20 to P27
PORT3	P30 to P35	P30 to P35	P30 to P35,P36,P37	P30 toP35,P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P55	P50 to P56	P50 to P55
PORT6	P60 to P67	None	P60 to P67	None
PORT7	P70 to P77	None	P70 to P77	None
PORT8	P80 to P83,	None	P80 to P83, P86, P87	None
PORT9	P90 to P93	None	P90 to P93	None
PORTA	PA0 to PA7	PA0 to PA7	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7	PE0 to PE7	PE0 to PE7
PORTF	None	None	PF5	None
PORTG	None	None	None	None
PORTJ	None	None	PJ3, PJ5	PJ3
Total Ports	105	74	112	79

Table 2.28 Comparative Listing of I/O Port Registers

Register	Bit	RX62N	RX65N
DDR PDR	-	Data Direction Register Pnx I/O Select n=0 to 9,A to E x=0 to 7	Port Direction Register Pmx I/O Select m = 0 to 9, A to E,F, J x=0 to 7
DR PODR	-	Data Register Pnx Output Data Store n=0 to 9,A to E x=0 to 7	Port Output Data Register Pmx Output Data Store m = 0 to 9, A to E,F, J x=0 to 7
PORT PIDR	-	Port Register Pnx n=0 to 9,A to E x=0 to 7	Port Input Register Pmx m = 0 to 9, A to E,F, J x=0 to 7
ICR	-	Input Buffer Control Register	-

Register	Bit	RX62N	RX65N
ODR ODR0	-	Open Drain Control Register n=0 to 3,C	Open Drain Control Register 0 m=0 to 3,4 to 9,A,B,C,D,E,J
	Pn1 Output Type Select : Pm1 Output Type Select PE1 Output Type Select	Pn1 Output Type Select 0 : CMOS output pin 1 : NMOS open-drain output pin	For pins other than the port PE1 pin Odd Even bit bit X 0: CMOS output X 1: NMOS open-drain output (b1, b3, b5, b7: Reserved) For port PE1 pin b3 b2 0 0: CMOS output 0 1: NMOS open-drain output 1 0: PMOS open-drain output 1 1: Setting prohibited
ODR1	-		Open Drain Control Register 1
PMR	-	-	Port Mode Register
PCR	-	Pull-Up Resistor Control Register Pnx Input Pull-Up Resistor Control n=9,A to E	Pull-Up Resistor Control Register Pnx Input Pull-Up Resistor Control m = 0 to 8, 9, A to E, F, J
DSCR	-	-	Drive Capacity Control Register
DSCR2	-	-	Drive Capacity Control Register 2
PF0CSE PF1CSS PF2CSS PF3BUS PF4BUS PF5BUS PF6BUS PF7DMA PF8IRQ PF9IRQ PFAADC PFBTMR PFCMTU PFDMTU PFENET PFFSCI PFGSPI PFHSPI FJCAN PFKUSB PFMPOE PFNPOE	-	Port Function Control Register *	-

*:0 to 9,A to H,J,K,M,N

2.15 Programmable Pulse Generator

Table 2.29 shows a Comparative Listing of Programmable Pulse Generator Specifications, and Table 2.30 shows a Comparative Listing of Programmable Pulse Generator Registers.

Table 2.29 Comparative Listing of Programmable Pulse Generator Specifications

Item	RX62N(PPG)	RX65N(PPG)
Number of output bits	Up to 32 bits	Up to 32 bits (*1)
Pulse output	• Two units, each capable of output through four pin groups • Output trigger signals are selectable • Non-overlapping operation is possible • Inverted output is selectable	• Two units, each capable of output through four pin groups • Output trigger signals are selectable • Non-overlapping operation is possible • Inverted output is selectable
Output data transfer	Can operate together with the DTC and DMACA (When MTU interrupt is in use)	Can operate together with the DTC and DMAC (when TPU and MTU3 interrupts are in use)
Power consumption reducing function	Module stop state can be set for each unit.	Module-stop state can be set for each unit.

*1: When setting PPG output trigger in MTU3, make settings so that PCLKA run at the same frequency as PCLKB

Table 2.30 Comparative Listing of Programmable Pulse Generator Registers

Register	Bit	RX62N(PPG)	RX65N(PPG)
PTRSLR	PTRSL	PPG Trigger Select 0: Selects the set of MTU0 toMTU3 as the trigger channels for PPG1. 1: Selects the set of MTU6 to MTU9 as the trigger channels for PPG1.	PPG Trigger Select 0: Selects the set of MTU0 to MTU3 of MTU3 as the trigger channels for PPG1. 1: Selects the set of TPU0 to TPU3 of TPU as the trigger channels for PPG1.
PCR	G0CMS[1:0]	Group 4 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b1 b0 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b1 b0 0 0 : Compare match in MTU6 0 1 : Compare match in MTU7 1 0 : Compare match in MTU8 1 1 : Compare match in MTU9	Group 4 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b1 b0 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b1 b0 0 0 : Compare match in TPU0 0 1 : Compare match in TPU1 1 0 : Compare match in TPU2 1 1 : Compare match in TPU3

Register	Bit	RX62N(PPG)	RX65N(PPG)
PCR	G1CMS[1:0]	Group 5 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b3 b2 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b3 b2 0 0 : Compare match in MTU6 0 1 : Compare match in MTU7 1 0 : Compare match in MTU8 1 1 : Compare match in MTU9	Group 5 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b3 b2 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b3 b2 0 0 : Compare match in TPU0 0 1 : Compare match in TPU1 1 0 : Compare match in TPU2 1 1 : Compare match in TPU3
	G2CMS[1:0]	Group 6 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b5 b4 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b5 b4 0 0 : Compare match in MTU6 0 1 : Compare match in MTU7 1 0 : Compare match in MTU8 1 1 : Compare match in MTU9	Group 6 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b5 b4 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b5 b4 0 0 : Compare match in TPU0 0 1 : Compare match in TPU1 1 0 : Compare match in TPU2 1 1 : Compare match in TPU3

Register	Bit	RX62N(PPG)	RX65N(PPG)
	G3CMS[1:0]	Group 7 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b7 b6 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b7 b6 0 0 : Compare match in MTU6 0 1 : Compare match in MTU7 1 0 : Compare match in MTU8 1 1 : Compare match in MTU9	Group 7 Compare Match Select • When the PTRSL bit in PPG1.PTRSLR is set to 0 b7 b6 0 0 : Compare match in MTU0 0 1 : Compare match in MTU1 1 0 : Compare match in MTU2 1 1 : Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1 b7 b6 0 0 : Compare match in TPU0 0 1 : Compare match in TPU1 1 0 : Compare match in TPU2 1 1 : Compare match in TPU3
PMR	G0NOV	Group 4 Non-Overlap 0:Normal operation (Output values updated on compare match A in the selected MTUn) 1:Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3, 6 to 9)	Group 4 Non-Overlap When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)

Register	Bit	RX62N(PPG)	RX65N(PPG)
	G1NOV	Group 5 Non-Overlap 0:Normal operation (Output values updated on compare match A in the selected MTUn) 1:Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3, 6 to 9)	Group 5 Non-Overlap When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)
PMR	G2NOV	Group 6 Non-Overlap 0:Normal operation (Output values updated on compare match A in the selected MTUn) 1:Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3, 6 to 9)	Group 6 Non-Overlap When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)

Register	Bit	RX62N(PPG)	RX65N(PPG)
	G3NOV	Group 7 Non-Overlap 0:Normal operation (Output values updated on compare match A in the selected MTUn) 1:Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3, 6 to 9)	Group 7 Non-Overlap When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)

2.16 8-Bit Timer

Table 2.31 shows a Comparative Listing of 8-Bit Timer Specifications, and Table 2.32 shows a Comparative Listing of 8-Bit Timer Registers.

Table 2.31 Comparative Listing of 8-Bit Timer Specifications

Item	RX62N(TMR)	RX65N(TMR)
Count clock	• Internal clock:PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024,PCLK/8192 • External clock: external count clock
Number of channels	(8 bits x 2 channels) x 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external reset signal.	Selected by compare match A or B, or an external reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (Output)	-	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (Input)	-	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0 to TMR3) (2) Event counting operation (TMR0 to TMR3) (3) Counting restart operation (TMR0 to TMR3)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0 and TMR2	Compare match A of TMR0 and TMR2
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI5 and SCI6.	Generates baud rate clock for SCI5,SCI6 and SCI12
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

Table 2.32 Comparative Listing of 8-Bit Timer Registers

Register	Bit	RX62N(TMR)	RX65N(TMR)
TCSTR	-	-	Timer Counter Start Register

2.17 Compare Match Timer

Table 2.33 shows a Comparative Listing of Compare Match Timer Specifications, and Table 2.34 shows a Comparative Listing of Compare Match Timer Registers.

Table 2.33 Comparative Listing of Compare Match Timer Specifications

Item	RX62N(CMT)	RX65N(CMT)
Count clock	Four internal clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel	Four frequency dividing clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel	A compare match interrupt can be requested for each channel
Event link function(output)	-	An event signal is output upon a CMT1 compare match
Event link function(input)	-	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

Table 2.34 Comparative Listing of Compare Match Timer Registers

Register	Bit	RX62N(CMT)	RX65N(CMT)
CMCR	-	Compare Match Timer Control Register If data write to the CMCR register conflicts with the generation of a compare-match, data write to the CMCR register is ignored.. Notes on Data Write to the Compare-Match Timer Control Register (CMCR)	Compare Match Timer Control Register None
CMCNT	-	Compare Match Timer Counter Do not set the CMCNT counter and the CMCOR register to the same value while the CMCNT counter is halted Notes on the Compare-Match Timer Counter (CMCNT) and the Compare-Match Constant Register (CMCOR)	Compare Match Timer Counter None
CMCOR	-	Compare Match Timer Constant Register Do not set the CMCNT counter and the CMCOR register to the same value while the CMCNT counter is halted Notes on the Compare-Match Timer Counter (CMCNT) and the Compare-Match Constant Register (CMCOR)	Compare Match Timer Constant Register None

2.18 Realtime Clock

Table 2.35 shows a Comparative Listing of Realtime Clock Specifications, and Table 2.36 shows a Comparative Listing of Realtime Clock Registers.

Table 2.35 Comparative Listing of Realtime Clock Specifications

Item	RX62N(RTC)	RX65N(RTCd)
Count mode	Calendar count mode	Calendar count mode/binary count mode
Count source	32.768-kHz clock dedicated for the RTC	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, the date, day of the week, hours, minutes, and seconds are counted and represented in BCD — 30-second adjustment (30 seconds or less are rounded down to 00 second, and 30 seconds or more are rounded up to one minute) — Automatic leap year adjustment — Start/stop function — Indicates the state of 1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32Hz, and 64Hz in binary — Output a 1-Hz clock	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode — Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output

Item	RX62N(RTC)	RX65N(RTCd)
Interrupts	• Alarm interrupt (ALM) Year, month, the date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/16 second, 1/64 second or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64-Hz counter from the prescaler during reading of the 64-Hz counter • Recovery from software standby mode or deep software standby mode can be performed by an alarm Interrupt	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time capture function	-	• Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured.
Event link function	-	• Periodic event output

Table 2.36 Comparative Listing of Realtime Clock Registers

Register	Bit	RX62N(RTC)	RX65N(RTCd)
BCNT0*	-	-	Binary Counter 0
BCNT1*	-	-	Binary Counter 1
BCNT2*	-	-	Binary Counter 2
BCNT3*	-	-	Binary Counter 3
RSECCNT	SEC1[3:0]	Ones Place of Seconds	1-Second Count
	SEC10[2:0]	Tens Place of Seconds	10-Second Count
RMINCNT	MIN1[3:0]	Ones Place of Minutes	1-Minute Count
	MIN10[2:0]	Tens Place of Minutes	10-Minute Count
RHRCNT	HOUR1[3:0] HR1[3:0]	Ones Place of Hours	1-Hour Count
	HOUR10[1:0] HR10[1:0]	Tens Place of Hours	10-Hour Count
	PM	-	PM(b6)
RWKCNT	DAY[2:0] DAYW[2:0]	Day-of-Week Counting	Day-of-Week Counting
RDAYCNT	DAY1[3:0]: DATE1[3:0]	Ones Place of Days	1-Day Count
	DAY10[1:0]: DATE10[1:0]	Tens Place of Days	10-Day Count
RMONCNT	MON1[3:0]	Ones Place of Months	1-Month Count
	MON10	Tens Place of Months	10-Month Count
RYRCNT	YEAR1[3:0] YR1[3:0]	Ones Place of Years	1-Year Count
	YEAR10[3:0] YR10[3:0]	Tens Place of Years	10-Year Count
	YEAR100[3:0]	Hundreds Place of Years (b11-b8)	-
	YEAR1000[3:0]	Thousands Place of Years (b15-b12)	-
RHRAR	HOUR1[3:0] HR1[3:0]	1 Hour	1 Hour
	HOUR10[1:0] HR10[1:0]	10 Hour	10 Hour
	PM	-	PM(b6)
		The Value after reset is different.	
RWKAR	DAY[2:0] DAYW[2:0]	Day-of-Week Setting	Day-of-Week Setting
RDAYAR	DAY1[3:0] DATE1[3:0]	1 Day	1 Day
	DAY10[1:0] DATE10[1:0]	10 Day	10 Day
RYRAR	YEAR1[3:0] YR1[3:0]	1 Year	1 Year
	YEAR10[3:0] YR10[3:0]	10 Year	10 Year
	YEAR100[3:0]	100 Year (b11-b8)	-
	YEAR1000[3:0]	1000 Year (b15-b12)	-
BCNT0AR*	-	-	Binary Counter 0 Alarm Register
BCNT1AR*	-	-	Binary Counter 1 Alarm Register

Register	Bit	RX62N(RTC)	RX65N(RTCd)
BCNT2AR*	-	-	Binary Counter 2 Alarm Register
BCNT3AR*	-	-	Binary Counter 3 Alarm Register
BCNT0AER*	-	-	Binary Counter 0 Alarm Enable Register
BCNT1AER*	-	-	Binary Counter 1 Alarm Enable Register
BCNT2AER*	-	-	Binary Counter 2 Alarm Enable Register
BCNT3AER*	-	-	Binary Counter 3 Alarm Enable Register
RCR1	AIE	Alarm Interrupt Enable	Alarm Interrupt Enable
		The Value after reset is different.	
	PIE	Periodic Interrupt Enable	Periodic Interrupt Enable
		The Value after reset is different.	
	RTCOS	-	RTCOUT Output Select (b3)
	PES[2:0] PES[3:0]	Periodic Interrupt Select (b6-b4)	Periodic Interrupt Select (b7-b4)
RCR2	START	Start	Start
		The Value after reset is different.	
	ADJ ADJ30	30-Second Adjustment	30-Second Adjustment
	RTCOE	RTCOUT Output Control	RTCOUT Output Enable
	AADJE	-	Automatic Adjustment Enable (b4)
	AADJP	-	Automatic Adjustment Period Select (b5)
	HR24	-	Hours Mode (b6)
	CNTMD	-	Count Mode Select (b7)
RCR3	-	-	RTC Control Register3
RCR4	-	-	RTC Control Register 4
RFRH/L	-	-	Frequency Register H/L
RADJ	-	-	Time Error Adjustment Register
RTCCRy	-	-	Time Capture Control Register y
RSECCPy	-	-	Second Capture Register y
RMINCPy	-	-	Minute Capture Register y
RHRCPy	-	-	Hour Capture Register y
RDAYCPy	-	-	Date Capture Register y
RMONCPy	-	-	Month Capture Register y
BCNT0CPy*	-	-	BCNT0 Capture Register y (y = 0～2)
BCNT1CPy*	-	-	BCNT1 Capture Register y (y = 0～2)
BCNT2CPy*	-	-	BCNT2 Capture Register y (y = 0～2)
BCNT3CPy*	-	-	BCNT3 Capture Register y (y = 0～2)

* In the Binary Counter mode

2.19 Watchdog Timer

Table 2.37 shows a Comparative Listing of Watchdog Timer Specifications, and Table 2.38 shows a Comparative Listing of Watchdog Timer Registers.

Table 2.37 Comparative Listing of Watchdog Timer Specifications

Item	RX62N(WDT)	RX65N(WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, and PCLK/131072	Divide by 4, 64, 128, 512, 2048, or 8192
Number of channel	8bits x1channel	14bits x1channel
Counter operation	Counting up using a 8-bit up-counter	Counting down using a 14-bit down-counter
Counter clear	Write to TCNT	Write the refresh request to WDT refresh register (WDTRR).
Operation modes	Switchable between watchdog timer mode and interval timer mode	-
Watchdog timer mode	Outputs a WDTOVF# signal when the counter overflows. Selectable whether or not to internally reset the LSI at the same time.	-
Interval timer mode	Generates an interval timer interrupt (WOVI) when the counter overflows.	-
Conditions for starting the counter	• Write to the register(TCSR.TME='1')	• Auto-start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started by refresh operation (writing to the WDTRR register)
Conditions for stopping the counter	• When writing to the register (TCSR.TME='0'), the counter is initialized "00h".	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated
Window function	-	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Up-counter overflows	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	Interrupt Sources • Up-counter overflows	Non-maskable interrupt/interrupt Sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The up-counter value can be read by the TCNT register.	The down-counter value can be read by the WDTSR register.

Table 2.38 Comparative Listing of Watchdog Timer Registers

Register	Bit	RX62N(WDT)	RX65N(WDTA)
TCNT	-	Timer Counter	-
TCSR	-	Timer Control/Status Register	-
RSTCSR	-	Reset Control/Status Register	-
WINA	-	Write Window A Register	-
WINB	-	Write Window B Register	-
WDTRR	-	-	WDT Refresh Register
WDTCR	-	-	WDT Control Register
WDTSR	-	-	WDT Status Register
WDTRCR	-	-	WDT Reset Control Register
OFS0	-	-	Option Function Select Register 0

2.20 Independent Watchdog Timer

Table 2.39 shows a Comparative Listing of Independent Watchdog Timer Specifications, and Table 2.40 shows a Comparative Listing of Independent Watchdog Timer Registers.

Table 2.39 Comparative Listing of Independent Watchdog Timer Specifications

Item	RX62N(IWDT)	RX65N(IWDTa)
Count sources	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)*
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down by a 14-bit down-counter	Counting down by a 14-bit down-counter
Conditions for starting the counter	• Counting can be started by refreshing the down-counter (write FFh after 00h has been written to the IWDTRR register).	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Pin reset (the down-counter and other registers return to their initial values) • Generation of an underflow Counting restarts counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error occurs Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a no-nmaskable interrupt request/interrupt request is output. In register start mode, counting restarts after refreshing.)
Window function	-	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Underflow of the down-counter	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	-	Non-maskable interrupt/ interrupt sources • Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The value reached in counting by the down-counter can be read out from a register (the IWDTSR).	The down-counter value can be read by the IWDTSR register.
Event link function(Output)	-	• Down-counter underflow event output • Refresh error event output
Output signal(internal signal)	• Reset output	• Reset output • Interrupt request output • Sleep mode count stop control output

*)Satisfy the frequency of the peripheral module clock (PCLK) ≧ 4 × (the frequency of the count source after divide).

Table 2.40 Comparative Listing of Independent Watchdog Timer Registers

Register	Bit	RX62N(IWDT)	RX65N(IWDTa)
IWDTCR	CKS[3:0]	Clock Selection b7 b4 0 0 - -: IWDTCLK 0 1 0 0: IWDTCLK/16 0 1 0 1: IWDTCLK/32 0 1 1 0: IWDTCLK/64 0 1 1 1: IWDTCLK/128 1 - - -: IWDTCLK/256	Clock Divide Ratio Select b7 b4 0 0 0 0: No division 0 0 1 0: Divide-by-16 0 0 1 1: Divide-by-32 0 1 0 0: Divide-by-64 1 1 1 1: Divide-by-128 0 1 0 1: Divide-by-256 Other settings are prohibited
		The Value after reset is different.	
	RPES[1:0]	-	Window End Position Select (b9-b8)
	RPSS[1:0]	-	Window Start Position Select (b13-b12)
IWDTSR	REFEF	-	Refresh Error Flag (b15)
IWDTRCR	-	-	IWDT Reset Control Register
IWDTCSTPR	-	-	IWDT Count Stop Control Register
OFS0	-	-	Option Function Select Register 0

2.21 Ethernet Controller

Table 2.41Table 2.45 shows a Comparative Listing of Ethernet Controller Specifications, and Table 2.42shows a Comparative Listing of Ethernet Controller Registers.

Table 2.41 Comparative Listing of Ethernet Controller Specifications

Item	RX62N(ETHERC)	RX65N(ETHERC)
Number of channels	1channel	1channel
Protocol	Flow control compliant with IEEE802.3x	Flow control compliant with IEEE802.3x
Data transmission/reception	Frames compliant with the Ethernet/IEEE802.3 standard can be transmitted and received.	Frames compliant with the Ethernet/IEEE802.3 standard can be transmitted and received.
Bit rate	Supports 10 Mbps and 100 Mbps	Supports 10 Mbps and 100 Mbps
Operation modes	Supports full-duplex and half-duplex modes	Supports full-duplex and half-duplex modes
Interfaces	Media Independent Interface (MII), Reduced Media Independent Interface (RMII), compliant with the IEEE802.3u standard	Media Independent Interface (MII), Reduced Media Independent Interface (RMII), compliant with the IEEE802.3u standard
Functions	Magic Packet™ *1 detection, Wake-On-LAN (WOL) signal output	Magic Packet™ *1 detection, Wake-On-LAN (WOL) signal output

*1:. Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

Table 2.42 Comparative Listing of Ethernet Controller Registers

Register	Bit	RX62N(ETHTERC)	RX65N(ETHERC)
ECMR	PRCEF	CRC Error Frame Reception Enable 0: A frame with a CRC error is received as a frame with an error. 1: A frame with a CRC error is received as a frame without an error.	CRC Error Frame Receive Mode 0: EDMAC is notified of a CRC error. 1: EDMAC is not notified of a CRC error.
ECSR	BFR	Continuous Broadcast Frame Reception Flag 0: Continuous reception of broadcast frames has not been Detected 1: Continuous reception of broadcast frames has been detected	Continuous Broadcast Frame Reception Flag 0: The number of continuously received broadcast frames has not exceeded the value set in the BCFRR register. 1: The number of continuously received broadcast frames has exceeded the value set in the BCFRR register.
RDMLR	RMD[19:0]	Upper Limit for Counter Used in Random Number Generation Block 00000h: Setting for normal operation 00001h to FFFFEh: Upper limit for the counter	Random Number Generation Counter 00000h: Normal operation 00001h to FFFFFh: Setting prohibited
RFCF	-	PAUSE Frame Receive Counter Register RFCF is a counter that indicates the number of times a PAUSE frame was received	Received PAUSE Frame Counter The RFCF register is a counter indicating the number of received PAUSE frames. The counter is reset after this register is read.
TPAUSECR	-	PAUSE Frame Retransmit Counter Register TPAUSECR is a counter that indicates the number of times a PAUSE frame was retransmitted.	PAUSE Frame Retransmit Counter The TPAUSECR register is a counter indicating the number of times a PAUSE frame was automatically retransmitted. The counter is reset after this register is read.

Register	Bit	RX62N(ETHTERC)	RX65N(ETHERC)
BCFRR	-	Broadcast Frame Receive Count Setting Register BCFRR specifies the number of Broadcast frames that can be received continuously. If the destination address (DA) can receive a frame with a Broadcast address up to the number of times set in these bits and frames have been received for more times than the specified count, the excess Broadcast frames are discarded. This setting must not be changed while the transmitting and receiving functions of BCFRR are enabled	Broadcast Frame Receive Count Setting Register The BCFRR register sets the number of times broadcast frames can be received continuously. When the number of received frames exceeds the BCF[15:0] bit value, the ECSR.BFR flag becomes 1 and the excess broadcast frames are discarded. The internal counter that counts the number of continuously received broadcast frames is reset when receiving any other frame than broadcast frame. Do not rewrite this register while the ECMR.RE bit is 1 (receive function is enabled).
MAHR	MA[47:16]: -	MAC Address Bits 47 to 16	MAC Address Bits 47 to 16

2.22 DMA Controller for the Ethernet Controller

Table 2.43 shows a Comparative Listing of DMA Controller for the Ethernet Controller Specifications, and Table 2.44 shows a Comparative Listing of DMA Controller for the Ethernet Controller Registers.

Table 2.43 Comparative Listing of DMA Controller for the Ethernet Controller Specifications

Item	RX62N(EDMAC)	RX65N(EDMACa)
Data transmission and reception	• Descriptor management system • Supports single-frame/multi-buffer operation	• Descriptor management system • Supports single-frame/multi-buffer operation
Functions	• Achieves efficient system bus utilization through the use of DMA block transfer (32-byte units) • Transmit/receive frame status information is indicated in descriptors • Padding can be inserted in receive data	• Achieves efficient system bus utilization through the use of DMA block transfer (32-byte units) • Transmit/receive frame status information is indicated in descriptors • Padding can be inserted in receive data
Low power consumption function	• The EDMAC can be set to the module-stop state to reduce power consumption	• The EDMAC can be set to the module-stop state to reduce power consumption

Table 2.44 Comparative Listing of DMA Controller for the Ethernet Controller Registers

Register	Bit	RX62N(EDMAC)	RX65N(EDMACa)
TDLAR	TDLA[31:0]: -	Transmit Descriptor List Start Address	–
RDLAR	RDLA[31:0] : -	Receive Descriptor List Start Address	–
EESR	CND	Carrier Not Detect Flag 0: A carrier is detected when transmission starts 1: A carrier has not been detected during preamble transmission or no transmission has been requested	Carrier Not Detect Flag 0: A carrier has been detected when transmission starts. 1: A carrier has not been detected during preamble transmission.
	ADE	Address Error Flag (b23)	-
EESIPR	ADEIP	Address Error Interrupt Enable (b23)	-
TRSCER		Transmit/Receive Status Copy Enable Register	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register
RMCR	RNC	Receive Request Bit Non-Reset Mode (b1)	-
RBWAR	-	Receive Buffer Write Address Register RBWAR stores the address of data to be written in the receive buffer by the EDMAC. Which addresses in the receive buffer are processed by the EDMAC can be recognized by monitoring addresses indicated in RBWAR. The address to which the EDMAC is actually writing may be different from the value read from RBWAR.	Receive Buffer Write Address Register The RBWAR register indicates the last address that the EDMAC has written data to when writing to the receive buffer. Refer to the address indicated by the RBWAR register to recognize which address in the receive buffer the EDMAC is writing data to. Note that the address that the EDMAC is outputting to the receive buffer may not match the read value of the RBWAR register during data reception. The RBWAR register is read only. Do not write to this register.

Register	Bit	RX62N(EDMAC)	RX65N(EDMACa)
RDFAR	-	Receive Descriptor Fetch Address Register RDFAR stores the descriptor start address that is required when the EDMAC fetches descriptor information from the receive descriptor. Which receive descriptor information is used for processing by the EDMAC can be recognized by monitoring addresses indicated in RDFAR. The address from which the EDMAC is actually fetching a descriptor may be different from the value read from RDFAR	Receive Descriptor Fetch Address Register The RDFAR register indicates the start address of the last fetched receive descriptor when the EDMAC fetches descriptor information from the receive descriptor. Refer to the address indicated by the RDFAR register to recognize which receive descriptor information the EDMAC is using for the current processing. Note that the address of the receive descriptor that the EDMAC fetches may not match the read value of the RDFAR register during data reception. The RDFAR is read only. Do not write to this register
TBRAR	-	Transmit Buffer Read Address Register TBRAR stores the address of data to be read from the transmit buffer by the EDMAC. Which addresses in the transmit buffer are processed by the EDMAC can be recognized by monitoring addresses indicated in TBRAR. The address from which the EDMAC is actually reading may be different from the value read from TBRAR.	Transmit Buffer Read Address Register The TBRAR register indicates the last address that the EDMAC has read data from when reading data from the transmit buffer. Refer to the address indicated by the TBRAR register to recognize which address in the transmit buffer the EDMAC is reading from. Note that the address that the EDMAC is outputting to the transmit buffer may not match the read value of the TBRAR register. The TBRAR register is read only. Do not write to this register.

Register	Bit	RX62N(EDMAC)	RX65N(EDMACa)
TDFAR	-	Transmit Descriptor Fetch Address Register TDFAR stores the descriptor start address that is required when the EDMAC fetches descriptor information from the transmit descriptor. Which transmit descriptor information is used for processing by the EDMAC can be recognized by monitoring addresses indicated in TDFAR. The address from which the EDMAC is actually fetching a descriptor may be different from the value read from TDFAR.	Transmit Descriptor Fetch Address Register The TDFAR register indicates the start address of the last fetched transmit descriptor when the EDMAC fetches descriptor information from the transmit descriptor. Refer to the address indicated by the TDFAR register to recognize which transmit descriptor information the EDMAC is using for the current processing. Note that the address of the transmit descriptor that the EDMAC fetches may not match the read value of the TDFAR register. The TDFAR is read only. Do not write to this register.
TRIMD	TIM	Transmit Interrupt Mode 0:Per-transmit-frame mode An interrupt is issued upon write-back completion of each frame. 1:Interrupt mode An interrupt is issued upon write-back completion of the transmit descriptor with the TD0.TWBI bit set to 1.	Transmit Interrupt Mode 0: Transmission complete interrupt mode An interrupt occurs when a frame has been transmitted 1: Write-back complete interrupt mode An interrupt occurs when write-back to the transmit descriptor has been completed while the TWBI bit is 1.

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2.23 USB 2.0 Function Module

Table 2.45 shows a Comparative Listing of USB 2.0 Function Module Specifications, and Table 2.46 shows a Comparative Listing of USB 2.0 Function Module Registers.

Table 2.45 Comparative Listing of USB 2.0 Function Module Specifications

Item	RX62N(USB)	RX65N(USBb)
Features	• USB Device Controller (UDC) and transceiver for USB2.0 are incorporated. • Two ports are provided. • The USB host controller and USB function controller are incorporated (can be switched by software). • Self-power mode or bus-power mode can be selected. • OTG (ON-The-Go) is supported. (1) Features of the USB host controller — Full-speed transfer (12 Mbps) is supported — Communications with multiple peripheral devices connected via a single HUB — Automatic scheduling for SOF and packet transmissions — Programmable intervals for isochronous and interrupt transfers (2) Features of the USB function controller — Full-speed transfer (12 Mbps) is supported*1 — Control transfer stage control function — Device state control function — Auto response function for SET_ADDRESS request — SOF recovery function	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • One port is provided. • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected. • Host controller, function controller, and On-The-Go (OTG) are supported (one channel) When the host controller is selected: — Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported — Multiple peripheral devices can be connected for communication via a one-stage hub. — Automatic scheduling for SOF and packet transmissions — Programmable intervals for isochronous and interrupt transfers When the function controller is selected: — Full-speed transfer (12 Mbps)*1 is supported — Control transfer stage control function — Device state control function — Auto response function for SET_ADDRESS request — SOF interpolation function
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer

Item	RX62N(USB)	RX65N(USBb)
Pipe configuration	• Buffer memory for USB communications is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: — PIPE0:Control transfer only (default control pipe: DCP) Buffer size: 8, 16, 32, or 64 bytes (single buffer) — PIPE1 and PIPE2:Bulk transfer or isochronous transfer Buffer size: 8, 16, 32, or 64 bytes for bulk transfer or 1 to 256 bytes for isochronous transfer (double buffer can be specified) — PIPE3 to PIPE5:Bulk transfer only Buffer size: 8, 16, 32, or 64 bytes (double buffer can be specified) — PIPE6 to PIPE9:Interrupt transfer only Buffer size: 1 to 64 bytes (single buffer)	• Buffer memory for USB communication is provided. • Up to 10 pipes can be selected (including the default control pipe). • PIPE1 to PIPE9 can be assigned any endpoint number Transfer conditions that can be set for each pipe: — PIPE0: Control transfer, 64-byte single buffer — PIPE1 and PIPE2: 64-byte double buffer can be specified for bulk transfer 256-byte double buffer for isochronous transfer — PIPE3 to PIPE5: Bulk transfer, 64-byte double buffer — PIPE6 to PIPE9: Interrupt transfer, 64-byte single buffer
Internal bus interface	• Connected to internal peripheral bus 3	-
Others	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/D–
Low power consumption function	Module stop state can be set.	Module stop state can be set.

*1 When the function controller is selected, low-speed transfer (1.5 Mbps) is not supported.

Table 2.46 Comparative Listing of USB 2.0 Function Module Registers

Register	Bit	RX62N(USB)	RX65N(USBb)
SYSCFG	SCKE	USB Module Clock Enable 0: Stops supplying the clock signal to the USB module. 1: Enables supplying the clock signal to the USB module.	USB Clock Enable 0: Stops supplying the clock signal to the USB. 1: Enables supplying the clock signal to the USB. After writing 1 to the SCKE bit, read it and confirm it is set to 1.
SYSSTS0	LNST[1:0]	USB Data Line Status Monitor b1 b0 0 0 : SE0 0 1 : J-State 1 0 : K-State 1 1 : SE1	USB Data Line Status Monitor Flag • During Low-Speed Operation (Only in Host Controller Operation) b1 b0 0 0 : SE0 0 1 : K-State 1 0 : J-State 1 1 : SE1 • During Full-Speed Operation b1 b0 0 0 : SE0 0 1 : J-State 1 0 : K-State 1 1 : SE1
	IDMON	External ID0 Input Pin Monitor	External ID0 Input Pin Monitor Flag
	SOFEA	-	SOF Active Monitor Flag When the Host Controller is Selected (b5)
	HTACT	USB Host Sequencer Status Monitor	USB Host Sequencer Status Monitor Flag
	OVCMON[1:0]	External USBm_OVRCURA/USBm_OVRCURB Input Pin Monitor The OVCMON[1] bit indicates the status of the USBm_OVRCURA pin. The OVCMON[0] bit indicates the status of the USBm_OVRCURB pin.	External USB0_OVRCURA/USB0_OVRCURB Input Pin Monitor Flag The OVCMON[1] flag indicates the status of the USB0_OVRCURA pin. The OVCMON[0] flag indicates the status of the USB0_OVRCURB pin.

<table>
<tr><th>Register</th><th>Bit</th><th>RX62N(USB)</th><th>RX65N(USBb)</th></tr>
<tr><td>DVSTCTR0</td><td>RHST[2:0]</td><td>USB Bus Reset Status

When the host controller function is selected
b2 b1 b0
0 0 0: Communication speed not determined
(powered state or no connection)
1 x x: USB bus reset in progress
0 0 1: Low-speed connection*1
0 1 0: Full-speed connection
[Legend] x: Don’t care

When the function controller function is selected
b2 b1 b0
0 0 0: Communication speed not determined

0 1 0: USB bus reset in progress or full-speed connection

*1. The USB controller does not support communication with a low-speed device. When this value is read, abnormal connection processing should be executed in a higher application.</td><td>USB Bus Reset Status Flag

When the host controller is selected
b2 b0
0 0 0: Communication speed not determined
(powered state or no connection)
1 x x: USB bus reset in progress
0 0 1: Low-speed connection
0 1 0: Full-speed connection

When the function controller is selected
b2 b0
0 0 0: Communication speed not determined
0 0 1: USB bus reset in progress
0 1 0: USB bus reset in progress or full-speed connection</td></tr>
<tr><td rowspan="2">CFIFO
D0FIFO
D1FIFO</td><td rowspan="2">L[7:0](b15~b8)
FIFO Port</td><td colspan="2">MBW=”1”</td></tr>
<tr><td>MDMONR.MDE＝“0”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND=0: N+1 address
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N address (Bytes of data inverted)</td><td>MDE.MDE[2:0]＝“000”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =0: N+1 address (Bytes of data inverted)
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: address</td></tr>
</table>

<table>
<tr><th>Register</th><th>Bit</th><th>RX62N(USB)</th><th>RX65N(USBb)</th></tr>
<tr><td rowspan="5"></td><td rowspan="3"></td><td>MDMONR.MDE＝“1”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND=0: N+1 address(Bytes of data inverted)
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N address</td><td>MDE.MDE[2:0]＝“111”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =0: N+1 address CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N address (Bytes of data inverted)</td></tr>
<tr><td colspan="2">MBW=”0”</td></tr>
<tr><td>The start address should be accessed in bytes.</td><td>The start address should be accessed in bytes.</td></tr>
<tr><td rowspan="3">H[7:0](b7~b0)
FIFO Port</td><td colspan="2">MBW=”1”</td></tr>
<tr><td>MDMONR.MDE＝“0”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =0: N address
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N+1 address(Bytes of data inverted)</td><td>MDE.MDE[2:0]＝“000”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =0: N address (Bytes of data inverted)
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N+1 address</td></tr>
<tr><td>MDMONR.MDE＝“1”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =0: N address(Bytes of data inverted)
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N+1 address</td><td>MDE.MDE[2:0]＝“111”
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =0: N address
CFIFOSEL.BIGEND/
D0FIFOSEL.BIGEND/
D1FIFOSEL.BIGEND =1: N+1 address (Bytes of data inverted)</td></tr>
<tr><td>D0FIFOSEL
D1FIFOSEL</td><td>DREQE</td><td>DMA Transfer Request Enable

0: DMA transfer request is disabled.
1: DMA transfer request is enabled</td><td>DMA/DTC Transfer Request Enable
0: DMA/DTC transfer request is disabled.
1: DMA/DTC transfer request is enabled.</td></tr>
<tr><td>CFIFOCTR
D0FIFOCTR
D1FIFOCTR</td><td>BVAL</td><td>Buffer Memory Valid Flag</td><td>Buffer Memory Valid</td></tr>
<tr><td>SOFCFG</td><td>TRNENSEL</td><td>-</td><td>Transaction-Enabled Time Select (b8)</td></tr>
</table>

Register	Bit	RX62N(USB)	RX65N(USBb)
INTSTS0	CTSQ[2:0]	Control Transfer Stage b2 b0 0 0 0 : Idle or setup stage . . 1 0 1 : Control write (no data) status stage 1 1 0 : Control transfer sequence error 1 1 1 : Setting prohibited	Control Transfer Stage Flag b2 b0 0 0 0 : Idle or setup stage . . 1 0 1 : Control write (no data) status stage 1 1 0 : Control transfer sequence error
	VALID	USB Request Reception	USB Request Reception Flag
	DVSQ[2:0]	Device State	Device State Flag
	VBSTS	VBUS Input Status	VBUS Input Status Flag
	BRDY	Buffer Ready Interrupt Status	Buffer Ready Interrupt Status Flag
	NRDY	Buffer Not Ready Interrupt Status	Buffer Not Ready Interrupt Status Flag
	BEMP	Buffer Empty Interrupt Status	Buffer Empty Interrupt Status Flag
	CTRT	Control Transfer Stage Transition Interrupt Status	Control Transfer Stage Transition Interrupt Status Flag
	DVST	Device State Transition Interrupt Status	Device State Transition Interrupt Status Flag
	SOFR	Frame Number Refresh Interrupt Status	Frame Number Refresh Interrupt Status Flag
	RESM	Resume Interrupt Status	Resume Interrupt Status Flag
	VBINT	VBUS Interrupt Status	VBUS Interrupt Status Flag
INTSTS1	SACK	Setup Transaction Normal Response Interrupt Status	Setup Transaction Normal Response Interrupt Status Flag
	SIGN	Setup Transaction Error Interrupt Status	Setup Transaction Error Interrupt Status Flag
	EOFERR	EOF Error Detection Interrupt Status	EOF Error Detection Interrupt Status Flag
	ATTCH	ATTCH Interrupt Status	ATTCH Interrupt Status Flag
	DTCH	USB Disconnection Detection Interrupt Status	USB Disconnection Detection Interrupt Status Flag
	BCHG	USB Bus Change Interrupt Status	USB Bus Change Interrupt Status Flag
	OVRCR	Overcurrent Input Change Interrupt Status	Overcurrent Input Change Interrupt Status Flag
BRDYSTS	PIPE0BRDY	BRDY Interrupt Status for PIPE0	BRDY Interrupt Status Flag for PIPE0
	PIPE1BRDY	BRDY Interrupt Status for PIPE1	BRDY Interrupt Status Flag for PIPE1
	PIPE2BRDY	BRDY Interrupt Status for PIPE2	BRDY Interrupt Status Flag for PIPE2
	PIPE3BRDY	BRDY Interrupt Status for PIPE3	BRDY Interrupt Status Flag for PIPE3
	PIPE4BRDY	BRDY Interrupt Status for PIPE4	BRDY Interrupt Status Flag for PIPE4
	PIPE5BRDY	BRDY Interrupt Status for PIPE5	BRDY Interrupt Status Flag for PIPE5

Register	Bit	RX62N(USB)	RX65N(USBb)
	PIPE6BRDY	BRDY Interrupt Status for PIPE6	BRDY Interrupt Status Flag for PIPE6
	PIPE7BRDY	BRDY Interrupt Status for PIPE7	BRDY Interrupt Status Flag for PIPE7
	PIPE8BRDY	BRDY Interrupt Status for PIPE8	BRDY Interrupt Status Flag for PIPE8
	PIPE9BRDY	BRDY Interrupt Status for PIPE9	BRDY Interrupt Status Flag for PIPE9
NRDYSTS	PIPE0NRDY	NRDY Interrupt Status for PIPE0	NRDY Interrupt Status Flag for PIPE0
	PIPE1NRDY	NRDY Interrupt Status for PIPE1	NRDY Interrupt Status Flag for PIPE1
	PIPE2NRDY	NRDY Interrupt Status for PIPE2	NRDY Interrupt Status Flag for PIPE2
	PIPE3NRDY	NRDY Interrupt Status for PIPE3	NRDY Interrupt Status Flag for PIPE3
	PIPE4NRDY	NRDY Interrupt Status for PIPE4	NRDY Interrupt Status Flag for PIPE4
	PIPE5NRDY	NRDY Interrupt Status for PIPE5	NRDY Interrupt Status Flag for PIPE5
	PIPE6NRDY	NRDY Interrupt Status for PIPE6	NRDY Interrupt Status Flag for PIPE6
	PIPE7NRDY	NRDY Interrupt Status for PIPE7	NRDY Interrupt Status Flag for PIPE7
	PIPE8NRDY	NRDY Interrupt Status for PIPE8	NRDY Interrupt Status Flag for PIPE8
	PIPE9NRDY	NRDY Interrupt Status for PIPE9	NRDY Interrupt Status Flag for PIPE9
BEMPSTS	PIPE0BEMP	BEMP Interrupt Status for PIPE0	BEMP Interrupt Status Flag for PIPE0
	PIPE1BEMP	BEMP Interrupt Status for PIPE1	BEMP Interrupt Status Flag for PIPE1
	PIPE2BEMP	BEMP Interrupt Status for PIPE2	BEMP Interrupt Status Flag for PIPE2
	PIPE3BEMP	BEMP Interrupt Status for PIPE3	BEMP Interrupt Status Flag for PIPE3
	PIPE4BEMP	BEMP Interrupt Status for PIPE4	BEMP Interrupt Status Flag for PIPE4
	PIPE5BEMP	BEMP Interrupt Status for PIPE5	BEMP Interrupt Status Flag for PIPE5
	PIPE6BEMP	BEMP Interrupt Status for PIPE6	BEMP Interrupt Status Flag for PIPE6
	PIPE7BEMP	BEMP Interrupt Status for PIPE7	BEMP Interrupt Status Flag for PIPE7
	PIPE8BEMP	BEMP Interrupt Status for PIPE8	BEMP Interrupt Status Flag for PIPE8
	PIPE9BEMP	BEMP Interrupt Status for PIPE9	BEMP Interrupt Status Flag for PIPE9

Register	Bit	RX62N(USB)	RX65N(USBb)
FRMNUM	FRNM[10:0]	Frame Number Repeatreading the FRNM[10:0] bits until the same value is read twice.	Frame Number Flag
	CRCE	Receive Data Error	Receive Data Error Flag
	OVRN	Overrun/Underrun Detection Status	Overrun/Underrun Detection Status Flag
USBVAL	— WVALUE[15:0]	- These bits store the USB request wValue value.	Value These bits store the USB request wValue value.
USBINDX	— WINDEX[15:0]	- These bits store the USB request wIndex value.	Index These bits store the USB request wIndex value.
USBLENG	— WLENGTH[15:0]	- These bits store the USB request wLength value.	Length These bits store the USB request wLength value.
DCPCTR	PBUSY	Pipe Busy	Pipe Busy Flag
	SQMON	Sequence Toggle Bit Monitor	Sequence Toggle Bit Monitor Flag
	BSTS	Buffer Status	Buffer Status Flag
	SQSET	Toggle Bit Set	Sequence Toggle Bit Set
	SQCLR	Toggle Bit Clear	Sequence Toggle Bit Clear
PIPEnCTR	PBUSY	Pipe Busy	Pipe Busy Flag
	SQMON	Toggle Bit Confirmation	Sequence Toggle Bit Confirmation
	INBUFM	Transmit Buffer Monitor	Transmit Buffer Monitor Flag
	BSTS	Buffer Status	Buffer Status Flag
PIPEnTRN n=1~5	- TRNCNT[15:0]	-	Transaction Counter
DEVADDn n=0~5	USBSPD[1:0]	Transfer Speed of Communication Target Device b7 b6 0 0: DEVADDn is not used 0 1: Setting prohibited 1 0: Full speed 1 1: Setting prohibited	Transfer Speed of Communication Target Device b7 b6 0 0: DEVADDn is not used 0 1: Low-speed 1 0: Full-speed 1 1: Setting prohibited
PHYSLEW	-	-	PHY Cross Point Adjustment Register
DPUSR0R	RPUE0	-	D+ Pull-Up Resistor Control (b1)
	DRPD0	-	D+/D– Pull-Down Resistor Control (b3)
	SRPC1	USB1 Single End Receiver Control (b8)	-
	FIXPHY1	USB1 Transceiver Output Fix (b12)	-
	DP0	USB0 DP Input	USB D+ Input Flag
	DM0	USB0 DM Input	USB D- Input Flag
	DOVCA0	USB0 OVRCURA Input	USB OVRCURA Input Flag
	DOVCB0	USB0 OVRCURB Input	USB OVRCURB Input Flag

Register	Bit	RX62N(USB)	RX65N(USBb)
	DP1	USB1 DP Input (b24)	-
		The Value after reset is different.	
	DM1	USB1 DM Input (b24)	-
		The Value after reset is different.	
	DOVCA1	USB1 OVRCURA 入力(b28)	-
		The Value after reset is different.	
	DOVCB1	USB1 OVRCURB Input (b29)	-
		The Value after reset is different.	
	DVBSTS1	USB1 VBUS Input (b31)	-
		The Value after reset is different.	
DPUSR1R	DPINTE1	USB1 DP Interrupt Enable/Clear (b8)	-
	DMINTE1	USB1 DM Interrupt Enable/Clear (b9)	-
	DOVRCRAE1	USB1 OVRCURA Interrupt Enable/Clear (b12)	-
	DOVRCRBE1	USB1 OVRCURB Interrupt Enable/Clear (b13)	-
	DVBSE1	USB1 VBUS Interrupt Enable/Clear (b15)	-
	DPINT0	USB0 DP Interrupt Source Recovery Flag	USB D+ Interrupt Source Recovery Flag
	DMINT0	USB0 DM Interrupt Source Recovery Flag	USB D-Interrupt Source Recovery Flag
	OVRCURAINT0: DOVRCRA0	USB0 OVRCURA Interrupt Source Recovery Flag	USB OVRCURA Interrupt Source Recovery Flag
	OVRCURBINT0: DOVRCRB0	USB0 OVRCURB Interrupt Source Recovery Flag	USB OVRCURB Interrupt Source Recovery Flag
	DVBINT0	USB0 VBUS Interrupt Source Recovery Flag	USB VBUS Interrupt Source Recovery Flag
	DPINT1	USB1 DP Interrupt Source Recovery Flag)	-
	DMINT1	USB1 DM Interrupt Source Recovery Flag (b25)	-
	DOVRCRA1	USB1 OVRCURA Interrupt Source Recovery Flag (b28)	-
	DOVRCRB1	USB1 OVRCURB Interrupt Source Recovery Flag (b29)	-
	DVBINT1	USB1 VBUS Interrupt Source Recovery Flag (b31)	-

Note: * When the function controller is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller is selected, these bits can be read from and written to.

2.24 Serial Communications Interface

The RX62N Group has 6 independent serial communications interface channels (SCIc: 6 channels, SCId: 1 channel).

The RX65N Group has 13 independent serial communications interface channels (SCIg: 10 channels, SCIi: 2 channels, SCIh: 1 channel).

Table 2.47 shows a Comparative Listing of SCIa and SCIg Specifications, Table 2.48 shows a Comparative Listing of SCIi Specifications, Table 2.49 shows a Comparative Listing of SCIh Specifications, Table 2.50 shows a Comparative Listing of Serial Communications Interface Channels Specifications, and Table 2.51 shows a Comparative Listing of Serial Communications Interface Registers.

Table 2.47 Comparative Listing of SCIa and SCIg Specifications

Item		RX62N(SCIa)	RX65N(SCIg)
Number of channel		6channels	10channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with on-chip baud rate generator	Bit rate specifiable with on-chip baud rate generator
Full-duplex communications		• Transmitter: Enables continuous transmission by double-buffering • Receiver: Enables continuous reception by double-buffering	• Transmitter: Enables continuous transmission by double-buffering • Receiver: Enables continuous reception by double-buffering
Data transfer		Selectable from LSB-first or MSB-first transfer	Selectable from LSB-first or MSB-first transfer(*1)
Interrupt sources		Transmit-end, transmit-data-empty, receive-data-full, and receive error	Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Power consumption function		Module stop state can be set for each channel	Module stop state can be set for each channel
Asynchronous mode	Data length	7or 8bits	7,8 or 9bits
	Transfer stop bit	1 or 2bits	1 or 2bits
	Parity	Even, odd, or none	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Detect the Low	Low level or falling edge is selectable.
	Break detection	Break can be detected by reading RxDn (n = 0 to 3, 5, 6) pin level directly in case of a framing error	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.

Item		RX62N(SCIa)	RX65N(SCIg)
Asynchronous mode	Clock source	• Selectable from internal or external clock • Enables transfer rate clock input from TMR (SCI5 and SCI6)	• An internal or external clock can be selected • Transfer rate clock input from the TMR can be used. (SCI5, SCI6)
	Double-speed mode	-	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	-	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8bits	8bits
	Receive error detection	Overrun errors	Overrun error
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted on detection of a parity error during reception	An error signal can be utomatically transmitted when detecting a parity error during reception
		Data can be automatically re-transmitted on receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	-	I^2C-bus format
	Operating mode	-	Master (single-master operation only)
	Transfer rate	-	Fast mode is supported (refer to section 37.2.13, Bit Rate Register (BRR) to set the transfer rate).
	Noise cancellation	-	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, • The interval for noise cancellation is adjustable.
Simple SPI bus	Data length	-	8bits
	Detection of errors	-	Overrun error
	SS input pin function	-	Applying the high level to the SSn# pin can cause the output pins to enter the highimpedance state.
	Clock settings	-	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		-	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function		-	Error (receive error or error signal detection) event output

Item	RX62N(SCIa)	RX65N(SCIg)
	-	Receive data full event output
	-	Transmit data empty event output
	-	Transmit end event output

*1. In simple I²C mode, only MSB first is available

Table 2.48 Comparative Listing of SCIi Specifications

Item		RX62N(-)	RX65N(SCIi)
Number of channel		-	2channels
Serial communication modes		-	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		-	Bit rate specifiable with on-chip baud rate generator
Full-duplex communications		-	• Transmitter: Enables continuous transmission by double-buffering • Receiver: Enables continuous reception by double-buffering
Data transfer		-	Selectable from LSB-first or MSB-first transfer(*1)
Interrupt sources		-	Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Power consumption function		-	Module stop state can be set for each channel
Asynchronous mode	Data length	-	7,8 or 9bits
	Transfer stop bit	-	1 or 2bits
	Parity	-	Even parity, odd parity, or no parity
	Receive error detection	-	Parity, overrun, and framing errors
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	-	16-stage FIFOs for transmit and receive buffers
	Data match detection	-	Compares receive data and comparison data, and generates interrupt when they are matched
	Start-bit detection	-	Low level or falling edge is selectable.
	Break detection	-	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	-	An internal or external clock can be selected.

Item		RX62N(-)	RX65N(SCIi)
	Double-speed mode	-	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	-	Serial communication among multiple processors
	Noise cancellation	-	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	-	8bits
	Receive error detection	-	Overrun error
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	-	16-stage FIFOs for transmit and receive buffers
Smart card interface mode	Error processing	-	An error signal can be utomatically transmitted when detecting a parity error during reception
		-	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	-	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	-	I^2C-bus format
	Operating mode	-	Master (single-master operation only)
	Transfer rate	-	Fast mode is supported (refer to section 37.2.13, Bit Rate Register (BRR) to set the transfer rate).
	Noise cancellation	-	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, • The interval for noise cancellation is adjustable.
Simple SPI bus	Data length	-	8bits
	Detection of errors	-	Overrun error
	SS input pin function	-	Applying the high level to the SSn# pin can cause the output pins to enter the highimpedance state.
	Clock settings	-	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		-	Correction of outputs from the on-chip baud rate generator can reduce errors.

*1. In simple I^2C mode, only MSB first is available

Table 2.49 Comparative Listing of SCIh Specifications

Item	RX62N(-)	RX65N(SCIh)

Item		RX62N(-)	RX65N(SCIh)
Number of channel		-	1channel
Serial communication modes		-	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C-bus • Simple SPI bus
Transfer speed		-	Bit rate specifiable with on-chip baud rate generator
Full-duplex communications		-	• Transmitter: Enables continuous transmission by double-buffering • Receiver: Enables continuous reception by double-buffering
Data transfer		-	Selectable from LSB-first or MSB-first transfer(*1)
Interrupt sources		-	Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Power consumption function		-	Module stop state can be set for each channel
synchronous mode	Data length	-	7,8 or 9bits
	Transfer stop bit	-	1 or 2bits
	Parity	-	Even parity, odd parity, or no parity
	Receive error detection	-	Parity, overrun, and framing errors
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	-	Low level or falling edge is selectable.
	Break detection	-	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	-	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI12)
	Double-speed mode	-	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	-	Serial communication among multiple processors
	Noise cancellation	-	The signal paths from input on the RXDn pins incorporate digital noise filters.

Item		RX62N(-)	RX65N(SCIh)
Clock synchronous mode	Data length	-	8bits
	Receive error detection	-	Overrun error
	Hardware flow control	-	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	-	An error signal can be automatically transmitted when detecting a parity error during reception
		-	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	-	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	-	I^2C-bus format
	Operating mode	-	Master (single-master operation only)
	Transfer rate	-	Fast mode is supported (refer to section 37.2.13, Bit Rate Register (BRR) to set the transfer rate).
	Noise cancellation	-	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, • The interval for noise cancellation is adjustable.
Simple SPI bus	Data length	-	8bits
	Detection of errors	-	Overrun error
	SS input pin function	-	Applying the high level to the SSn# pin can cause the output pins to enter the highimpedance state.
	Clock settings	-	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode	Start Frame transmission	-	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection

Item		RX62N(-)	RX65N(SCIh)
	Start Frame reception	-	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field • Function for measuring bit rates
	I/O control function	-	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.
	Timer function	-	Usable as a reloading timer
Bit rate modulation function		-	Correction of outputs from the on-chip baud rate generator can reduce errors.

*1. In simple I^2C mode, only MSB first is available

Table 2.50 Comparative Listing of Serial Communications Interface Channels Specifications

Item	RX62N(SCIa)	RX65N(SCIg, SCIi, SCIh)
Asynchronous mode	SCI0,SCI1,SCI2,SCI3,SCI5,SCI6	SCI0～SCI12
Clock synchronous mode	SCI0,SCI1,SCI2,SCI3,SCI5,SCI6	SCI0～SCI12
Smart card interface mode	SCI0,SCI1,SCI2,SCI3,SCI5,SCI6	SCI0～SCI12
Simple I²C mode	-	SCI0～SCI12
Simple SPI bus	-	SCI0～SCI12
Extended serial mode	-	SCI12
TMR Clock Input	SCI5,SCI6	SCI5, SCI6, SCI12
Event link function	-	SCI5
FIFO mode	-	SCI10, SCI11

Table 2.51 Comparative Listing of Serial Communications Interface Registers

Register	Bit	RX62N(SCIa)	RX65N(SCIg, SCIi, SCIh)
RDRH	-	-	Receive Data Register H
RDRL	-	-	Receive Data Register L
RDRHL	-	-	Receive Data Register HL
FRDR	-	-	Receive FIFO Data Register
TDRH	-	-	Transmit Data Register H
TDRL	-	-	Transmit Data Register L
TDRHL	-	-	Transmit Data Register HL
FTDR	-	-	Transmit FIFO Data Register
SMR	CHR	Character Length (Valid only in asynchronous mode)) 0: Selects 8 bits as the data length 1: Selects 7 bits as the data length	Character Length (Valid only in asynchronous mode)) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length*3
	CM	Communications Mode 0: Asynchronous mode 1: Clock synchronous mode	Communications Mode 0: Asynchronous mode or simple I²C mode 1: Clock synchronous mode or simple SPI mode

SSRFIFO	-	-	Serial Status Register
SCMR	SINV	Smart Card Data Invert	Transmitted/Received Data Invert
	SDIR	Smart Card Data Transfer Direction 0: Transfer with LSB-first 1: Transfer with MSB-first	Transmitted/Received Data Transfer Direction This bit can be used in the following modes. • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode Set this bit to 1 if operation is to be in simple I²C mode. 0: Transfer with LSB first 1: Transfer with MSB first
	CHR1	-	Character Length 1(b4)
BRR	-	Bit Rate Register In the Asynchronous mode, the set value and the bitrate depends on SEMR.ABCS bit setting. For more related information, refer to the user's manual.	Bit Rate Register In the Asynchronous mode and the Multiprocessor communication mode, the set value and the bitrate depends on SEMR.BGDM and SEMR.ABCS bit setting. For more related information, refer to the user's manual. In case of SCI10 & SCI11,when SMR.CM=”1”(Clock synchronous mode or simple SPI mode),FCR.FM = “1”(FIFO mode) and SMR.CKS[1:0] =”00b” ,do not write the value of “00h” to BBR Register
MDDR	-	-	Modulation Duty Register
SEMR	BRME	-	Bit Rate Modulation Enable (b2)
	NFEN	-	Digital Noise Filter Function Enable (b5)
	BGDM	-	Baud Rate Generator Double-Speed Mode Select (b6)
	RXDESEL	-	Asynchronous Start Bit Edge Detection Select (b7)
SNFR	-	-	Noise Filter Setting Register
SIMR1	-	-	I²C Mode Register 1
SIMR2	-	-	I²C Mode Register 2
SIMR3	-	-	I²C Mode Register 3
SISR	-	-	I²C Status Register

SPMR	-	-	SPI Mode Register
FCR	-	-	FIFO Control Register
FDR	-	-	FIFO Data Count Register
LSR	-	-	Line Status Register
CDR	-	-	Comparison Data Register
DCCR	-	-	Comparison Data Register
SPTR	-	-	Serial Port Register
ESMER	-	-	Extended Serial Module Enable Register
CR0	-	-	Control Register 0
CR1	-	-	Control Register 1
CR2	-	-	Control Register 2
CR3	-	-	Control Register 3
PCR	-	-	Port Control Register
ICR	-	-	Interrupt Control Register
STR	-	-	Status Register
STCR	-	-	Status Register
CF0DR	-	-	Control Field 0 Data Register
CF0CR	-	-	Control Field 0 Compare Enable Register
CF0RR	-	-	Control Field 0 Receive Data Register
PCF1DR	-	-	Primary Control Field 1 Data Register
SCF1DR	-	-	Primary Control Field 1 Data Register
CF1CR	-	-	Control Field 1 Compare Enable Register
CF1RR	-	-	Control Field 1 Receive Data Register
TCR	-	-	Timer Control Register
TMR	-	-	Timer Mode Register
TPRE	-	-	Timer Prescaler Register
TCNT	-	-	Timer Count Register

2.25 I²C-bus Interface

Table 2.52 shows a Comparative Listing of I2C-bus Interface Specifications, and Table 2.53 shows a Comparative Listing of I2C-bus Interface Registers.

Table 2.52 Comparative Listing of I²C-bus Interface Specifications

Item	RX62N(RIIC)	RX65N(RIICa)
Number of channel	2channles	2channles
Communications format	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various set-up times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Up to 1M bps	Fast-mode Plus is supported (up to 1 Mbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three slave-address settings can be made. • Seven- and ten-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible (i.e. the return of ACK or NACK is selectable).	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.

Item	RX62N(RIIC)	RX65N(RIICa)
Wait function	• In reception, the following periods of waiting can be obtained by holding the clock signal (SCL) at the low level: Waiting between the eighth and ninth clock cycles (timing of the received data full interrupt can be selected for this); Waiting between the ninth clock cycle and the first clock cycle of the next transfer (WAIT function)	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: Waiting between the eighth and ninth clock cycles Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the not-acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation Operation to synchronize the SCL (clock) signal in cases of conflict with the SCL signal from another master is possible. When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout detection function is capable of detecting long-interval stoppages of the SCL (clock signal).	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.

Item	RX62N(RIIC)	RX65N(RIICa)
Interrupt sources	Four sources: • Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete	Four sources: • Error in transfer or occurrence of events. Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	-	Module stop state can be set.
RIIC operating modes	-	Four Master transmit mode, master receive mode, slave transmit mode, and slave receive mode
Event link function (output)	-	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Table 2.53 Comparative Listing of I²C-bus Interface Registers

Register	Bit	RX62N(RIIC)	RX65N(RIICa)
ICMR2	TMWE	Timeout Internal Counter Write Enable (b3)	-
ICFER	FMPE	Fast-mode Plus Enable	Fast-Mode Plus Enable *
TMOCNT	-	Timeout Internal Counter	-

* : The Fast-mode Plus enable bit (FMPE) is only supported by RIIC0. In RIIC2, bit 7 is reserved.

2.26 CAN Module

Table 2.54 shows a Comparative Listing of CAN Module Specifications, and Table 2.55 shows a Comparative Listing of CAN Module Registers.

Table 2.54 Comparative Listing of CAN Module Specifications

Item	RX62N(CAN)	RX65N(CAN)
Number of channel	1channel	2channels
Protocol	ISO11898-1 compliant (standard and extended frames)	ISO11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate up to 1 Mbps (fCAN ≧ 8 MHz) fCAN: CAN clock source	Programmable bit rate up to 1 Mbps (fCAN ≧ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable from overwrite mode (message overwritten) and overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX62N(CAN)	RX65N(CAN)
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox.	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable from ID priority mode and mailbox number priority mode • Transmission request can be aborted (the completion of abort can be confirmed with a flag) The transmission complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	• Mode transition for the recovery from the bus-off state can be selected: — ISO11898-1 Specifications compliant — Automatic entry to CAN halt mode at bus-off entry — Automatic entry to CAN halt mode at bus-off end — Entry to CAN halt mode by a program — Transition into error-active state by a program	• Mode transition for the recovery from the bus-off state can be selected: — ISO11898-1 Specifications compliant — Automatic entry to CAN halt mode at bus-off entry — Automatic entry to CAN halt mode at bus-off end — Entry to CAN halt mode by a program Transition into error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and busoff recovery). • The error counters can be read.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and busoff recovery). The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five types of interrupt sources (reception complete, transmission complete, receive FIFO,transmit FIFO, and error interrupts)	Five types of interrupt sources (reception complete, transmission complete, receive FIFO,transmit FIFO, and error interrupts)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support unit	Three software support units: Acceptance filter support Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) Channel search support	Three software support units: Acceptance filter support Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) Channel search support
CAN clock source	Peripheral module clock (PCLK)	Peripheral module clock (PCLKB) or CANMCLK

Item	RX62N(CAN)	RX65N(CAN)
Test mode	Three test modes available for user evaluation Listen-only mode Self-test mode 0 (external loopback) Self-test mode 1 (internal loopback)	Three test modes available for user evaluation Listen-only mode Self-test mode 0 (external loopback) Self-test mode 1 (internal loopback)
Power consumption reducing function	Module-stop state can be set.	Module-stop state can be set.

Table 2.55 Comparative Listing of CAN Module Registers

Register	Bit	RX62N(USBa)	RX65N(USBb)
BCR	CCLKS	-	CAN Clock Source Selection (b0)
MKIVLR	-:/ MB31~MB0	-	Mask Invalid
MIER	Normal mailbox mode		
	-: MB31~MB0	Interrupt Enable	Interrupt Enable
	FIFO mailbox mode		
	-: MB23~MB0	Interrupt Enable	Interrupt Enable
	-: MB24	Transmit FIFO Interrupt Enable	Transmit FIFO Interrupt Enable
	-: MB25	Transmit FIFO Interrupt Generation Timing Control	Transmit FIFO Interrupt Generation Timing Control
	-: MB28	Receive FIFO Interrupt Enable	Receive FIFO Interrupt Enable
	-: MB29	Receive FIFO Interrupt Generation Timing Control	Receive FIFO Interrupt Generation Timing Control
RFCR	RFUST[2:0]	Receive FIFO Unread Message Number Status	Receive FIFO Unread Message Number Status Flag
TFCR	TFUST[2:0]	Transmit FIFO Unsent Message Number Status	Transmit FIFO Unsent Message Number Status Flag
	TFFST	Transmit FIFO Full Status	Transmit FIFO Full Status Flag
	TFEST	Transmit FIFO Empty Status	Transmit FIFO Empty Status Flag
STR	-	Status Register	Status Register
		The Value after reset is different.	
MSSR	MBNST[4:0]	Search Result Mailbox Number Status	Search Result Mailbox Number Status Flag
	SEST	Search Result Status	Search Result Status Flag

2.27 Serial Peripheral Interface

Table 2.56 shows a Comparative Listing of Serial Peripheral Interface Specifications, and Table 2.57 shows a Comparative Listing of Serial Peripheral Interface Registers.

Table 2.56 Comparative Listing of Serial Peripheral Interface Specifications

Item	RX62N(RSPI)	RX65N(RSPIc)
Number of channels	2channels	3channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Capable of serial communications in master/slave mode • Switching of the polarity of the serial transfer clock • Switching of the phase of the serial transfer clock
Data format	• MSB-first/LSB-first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB-first/LSB-first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8).Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4).Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	Double buffer configuration for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX62N(RSPI)	RX65N(RSPIc)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection* • Parity error detection • Underrun error detection
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSL0 to SSL3 signals are output. • In multi-master mode: SSL0 signal for input, and SSL1 to SSL3 signals for either output or high-impedance • In slave mode: SSL0 signal for input, and SSL1 to SSL3 signals for high-impedance • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stoppage to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSL0 to SSL3 signals are output. • In multi-master mode: SSL0 signal for input, and SSL1 to SSL3 signals for either output or high-impedance • In slave mode: SSL0 signal for input, and SSL1 to SSL3 signals for high-impedance • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stoppage to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first,burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first,burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, parity error)) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)

Item	RX62N(RSPI)	RX65N(RSPIc)
Event link function (output)	-	The following events can be output to the event link controller. • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, underrun, or parity error signal • RSPI idle signal • Transmission-completed signal
Others	• Function for switching between CMOS output and open-drain output • Function for disabling (initializing) the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Module stop state can be set.	Module stop state can be set.

* In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped at the timing of overrun error detection

Table 2.57 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX62N(RSPI)	RX65N(RSPIc)
SPPCR	SPOM	**RSPI Output Pin Mode(b2)**	-
SPSR	MODF	**Mode Fault Error Flag** 0: No mode fault error occurs 1: A mode fault error occurs	**Mode Fault Error Flag** 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	-	Underrun Error Flag (b4)
SPDR	-	RSPI Data Register Available access size • Longwords: (SPDCR.SPLW=1) • Words: (SPDCR.SPLW=0)	RSPI Data Register Available access size • Longwords: (SPDCR.SPLW=1,SPBYTE=0) • Words: (SPDCR.SPLW=0,SPBYTE=0) • Bytes (SPDCR.SPBYT=1)
SPDCR	SLSEL[1:0]	SSI Pin Output Selection (b3-b2)	-
	SPBYT	-	RSPI Byte Access Specification (b6)
SPCR2	SCKASE	-	RSPCK Auto-Stop Function Enable
SPDCR2	-	-	RSPI Data Control Register2

2.28 CRC Calculator

Table 2.58 shows a Comparative Listing of CRC Calculator Specifications, and Table 2.59 shows a Comparative Listing of CRC Calculator Registers.

Table 2.58 Comparative Listing of CRC Calculator Specifications

Item	RX62N(CRC)	RX65N(CRCA)	
Data size	8bits	8bits	32bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on eight bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials selectable • 8-bit CRC — $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC — $X^8 + X^2 + X + 1$ • 16-bit CRC — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption	Module stop state can be set	Module stop state can be set	

Table 2.59 Comparative Listing of CRC Calculator Registers

Register	Bit	RX62N(CRC)	RX65N(CRCA)
CRCCR	GPS[1:0] GPS[2:0]	CRC Generating Polynomial Switching (b1-b0) b1 b0 0 0 : No calculation is executed. 0 1 : $X^8 + X^2 + X + 1$ 1 0 : $X^{16} + X^{15} + X^2 + 1$ 1 1 : $X^{16} + X^{12} + X^5 + 1$	CRC Generating Polynomial (b2-b0) b2 b0 0 0 0 : No calculation is executed. 0 0 1 : 8-bit CRC($X^8 + X^2 + X + 1$) 0 1 0 : 16-bit CRC($X^{16} + X^{15} + X^2 + 1$) 0 1 1 : 16-bit CRC($X^{16} + X^{12} + X^5 + 1$) 1 0 0 : 32-bit CRC($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1 : 32-bit CRC($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0 : No calculation is executed. 1 1 1 : No calculation is executed.
	LMS	CRC Calculation Switching (b2)	CRC Calculation Switching (b6)
CRCDIR	-	CRC Data Input Register Access Size • Byte Access	CRC Data Input Register Access Size • Long word Access (When 32-bit CRC is selected) • Byte Access (When 16-bit or 8-bit CRC is selected)
CRCDOR	-	CRC Data Output Register Access Size • Word Access When an 8-bit, CRC code is obtained in the lower-order byte (b7～b0)	CRC Data Output Register Access Size • Long word Access (When 32-bit CRC is selected) • Word Access (When 16-bit CRC is selected) • Byte Access (When 8-bit CRC is selected)

2.29 Boundary Scan

Table 2.60Table 2.62 shows a Comparative Listing of Boundary Scan Specifications, and Table 2.61shows a Comparative Listing of Boundary Scan Registers.

Table 2.60 Comparative Listing of Boundary Scan Specifications

Item	RX62N	RX65N
Boundary scan enabled/disabled	Boundary can is enabled when the EMLE pin is driven low and the BSCANP pin is driven high.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLEpin is driven low
Dedicated boundary scan pins	The following pins are dedicated for JTAG, when boundary scan function is enabled (TDO/TCK/TDI/TMS/TRST#). 176-pin LFBGA： PF0/PF1/PF2/PF3/PF4 145-pin TFLGA/144-pin LQFP： P26/P27/P30/P31/P34 85-pin TFLGA： P26/P27/P30/P31/P34	The following pins are dedicated for JTAG, when boundary scan function is enabled(TDO/TCK/TDI/TMS/TRST#) 145-pin TFLGA：P26/P27/P30/P31/P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

Table 2.61 Comparative Listing of Boundary Scan Registers

Register	RX62N			RX65N		
	Value after Reset	Serial Input	Serial Output	Value after Reset	Serial Input	Serial Output
JTIR	55h	Available	Not available	55h	Available	Available
JTIDR	080B B447h	Not available	Available	0831 6447h	Available	Available
JTBPR	Undefined	Available	Available	Undefined	Available	Available
JTBSR	Undefined	Available	Available	Undefined	Available	Available

2.30 12-Bit A/D Converter

Table 2.62 shows a Comparative Listing of 12-Bit A/D Converter Specifications, and Table 2.63 shows a Comparative Listing of 12-Bit A/D Converter Registers.

Table 2.62 Comparative Listing of 12-Bit A/D Converter Specifications

Item	RX62N(S12AD)	RX65N(S12ADFa)
Number of units	1	2
Input channels	8channels	• S12AD:8channels • S12AD1:21chennels+ 1 Extension
Extended analog function	-	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12bits	12bits
Conversion time	1.0μs per 1 channel (when operating with peripheral module clock PCLK = 50 MHz)	• 0.48 μs per channel (12-bit conversion mode) • 0.45 μs per channel (10-bit conversion mode) • 0.42 μs per channel (8-bit conversion mode) (A/D conversion clock: when ADCLK operates at 60 MHz)
A/D conversion clock(ADCLK)	4 types: PCLK, PCLK/2, PCLK/4, PCLK/8	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.

Item	RX62N(S12AD)	RX65N(S12ADFa)
Data registers	• Eight data registers	• 29 registers for analog input (eight for S12AD and 21 for S12AD1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD1) • One register for internal reference (S12AD1) • One register for self-diagnosis per unit
	• The A/D conversion result is held in a 12-bit A/D data register.	• The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion
	• In A/D-converted value addition mode, 14 bits of data are stored in an A/D data register.	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.
		• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX62N(S12AD)	RX65N(S12ADFa)
Operating modes	• Single-cycle scan mode: — A/D conversion is to be performed for only once on the analog inputs of up to eight arbitrarily selected channels. maximum 8channels	• Single-cycle scan mode: — A/D conversion is performed only once on the analog inputs arbitrarily selected S12AD : maximum : 8 channels S12AD1 : maximum 21 channels — A/D conversion is performed only once on the temperature sensor output (S12AD1) — A/D conversion is performed only once on the internal reference voltage (S12AD1). — A/D conversion is performed only once on the extended analog input (S12AD1).
	• Continuous scan mode: — A/D conversion is to be performed sequentially on the analog inputs of up to eight arbitrarily selected channels maximum 8channels	• Continuous scan mode: — A/D conversion is performed repeatedly on the analog input, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) of the arbitrarily selected channel S12AD: maximum 8 channels S12AD1 : maximum 21 channels. — A/D conversion is performed repeatedly on the extended analog input (S12AD1).
		• Group scan mode:: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used — Only the combination of groups A and B can be selected when the number of the groups is two. — Analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently.

Item	RX62N(S12AD)	RX65N(S12ADFa)
Operating modes	-	• Group scan mode (when group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Conversion start trigger by the multifunction timer pulse unit (MTU) or 8-bit timer (TMR). • Asynchronous trigger A/D conversion can be triggered from the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) or ADTRG1# (S12AD1) pin (independently for two units).
Functions	• Sample-and-hold function • A/D-converted value addition mode	• Sample-and-hold function • Channel-dedicated sample-and-hold function (three channels for S12AD only) • Variable sampling state count (settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • 12-/10-/8-bit conversion switching • Automatic clear function of A/D data registers • Extended analog input • Comparison function (windows A and B)

Item	RX62N(S12AD)	RX65N(S12ADFa)
Interrupt sources	• A/D conversion end interrupt (S12ADI0) request can be generated on completion of A/D conversion. • • An S12ADI0 interrupt can activate DMA controller (DMACA) or data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (independently for two units). • In double trigger mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan. (independently for two units) • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of group A scan, whereas a scan end interrupt request (GBADI or GBADI1) for group B can be generated on completion of group B scan, and a group C scan end interrupt request (GCADI or GCADI1) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI/GCADI or GBADI1/GCADI1) can be generated on completion of group B and group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1, GBADI/GBADI1, and GCADI/GCADI1 interrupts can activate the DMA controller (DMAC) and data transfer controller (DTC).
Event link	-	• An ELC event is generated upon completion of all scans • Able to start scanning by a trigger from the ELC
Low power consumption function	Module stop state can be set(*1)	Module stop state can be set(*2)

*1: When the module stop state is canceled, A/D conversion can be started after 10 ms has elapsed

*2:Wait for 1 μs or longer to start A/D conversion after release from the module stop state.

Table 2.63 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX62N(S12AD)	RX65N(S12ADFa)
ADDRn: ADDRy		A/D Data Registers n (n=0~7)	A/D Data Registers y (y=0~7：S12AD y=0~20：S12AD1)
ADDBLDR	-	-	A/D Data Duplication Register
ADDBLDRA	-	-	A/D Data Duplication Register A
ADDBLDRB	-	-	A/D Data Duplication Register B
ADTSDR	-	-	A/D Temperature Sensor Data Register
ADOCDR	-	-	A/D Internal Reference Voltage Data Register
ADRD	-	-	A/D Self-Diagnosis Data Register
ADCSR RX62N：8bits RX65N：16bits	EXTRG	Trigger Select (b0) 0: Scan conversion is started by a timer source selected by the A/D start trigger select register (ADSTRGR). 1: Scan conversion is started by an external trigger (ADTRG0#).	Trigger Select (b8) 0: A/D conversion is started by synchronous trigger. 1: A/D conversion is started by asynchronous trigger.
	TRGE	Trigger Enable (b1) 0: Disables scan conversion to be started by an external trigger (ADTRG0#) or a trigger of MTU or TMR. 1: Enables scan conversion to be started by an external trigger (ADTRG0#) or a trigger of MTU or TMR.	Trigger Start Enable (b9) 0: Disables A/D conversion to be started by synchronous or asynchronous trigger. 1: Enables A/D conversion to be started by synchronous or asynchronous trigger.
	CKS[1:0]	Clock Select (b3-b2)	-
	ADIE	A/D Scan Conversion End Interrupt Enable (b4)	Scan End Interrupt Enable(b12)
	ADCS	Scan Conversion Mode Select (b6)	-
	ADST	A/D Conversion Start (b7)	A/D Conversion Start (b15)
	DBLANS[4:0]	-	Double Trigger Channel Select (b4-b0)
	GBADIE	-	Group B Scan End Interrupt Enable (b6)
	DBLE	-	Double Trigger Mode Select (b7)
	ADCS[1:0]	-	Scan Mode Select(b14-b13)
ADANS	-	A/D Channel Select Register	-
ADANSA0	-	-	A/D Channel Select Register A0
ADANSA1	-	-	A/D Channel Select Register A1
ADANSB0	-	-	A/D Channel Select Register B0

Register	Bit	RX62N(S12AD)	RX65N(S12ADFa)
ADANSB1	-	-	A/D Channel Select Register B1
ADANSC0	-	-	A/D Channel Select Register C0
ADANSC1	-	-	A/D Channel Select Register C1
ADADS	-	A/D-Converted Value Addition Mode Select Register	
ADADS0	-	-	A/D-Converted Value Addition/Average Function Select Register 0
ADADS1	-	-	A/D-Converted Value Addition/Average Function Select Register 1
ADADC	-	A/D-Converted Value Addition Count Select Register	A/D-Converted Value Addition/Average Count Select Register
	ADC[1:0] ADC[2:0]	Addition Count Select (b1-b0) b1b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition Count Select (b2-b0) b2b0 0 0 0: 1-time conversion (no addition; same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice)*1 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times)*1 Settings other than above are prohibited.
	AVEE	-	Average Mode Enable (b7)
ADCER	ADPRC[1:0]	-	A/D Conversion Resolution Setting (b2-b1)
	ACE	Automatic Clearing Enable	A/D Data Register Automatic Clearing Enable
	DIAGVAL[1:0]	-	Self-Diagnosis Conversion Voltage Select (b9-b8)
	DIAGLD	-	Self-Diagnosis Mode Select (b10)
	DIAGM	-	Self-Diagnosis Enable (b11)
ADSTRGR RX62N：8bits RX65N：16bits	ADSTRS[3:0]	A/D Start Trigger Select (b3-b0)	-
	TRSB[5:0]	-	A/D Conversion Start Trigger Select for Group B (b5-b0)
	TRSA[5:0]	-	A/D Conversion Start Trigger Select (b13-b8)
ADEXICR	-	-	A/D Conversion Extended Input Control Register
ADGCEXCR	-	-	A/D Group C Extended Input Control Register
ADGCTRGR	-	-	A/D Group C Trigger Select Register
ADSSTRn	-	-	A/D Sampling State Register n(n = 0～15, L, T, O)
ADSHCR	-	-	A/D Sample-and-Hold Circuit Control Register
ADSHMSR	-	-	A/D Sample-and-Hold Operating Mode Select Register

Register	Bit	RX62N(S12AD)	RX65N(S12ADFa)
ADDISCR	-	-	A/D Disconnection Detection Control Register
ADGSPCR	-	-	A/D Group Scan Priority Control Register
ADCMPCR	-	-	A/D Comparison Function Control Register
ADCMPANSR0	-	-	A/D Comparison Function Window A Channel Select Register 0
ADCMPANSR1	-	-	A/D Comparison Function Window A Channel Select Register 1
ADCMPANSER	-	-	A/D Comparison Function Window A Extended Input Select Register
ADCMPLR0	-	-	A/D Comparison Function Window A Comparison Condition Setting Register 0
ADCMPLR1	-	-	A/D Comparison Function Window A Comparison Condition Setting Register 1
ADCMPLER	-	-	A/D Comparison Function Window A Extended Input Comparison Condition Setting Register
ADCMPDR0	-	-	A/D Comparison Function Window A Lower Level Setting Register
ADCMPDR1	-	-	A/D Comparison Function Window A Upper Level Setting Register
ADCMPSR0	-	-	A/D Comparison Function Window A Channel Status Register 0
ADCMPSR1	-	-	A/D Comparison Function Window A Channel Status Register 1
ADCMPSER	-	-	A/D Comparison Function Window A Extended Input Channel Status Register
ADWINMON	-	-	A/D Comparison Function Window A/B Status Monitoring Register
ADCMPBNSR	-	-	A/D Comparison Function Window B Channel Select Register
ADWINLLB	-	-	A/D Comparison Function Window B Lower Level Setting Register
ADWINULB	-	-	A/D Comparison Function Window B Upper Level Setting Register
ADCMPBSR	-	-	A/D Comparison Function Window B Channel Status Register
ADSAM	-	-	A/D Conversion Time Setting Register
ADSAMPR	-	-	A/D Conversion Time Setting Protection Release Register

2.31 D/A Converter

Table 2.64 shows a Comparative Listing of D/A Converter Specifications, and Table 2.65 shows a Comparative Listing of D/A Converter Registers.

Table 2.64 Comparative Listing of D/A Converter Specifications

Item	RX62N	RX65N(R12DA)
Resolution	10bits	12bits
Output channels	2channels	2channels
Countermeasure against mutual interference between analog modules	-	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 1). Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function (input)	-	DA0 conversion can be started when an event signal is input.
Output buffer amplifier control function	-	Buffered output (gain = 1) or unbuffered can be selected.

Table 2.65 Comparative Listing of D/A Converter Registers

Register	Bit	RX62N	RX65N(R12DA)
DADRm	-	D/A Data Register m(DADRm)(m=0,1) 10-bit data can be relocated by setting the DPSEL bit in DADPR	D/A Data Register m(DADRm)(m=0,1) 12-bit data can be relocated by setting the DADPR.DPSEL bit
DAADSCR	-	-	D/A A/D Synchronous Start Control Register
DAADUSR	-	-	D/A A/D Synchronous Unit Select Register
DAAMPCR	-	-	D/A Output Amplifer Control Register
DAASWCR	-	-	D/A Output Amplifer Stabilization Wait Control Register

2.32 RAM

Table 2.66 shows a Comparative Listing of RAM Specifications, and Table 2.67 shows a Comparative Listing of RAM Registers.

Table 2.66 Comparative Listing of RAM Specifications

Item	RX62N	RX65N(Without ECC Error Correction)
RAM capacity	• 64Kbytes RAM0:64Kbytes • 96Kbytes RAM0:64Kbytes,RAM1:32Kbytes	256Kbytes RAM0:256Kbytes
RAM address	• 64Kbytes as RAM capacity RAM0:0000 0000h～0000 FFFFh RAM1:- • 96Kbytes as RAM capacity RAM0:0000 0000h～0000 FFFFh RAM1:0001 0000h～0001 7FFFh	RAM0:0000 0000h ～ 0003 FFFFh
Access	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of on-chip RAM is selectable	• Single-cycle access is possible for both reading and writing.*(*1) • Enabling or disabling of the RAM is selectable
Data retention function	Data in RAM0 can be retained during periods in deep standby mode	Not available in deep software standby mode(Data in the Standby RAM can be retained)
Power-down function	The module stop state is independently selectable for RAM0 and RAM1.	The module-stop state is selectable
Error checking	-	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error

*1: When accessing across the 8-byte boundary, the number of cycles is doubled

Table 2.67 Comparative Listing of RAM Registers

Register	Bit	RX62N	RX65N
RAMMODE	-	-	RAM Operating Mode Control Register
RAMSTS	-	-	RAM Error Status Register
RAMECAD	-	-	RAM Error Address Capture Register
RAMPRCR	-	-	RAM Protection Register

2.33 Flash Memory (Code Flash)

Table 2.68 shows a Comparative Listing of Flash Memory (Code Flash) Specifications, and Table 2.69 shows a Comparative Listing of Flash Memory Registers.

Table 2.68 Comparative Listing of Flash Memory (Code Flash) Specifications

Item	RX62N	RX65N
Memory capacity	• User mat: 512 Kbytes, 384 Kbytes, or 256 Kbytes • User boot mat: 16 Kbytes	User area: 1 Mbyte max.
ROM cache	-	• Capacity: 256 Bytes • Mapping method: 8-way set associative • Replace method: LRU method • Line size: 16 bytes
Read cycle	One Cycle of ICLK	When the cache is hit: One cycle When the cache is missed: One cycle if ICLK ≦50 MHz Two cycles if 50 MHz < ICLK <100 MHz Three cycles if ICLK > 100 MHz
Value after erasure	FFh	FFh
Programming/erasing method	• The chip incorporates a dedicated sequencer (FCU) for programming of the ROM. • Programming and erasing the ROM are handled by issuing commands to the FCU.	• Programming and erasing the code flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h) • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
Security function	Protects against illicit tampering with or reading out of data in flash memory	Protects against illicit tampering with or reading out of data in flash memory
Protection	• Software-controlled protection: The FENTRYR.FENTRY0, FWEPROR.FLWE[1:0], and lock bits can be used to prevent unintentional programming • Error protection Prevention of further programming or erasure after the detection of abnormal operations during programming or erasure	Protects against erroneous rewriting of the flash memory
Trusted memory (TM) function	-	Protects against illicit reading of blocks 8 and 9 in the code flash memory

Item	RX62N	RX65N
BGO (background operation)	• The CPU is able to execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased • Execution of program code from the ROM is possible while the data flash memory is being programmed or erased	-
Suspension and resumption	• The CPU is able to execute program code from the ROM during suspension of programming or erasure • Programming and erasure of the ROM can be restarted (resumed) after suspension	• The CPU is able to execute program code from the Code-Flash during suspension of programming or erasure • Programming and erasure of the Code-Flash can be restarted (resumed) after suspension
Units of programming and erasure	• Unit of programming for the user mat and the user boot mat: 256 bytes. • Unit of erasure for the user mat: 4 Kbytes (8 blocks), 16 Kbytes (30 blocks) • Unit of erasure for the user boot mat: 16 Kbytes	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units
Others	-	Interrupts can be accepted during self-programming)
	-	The startup area of the code flash memory is selectable from blocks 0 and 1.

Item	RX62N	RX65N
On-board programming	• Boot Mode — The user mat and the user boot mat are programmable via the SCI. — The transfer rate is adjusted automatically • USB (user) boot mode — Booting up from the user boot mat and programming of the user mat — The USB boot program is stored in the user boot mat at shipment; the user mat is programmable via the USB — Programming the user boot mat allows programming of the user mat via an arbitrary interface • User program — Programming of the user mat under program control	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used — The transfer rate is adjusted automatically • Programming/erasure in boot mode (for the USB interface) — USBb is used — Dedicated hardware is not required, so direct connection to a PC is possible • Programming/erasure in boot mode (for the FINE interface) — FINE is used • Programming/erasure by a routine for code flash memory programming within the user Program — This allows code flash memory programming/erasure without resetting the system
Programming and Erasure by Dedicated Parallel Programmer	A PROM programmer can be used to program or erase the user area and user boot area.	A flash programmer can be used to program or erase the user area
Unique ID	-	A 16-byte ID code provided for each MCU

Table 2.69 Comparative Listing of Flash Memory Registers

Register	Bit	RX62N	RX65N
FWEPROR	-	Flash Write Erase Protection Register	Flash P/E Protect Register
	FLWE[1:0]	Flash Write Erase	Flash Programming and Erasure Enable
FMODR	-	Flash Mode Register	-
FASTAT	DFLWPE	Data Flash Programming/Erasure Protection Violation (b0)	-
	DFLRPE	Data Flash Read Protection Violation (b1)	-
	DFLAE	Data Flash Access Violation (b3)	-
	CMDLK	FCU Command Lock	Command Lock Flag
	ROMAE	ROM Access Violation (b7)	-
	CFAE	-	Code Flash Memory Access Violation Flag (b7)

Register	Bit	RX62N	RX65N
FAEINT	DFLWPEIE	Data Flash Programming/Erasure Protection Violation Interrupt Enable(b0)	-
		The Value after reset is different.	
	DFLRPEIE	Data Flash Read Protection Violation Interrupt Enable (b1)	-
		The Value after reset is different.	
	DFLAEIE	Data Flash Access Violation Interrupt Enable (b3)	-
	ROMAEIE	ROM Access Violation Interrupt Enable (b7)	-
	CFAEIE	-	Code Flash Memory Access Violation Interrupt Enable (b7)
FSADDR	-	-	FACI Command Start Address Register
FCURAME	-	FCU RAM Enable Register	-
FSTATR0	-	Flash Status Register 0	-
FSTATR1	-	Flash Status Register 1	-
FSTATR	-	-	Flash Status Register
FENTRYR	FENTRY0	ROM P/E Mode Entry 0 (b0)	-
	FENTRYC	-	Code Flash Memory P/E Mode Entry (b0)
	FENTRYD	Data Flash P/E Mode Entry (b7)	-
	FEKEY[7:0]: KEY[7:0]	Key Code (b15-b8)	Key Code (b15-8)
FPROTR	-	Flash Protection Register	-
FRESETR	-	Flash Reset Register	-
FCMDR	-	FCU Command Register	FACI Command Register
FSUINITR	-	-	Flash Sequencer Set-Up Initialization Register
FAWMON	-	-	Flash Access Window Monitor Register
FPESTAT	-	Flash P/E Status Register	-
FCPSR	-	FCU Processing Switching Register	Flash Sequencer Processing Switching Register
FPCKAR	-	-	Flash Sequencer Processing Clock Notification Register
FSUACR	-	-	Start-Up Area Control Register
PCKAR	-	Peripheral Clock Notification Register	-
ROMCE	-	-	ROM Cache Enable Register
ROMCIV	-	-	ROM Cache Invalidate Register
UIDRn	-	-	Unique ID Register n (n = 0 ～ 3)

3. Comparison of Pin Functions

A comparison of the pin functions, power supply, clock, system control pins is provided below.

Blue character : Items that exist only in either group.

Red character : Items that exist in both group, but they have differences.

Black character : Items that are same specification.

3.1 144 Package

Table 3.1 shows a Comparative Listing of Pin Functions (144pin Package).

Table 3.1 Comparative Listing of Pin Functions (144pin Package)

144pin LFQFP	RX62N	RX65N
1	AVSS	AVSS0
2	P05/IRQ13-A/DA1	P05/IRQ13/DA1
3	VCC	AVCC1
4	P03/IRQ11-A/DA0	P03/IRQ11/DA0
5	VSS	AVSS1
6	P02/TMCI1-A/SCK6-A/IRQ10-A	P02/TMCI1/SCK6/IRQ10/AN120
7	P01/TMCI0-A/RxD6-A/IRQ9-A	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
8	P00/TMRI0-A/TxD6-A/IRQ8-A	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
9	BSCANP	PF5/IRQ4
10	EMLE	EMLE
11	WDTOVF#	PJ5/POE8#/CTS2#/RTS2#/SS2#
12	VSS	VSS
13	MDE	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
14	VCL	VCL
15	MD1	VBATT
16	MD0	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES#	RES#
20	XTAL	XTAL/P37
21	VSS	VSS
22	EXTAL	EXTAL/P36

144pin LFQFP	RX62N	RX65N
23	VCC	VCC
24	P35/NMI	UPSEL/P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/SCK6-B/IRQ4-A	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
26	P33/MTIOC0D/PO11/CRX0/RxD6-B/IRQ3-A	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS
27	P32/MTIOC0C/PO10/RTCOUT/CTX0/TxD6-B/IRQ2-A	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
28	TMS/P31/MTIOC4D-A/TMCI2-B/PO9/SSLB0-A/IRQ1	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	TDI/P30/MTIOC4B-A/TMRI3/PO8/RxD1/MISOB-A/IRQ0	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
30	TCK/P27/CS7#-C/MTIOC2B/PO7/SCK1/RSPCKB-A	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
31	TDO/P26/CS6#-C/MTIOC2A/TMO1/PO6/MOSIB-A/TxD1	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
32	P25/CS5#-C/EDACK1-B/USB0_DPRPD/MTIOC4C-A/MTCLKB-A/PO5/RxD3-B/ADTRG0#-B	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0#
33	P24/CS4#-C/EDREQ1-B/MTIOC4A-A/MTCLKA-A/TMRI1/PO4/SCK3-B/USB0_VBUSEN-A	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK
34	P23/EDACK0-B/USB0_DPUPE-A/MTIOC3D-A/MTCLKD-A/PO3/TxD3-B	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7
35	P22/EDREQ0-B/MTIOC3B-A/MTCLKC-A/TMO0/PO2/SCK0/USB0_DRPD	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6
36	P21/MTIOC1B/TMCI0-B/PO1/SCL1/RxD0/USB0_EXICEN	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9
37	P20/MTIOC1A/TMRI0-B/PO0/SDA1/TxD0/USB0_ID	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8
38	P17/MTIOC3A/PO15/TxD3-A/IRQ7-B	P17/MTIOC3A/MTIOC3B/MTIOC4B/TI

144pin LFQFP	RX62N	RX65N
		OCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1#
39	PLLVCC	P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2
40	P16/MTIOC3C-A/TMO2/PO14/RxD3-A/USB0_VBUS/USB0_VBUSEN-B/USB0_OVRCURB/IRQ6-B	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
41	PLLVSS	P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1
42	P15/MTIOC0B/TMCI2-A/PO13/SCK3-A/IRQ5-B	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5
43	P14/TMRI2/USB0_OVRCURA/USB0_DPUPE-B/IRQ4-B	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
44	P13/TMO3/TxD2-A/SDA0/IRQ3-B/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
45	P12/TMCI1-B/RxD2-A/SCL0/IRQ2-B	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
46	VCC_USB	VCC_USB
47	USB0_DM	USB0_DM
48	USB0_DP	USB0_DP
49	VSS_USB	VSS_USB
50	P56/EDACK1-C/MTIOC3C-B	P56/EDACK1/MTIOC3C/TIOCA1
51	TRDATA3/P55/WAIT#-B/EDREQ0-C/MTIOC4D-B/ET_EXOUT	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10
52	TRDATA2/P54/EDACK0-C/MTIOC4B-B/ET_LINKSTA	TRDATA2/P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA
53	BCLK/P53	BCLK/P53
54	P52/RD#/RxD2-B/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	P51/WR1#/BC1#/WAIT#/SSLB2-A/SCK2
56	P50/WR0#/WR#/TxD2-B/SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
57	VSS	VSS

144pin LFQFP	RX62N	RX65N
58	TRCLK/P83/EDACK1-A/MTIOC4C-B/ET_CRS/RMII_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/CTS10#/SS10#/ET0_CRS/RMII0_CRS_DV/SCK10
59	VCC	VCC
60	PC7/A23/CS0#-B/MTIC11U-A/MTCLKB-B/MISOA-A/ET_COL	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14
61	PC6/A22/CS1#-C/MTIC11V-A/MTCLKA-B/MOSIA-A/ET_ETXD3	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13
62	PC5/A21/CS2#-C/WAIT#-C/MTIC11W-A/MTCLKD-B/RSPCKA-A/ET_ETXD2	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/MMC_D5-A
63	TRSYNC/P82/EDREQ1-A/MTIOC4A-B/ET_ETXD1/RMII_TXD1	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET0_ETXD1/RMII0_TXD1/MMC_D4-A
64	TRDATA1/P81/EDACK0-A/MTIOC3D-B/ET_ETXD0/RMII_TXD0	TRDATA1/P81/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET0_ETXD0/RMII0_TXD0/MMC_D3-A/SDHI_CD-A/QIO3-A
65	TRDATA0/P80/EDREQ0-A/MTIOC3B-B/ET_TX_EN/RMII_TXD_EN	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/QIO2-A
66	PC4/A20/CS3#-C/MTCLKC-B/SSLA0-A/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A
67	PC3/A19-A/ET_TX_ER/MTCLKF-A/TxD5	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A
68	P77/CS7#-B/ET_RX_ER/RMII_RX_ER	TRDATA7/P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/ET0_RX_ER/RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A
69	P76/CS6#-B/ET_RX_CLK/REF50CK	TRDATA6/P76/CS6#/PO22/RXD11/SMISO11/SSCL11/ET0_RX_CLK/REF50CK0/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A

144pin LFQFP	RX62N	RX65N
70	PC2/A18-A/ET_RX_DV/MTCLKE-A/SSLA3-A/RxD5	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/MMC_CD-A/SDHI_D3-A/SDSI_D3-A
71	P75/CS5#-B/ET_ERXD0/RMII_RXD0	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A
72	P74/CS4#-B/ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/CTS11#/SS11#/ET0_ERXD1/RMII0_RXD1
73	PC1/A17-A/ET_ERXD2/MTCLKH-A/SSLA2-A/SCK5	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
74	VCC	VCC
75	PC0/A16-A/ET_ERXD3/MTCLKG-A/SSLA1-A	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
76	VSS	VSS
77	P73/CS3#-B/ET_WOL	TRDATA4/P73/CS3#/PO16/ET0_WOL
78	PB7/A15/MTIOC10D/PO31	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
79	PB6/A14/MTIOC10B/PO30	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
80	PB5/A13/MTIOC10C/MTCLKF-B/PO29	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B
81	PB4/A12/MTIOC10A/MTCLKE-B/PO28	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B
82	PB3/A11/MTIOC9D/MTCLKH-B/PO27	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B
83	PB2/A10/MTIOC9B/MTCLKG-B/PO26	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B
84	PB1/A9/MTIOC9C/PO25	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS
85	P72/CS2#-B/ET_MDC	P72/A19/CS2#/ET0_MDC

144pin LFQFP	RX62N	RX65N
86	P71/CS1#-B/ET_MDIO	P71/A18/CS1#/ET0_MDIO
87	PB0/A8/MTIOC9A/PO24	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12
88	PA7/A7/MTIOC8B/PO23/MISOA-B	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL
89	PA6/A6/MTIOC8A/PO22/MOSIA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT
90	PA5/A5/MTIOC7B/PO21/RSPCKA-B	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA
91	VCC	VCC
92	PA4/A4/MTIOC7A/PO20/SSLA0-B	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC6D/PO19	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS
95	PA2/A2/MTIOC6C/PO18/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B
96	PA1/A1/MTIOC6B/PO17/SSLA2-B	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11
97	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN
98	P67/CS7#-A/DQM1	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	P66/CS6#-A/DQM0	P66/CS6#/DQM0/MTIOC7D
100	P65/CS5#-A/CKE	P65/CS5#/CKE
101	PE7/D15/MISOB-B/IRQ7-A	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105
102	PE6/D14/MOSIB-B/IRQ6-A	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104
103	VCC	VCC
104	SDCLK/P70	SDCLK/P70
105	VSS	VSS
106	PE5/D13/RSPCKB-B/IRQ5-A	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103

144pin LFQFP	RX62N	RX65N
107	PE4/D12/SSLB0-B	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102
108	PE3/D11/POE8#	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101
109	PE2/D10/POE9#/SSLB3-B	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100
110	PE1/D9/SSLB2-B	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1
111	PE0/D8/SSLB1-B	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0
112	P64/CS4#-A/WE#	P64/CS4#/WE#
113	P63/CS3#-A/CAS#	P63/CS3#/CAS#
114	P62/CS2#-A/RAS#	P62/CS2#/RAS#
115	P61/CS1#-A/SDCS#	P61/CS1#/SDCS#
116	VSS	VSS
117	P60/CS0#-A	P60/CS0#
118	VCC	VCC
119	PD7/D7/MTIC5U/POE0#	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107
120	PD6/D6/MTIC5V/POE1#	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106
121	PD5/D5/MTIC5W/POE2#	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113
122	PD4/D4/MTIC11U-B/POE3#	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112
123	PD3/D3/MTIC11V-B/POE4#	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111
124	PD2/D2/MTIC11W-B/POE5#	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110
125	PD1/D1/POE6#	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109

144pin LFQFP	RX62N	RX65N
126	PD0/D0/POE7#	PD0/D0[A0/D0]/POE4#/IRQ0/AN108
127	P93/A19-B	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
128	P92/A18-B	P92/A18/POE4#/RXD7/SMISO7/SSCL7/AN116
129	P91/A17-B	P91/A17/SCK7/AN115
130	VSS	VSS
131	P90/A16-B	P90/A16/TXD7/SMOSI7/SSDA7/AN114
132	VCC	VCC
133	P47/IRQ15-B/AN7	P47/IRQ15-DS/AN007
134	P46/IRQ14/AN6	P46/IRQ14-DS/AN006
135	P45/IRQ13-B/AN5	P45/IRQ13-DS/AN005
136	P44/IRQ12/AN4	P44/IRQ12-DS/AN004
137	P43/IRQ11-B/AN3	P43/IRQ11-DS/AN003
138	P42/IRQ10-B/AN2	P42/IRQ10-DS/AN002
139	P41/IRQ9-B/AN1	P41/IRQ9-DS/AN001
140	VREFL	VREFL0
141	P40/IRQ8-B/AN0	P40/IRQ8-DS/AN000
142	VREFH	VREFH0
143	AVCC	AVCC0
144	P07/IRQ15-A/ADTRG0#-A	P07/IRQ15/ADTRG0#

3.2 145pin Package

Table 3.1 shows a Comparative Listing of Pin Functions (144pin Package).

Table 3.2 Comparative Listing of Pin Functions (144/145pin Package)

145pin TFLGA	RX62N	145pin TFLGA	RX65N
A1	AVSS	A1	AVSS0
A2	AVCC	B2	AVCC0
A3	VREFL	B4	VREFL0
A4	P42/IRQ10-B/AN2	A4	P42/IRQ10-DS/AN002
A5	P44/IRQ12/AN4	E5	P44/IRQ12-DS/AN004
A6	P47/IRQ15-B/AN7	B6	P47/IRQ15-DS/AN007
A7	P91/A17-B	B7	P91/A17/SCK7/AN115
A8	PD0/D0/POE7#	B8	PD0/D0[A0/D0]/POE4#/IRQ0/AN108
A9	PD3/D3/MTIC11V-B/POE4#	C8	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111
A10	PD6/D6/MTIC5V/POE1#	A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106
A11	P60/CS0#-A	D8	P60/CS0#
A12	P62/CS2#-A/RAS#	A11	P62/CS2#/RAS#
A13	P64/CS4#-A/WE#	D9	P64/CS4#/WE#
B1	P03/IRQ11-A/DA0	D3	P03/IRQ11/DA0
B2	P07/IRQ15-A/ADTRG0#-A	A2	P07/IRQ15/ADTRG0#
B3	VREFH	C3	VREFH0
B4	P40/IRQ8-B/AN0	A3	P40/IRQ8-DS/AN000
B5	P45/IRQ13-B/AN5	A5	P45/IRQ13-DS/AN005
B6	P90/A16-B	A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114
B7	PD1/D1/POE6#	C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109
B8	PD5/D5/MTIC5W/POE2#	D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113
B10	PE0/D8/SSLB1-B	C11	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0
B11	PE2/D10/POE9#/SSLB3-B	B12	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100

145pin TFLGA	RX62N	145pin TFLGA	RX65N
B12	PE1/D9/SSLB2-B	A12	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1
B13	PE4/D12/SSLB0-B	B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102
C1	P01/TMCI0-A/RxD6-A/IRQ9-A	D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
C2	P05/IRQ13-A/DA1	B3	P05/IRQ13/DA1
C4	P41/IRQ9-B/AN1	C4	P41/IRQ9-DS/AN001
C5	P46/IRQ14/AN6	C5	P46/IRQ14-DS/AN006
C6	P92/A18-B	A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/AN116
C7	PD2/D2/MTIC11W-B/POE5#	A8	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110
C8	PD7/D7/MTIC5U/POE0#	C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107
C9	P61/CS1#-A/SDCS#	B11	P61/CS1#/SDCS#
C10	P63/CS3#-A/CAS#	C10	P63/CS3#/CAS#
C11	PE5/D13/RSPCKB-B/IRQ5-A	D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103
C12	PE3/D11/POE8#	A13	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101
C13	SDCLK/P70	C12	P70/SDCLK
D1	EMLE	E4	EMLE
D3	P02/TMCI1-A/SCK6-A/IRQ10-A	C2	P02/TMCI1/SCK6/IRQ10/AN120
D4	P43/IRQ11-B/AN3	B5	P43/IRQ11-DS/AN003
D7	P93/A19-B	D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
D8	PD4/D4/MTIC11U-B/POE3#	B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112
D12	PE7/D15/MISOB-B/IRQ7-A	D10	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105
D13	PE6/D14/MOSIB-B/IRQ6-A	D13	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104
E1	VCL	E2	VCL

145pin TFLGA	RX62N	145pin TFLGA	RX65N
E3	P00/TMRI0-A/TxD6-A/IRQ8-A	D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
E4	BSCANP	G4	BSCANP
E10	P65/CS5#-A/CKE	E12	P65/CS5#/CKE
E11	P67/CS7#-A/DQM1	E13	P67/CS7#/DQM1/MTIOC7C/IRQ15
E12	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	E10	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN
E13	P66/CS6#-A/DQM0	E11	P66/CS6#/DQM0/MTIOC7D
F1	XCIN	F1	XCIN
F2	XCOUT	F2	XCOUT
F10	PA1/A1/MTIOC6B/PO17/SSLA2-B	F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11
F11	PA3/A3/MTIOC6D/PO19	F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS
F13	PA2/A2/MTIOC6C/PO18/SSLA3-B	F13	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B
G1	XTAL	G1	XTAL/P37
G4	MD0	G3	MD/FINED
G11	PA5/A5/MTIOC7B/PO21/RSPCKA-B	G10	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA
G12	PA6/A6/MTIOC8A/PO22/MOSIA-B	G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT
G13	PA4/A4/MTIOC7A/PO20/SSLA0-B	G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS
H1	EXTAL	H1	EXTAL/P36
H2	P34/MTIOC0A/TMCI3/PO12/SCK6-B/IRQ4-A/TRST#	J1	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
H4	RES#	G2	RES#
H10	PB0/A8/MTIOC9A/PO24	H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12
H11	P71/CS1#-B/ET_MDIO	H11	P71/A18/CS1#/ET0_MDIO
H12	PB1/A9/MTIOC9C/PO25	J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS

145pin TFLGA	RX62N	145pin TFLGA	RX65N
H13	PA7/A7/MTIOC8B/PO23/MISOA-B	H13	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL
J1	P33/MTIOC0D/PO11/CRX0/RxD6-B/IRQ3-A	J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS
J2	P27/CS7#-C/MTIOC2B/PO7/RSPCKB-A/SCK1/TCK	K1	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
J3	P35/NMI	H4	UPSEL/P35/NMI
J4	P32/MTIOC0C/PO10/RTCOUT/CTX0/TxD6-B/IRQ2-A	J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
J10	PB2/A10/MTIOC9B/MTCLKG-B/PO26	J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B
J11	PB4/A12/MTIOC10A/MTCLKE-B/PO28	J11	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B
J12	PB5/A13/MTIOC10C/MTCLKF-B/PO29	K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B
J13	P72/CS2#-B/ET_MDC	H10	P72/A19/CS2#/ET0_MDC
K1	P30/MTIOC4B-A/TMRI3/PO8/RxD1/MISOB-A/IRQ0/TDI	J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
K2	P24/CS4#-C/EDREQ1-B/USB0_VBUSEN-A/MTIOC4A-A/MTCLKA-A/TMRI1/PO4/SCK3-B	L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK
K3	P31/MTIOC4D-A/TMCI2-B/PO9/SSLB0-A/IRQ1/TMS	K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
K4	P26/CS6#-C/MTIOC2A/TMO1/PO6/MOSIB-A/TxD1/TDO	K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
K5	BCLK/P53	K6	P53/BCLK
K7	PC7/A23/CS0#-B/ET_COL/MTIC11U-A/MTCLKB-B/MISOA-A	N9	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14
K8	P82/EDREQ1-A/ET_ETXD1/RMII_TXD1/MTIOC4A-B/TRSYNC	N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET0_ETXD1/RMII0_TXD1/MMC_D4-A

145pin TFLGA	RX62N	145pin TFLGA	RX65N
K9	PC3/A19-A/ET_TX_ER/MTCLKF-A/TxD5	N11	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A
K10	PB7/A15/MTIOC10D/PO31	K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
K11	P73/CS3#-B/ET_WOL	L12	TRDATA4/P73/CS3#/PO16/ET0_WOL
K12	PC0/A16-A/ET_ERXD3/MTCLKG-A/SSLA1-A	M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
K13	PB3/A11/MTIOC9D/MTCLKH-B/PO27	J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B
L1	P25/CS5#-C/EDACK1-B/USB0_DPRPD/MTIOC4C-A/MTCLKB-A/PO5/RxD3-B/ADTRG0#-B	L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0#
L2	P22/EDREQ0-B/USB0_DRPD/MTIOC3B-A/MTCLKC-A/TMO0/PO2/SCK0	M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6
L3	P17/MTIOC3A/PO15/TxD3-A/IRQ7-B	M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1#
L4	P12/TMCI1-B/SCL0/RxD2-A/IRQ2-B	M4	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
L5	VCC_USB	M5	VCC_USB
L6	P56/EDACK1-C/MTIOC3C-B	L6	P56/EDACK1/MTIOC3C/TIOCA1
L7	P52/RD#/SSLB3-A/RxD2-B	L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
L8	P83/EDACK1-A/ET_CRS/RMII_CRS_DV/MTIOC4C-B/TRCLK	L8	TRCLK/P83/EDACK1/MTIOC4C/CTS10#/SS10#/ET0_CRS/RMII0_CRS_DV/SCK10
L9	P81/EDACK0-A/ET_ETXD0/RMII_TXD0/MTIOC3D-B/TRDATA1	M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET0_ETXD0/RMII0_TXD0/MMC_D3-A/SDHI_CD-A/QIO3-A
L10	P77/CS7#-B/ET_RX_ER/RMII_RX_ER	M10	TRDATA7/P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/ET0_RX_ER/RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A
L11	P75/CS5#-B/ET_ERXD0/RMII_RXD0	N12	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A
L13	PB6/A14/MTIOC10B/PO30	K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD

145pin TFLGA	RX62N	145pin TFLGA	RX65N
			1/RXD11/SMISO11/SSCL11/SDSI_D0-B
M1	P23/EDACK0-B/USB0_DPUPE-A/MTIOC3D-A/MTCLKD-A/PO3/TxD3-B	L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7
M2	P20/USB0_ID/MTIOC1A/TMRI0-B/PO0/SDA1/TxD0	N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8
M4	P15/MTIOC0B/TMCI2-A/PO13/SCK3-A/IRQ5-B	K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5
M5	P14/USB0_OVRCURA/USB0_DPUPE-B/TMRI2/IRQ4-B	N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
M6	VSS_USB	M6	VSS_USB
M7	P55/WAIT#-B/EDREQ0-C/ET_EXOUT/MTIOC4D-B/TRDATA3	N7	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10
M8	P50/WR0#/WR#/SSLB1-A/TxD2-B	M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
M9	PC6/A22/CS1#-C/ET_ETXD3/MTIC11V-A/MTCLKA-B/MOSIA-A	M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13
M10	P80/EDREQ0-A/ET_TX_EN/RMII_TXD_EN/MTIOC3B-B/TRDATA0	K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/QIO2-A
M11	PC2/A18-A/ET_RX_DV/MTCLKE-A/SSLA3-A/RxD5	L11	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/MMC_CD-A/SDHI_D3-A/SDSI_D3-A
M12	PC1/A17-A/ET_ERXD2/MTCLKH-A/SSLA2-A/SCK5	M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
N1	P21/USB0_EXICEN/MTIOC1B/TMCI0-B/PO1/SCL1/RxD0	N1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN//PIXD5/IRQ9
N2	P16/USB0_VBUS/USB0_OVRCURB/USB0_VBUSEN-B/MTIOC3C-A/TMO2/PO14/RxD3-A/IRQ6-B	L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
N4	P13/TMO3/SDA0/TxD2-A/IRQ3-B/ADTRG1#	L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
N5	USB0_DM	N5	USB0_DM

145pin TFLGA	RX62N	145pin TFLGA	RX65N
N6	USB0_DP	N6	USB0_DP
N7	P54/EDACK0-C/ET_LINKSTA/MTIOC4B-B/TRDATA2	K5	TRDATA2/P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA
N8	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
N10	PC5/A21/CS2#-C/WAIT#-C/ET_ETXD2/MTIC11W-A/MTCLKD-B/RSPCKA-A	L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/MMC_D5-A
N11	PC4/A20/CS3#-C/ET_TX_CLK/MTCLKC-B/SSLA0-A	L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A
N12	P76/CS6#-B/ET_RX_CLK/REF50CK	K10	TRDATA6/P76/CS6#/PO22/RXD11/SMISO11/SSCL11/ET0_RX_CLK/REF50CK0/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A
N13	P74/CS4#-B/ET_ERXD1/RMII_RXD1	N13	TRDATA5/P74/A20/CS4#/PO19/CTS11#/SS11#/ET0_ERXD1/RMII0_RXD1
G3	MD1	-	-
F3	WDTOVF#	-	-
F4	MDE	-	-
M3	PLLVCC	-	-
N3	PLLVSS	-	-
-	-	M13	VCC
-	-	N3	P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2
-	-	M3	P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1
-	-	K8	VCC
-	-	F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
-	-	F4	VBATT
-	-	E3	PJ5/POE8#/CTS2#/RTS2#/SS2#
-	-	D2	PF5/IRQ4
-	-	C1	AVSS1
-	-	B1	AVCC1
D2	VCC	B10	VCC

145pin TFLGA	RX62N	145pin TFLGA	RX65N
D5 D9 D11 F12 H3 L13 N9		D5 D11 G12 H2 K8 M13	
B9 C3 D6 D10 E2 G2 G10 K6 M13	VSS	A10 C6 C13 E1 F11 H3 L13 N8	VSS

3.3 100pin Package

Table 3.3 shows a Comparative Listing of Pin Functions (100pin Package).

Table 3.3 Comparative Listing of Pin Functions (100pin Package)

100pin	RX62N（LFQFP）	RX65N（LQFP）
1	VCC	AVCC1
2	EMLE	EMLE
3	VSS	AVSS1
4	MDE	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
5	VCL	VCL
6	MD1	VBATT
7	MD0	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL	P37/XTAL
12	VSS	VSS
13	EXTAL	P36/EXTAL
14	VCC	VCC
15	P35/NMI	P35/UPSEL/NMI
16	P34/MTIOC0A/TMCI3/PO12/SCK6/IRQ4-A/TRST#	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	P33/MTIOC0D/PO11/CRX0/RxD6/IRQ3-A	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS
18	P32/MTIOC0C/PO10/RTCOUT/CTX0/TxD6/IRQ2-A	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS
19	P31/MTIOC4D-A/TMCI2/PO9/SSLB0-A/IRQ1/TMS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	P30/MTIOC4B-A/TMRI3/PO8/RxD1/MISOB-A/IRQ0/TDI	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
21	P27/CS7#/MTIOC2B/PO7/RSPCKB-A/SCK1/TCK	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A

100pin	RX62N（LFQFP）	RX65N（LQFP）
22	P26/CS6#/MTIOC2A/TMO1/PO6/MOSIB-A/TxD1/TDO	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
23	P25/CS5#/USB0_DPRPD/MTIOC4C/MTCLKB-A/PO5/RxD3/ADTRG0#-B	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#
24	P24/CS4#/USB0_VBUSEN-A/MTIOC4A/MTCLKA-A/TMRI1/PO4/SCK3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN
25	P23/USB0_DPUPE-A/MTIOC3D/MTCLKD-A/PO3/TxD3	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3
26	P22/USB0_DRPD/MTIOC3B/MTCLKC-A/TMO0/PO2/SCK0	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB
27	P21/USB0_EXICEN/MTIOC1B/TMCI0/PO1/RxD0	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9
28	P20/USB0_ID/MTIOC1A/TMRI0/PO0/TxD0	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8
29	PLLVCC	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
30	P16/USB0_VBUS/USB0_OVRCURB/USB0_VBUSEN-B/MTIOC3C/TMO2/PO14/IRQ6-B	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
31	PLLVSS	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5
32	P14/USB0_OVRCURA/USB0_DPUPE-B/MTIOC3A/TMRI2/PO15/IRQ4-B	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
33	P13/MTIOC0B/TMO3/PO13/SDA0/TxD2-A/IRQ3-B/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
34	P12/TMCI1/SCL0/RxD2-A/IRQ2-B	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	USB0_DM
37	USB0_DP	USB0_DP
38	VSS_USB	VSS_USB

100pin	RX62N（LFQFP）	RX65N（LQFP）
39	P55/WAIT#-B//MTIOC4D-B	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10
40	P54/MTIOC4B-B	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA
41	BCLK/P53	P53/BCLK
42	P52/RD#/SSLB3-A/RxD2-B	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
43	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	P50/WR0#/WR#/SSLB1-A/TxD2-B	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
45	PC7/A23/CS0#/ET_COL/MTIC11U-A/MTCLKB-B/MISOA-A	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/IRQ14
46	PC6/A22/CS1#/ET_ETXD3/MTIC11V-A/MTCLKA-B/MOSIA-A	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/IRQ13
47	PC5/A21/CS2#/WAIT#-C/ET_ETXD2/MTIC11W-A/MTCLKD-B/RSPCKA-A	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10
48	PC4/A20/CS3#/ET_TX_CLK/MTCLKC-B/SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#
49	PC3/A19/ET_TX_ER/MTCLKF-A/TxD5	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	PC2/A18/ET_RX_DV/MTCLKE-A/SSLA3-A/RxD5	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV
51	PC1/A17/ET_ERXD2/MTCLKH-A/SSLA2-A/SCK5	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
52	PC0/A16/ET_ERXD3/MTCLKG-A/SSLA1-A	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	PB7/A15/ET_CRS/RMII_CRS_DV/MTIOC10D/PO31	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B

100pin	RX62N（LFQFP）	RX65N（LQFP）
54	PB6/A14/ET_ETXD1/RMII_TXD1/MTIOC10B/PO30	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
55	PB5/A13/ET_ETXD0/RMII_TXD0/MTIOC10C/MTCLKF-B/PO29	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B
56	PB4/A12/ET_TX_EN/RMII_TXD_EN/MTIOC10A/MTCLKE-B/PO28	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B
57	PB3/A11/ET_RX_ER/RMII_RX_ER/MTIOC9D/MTCLKH-B/PO27	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B
58	PB2/A10/ET_RX_CLK/REF50CK/MTIOC9B/MTCLKG-B/PO26	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B
59	PB1/A9/ET_ERXD0/RMII_RXD0/MTIOC9C/PO25	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS
60	VCC	VCC
61	PB0/A8/ET_ERXD1/RMII_RXD1/MTIOC9A/PO24	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12
62	VSS	VSS
63	PA7/A7/ET_WOL/MTIOC8B/PO23/MISOA-B	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL
64	PA6/A6/ET_EXOUT/MTIOC8A/PO22/MOSIA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT
65	PA5/A5/ET_LINKSTA/MTIOC7B/PO21/RSPCKA-B	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA
66	PA4/A4/ET_MDC/MTIOC7A/PO20/SSLA0-B	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS
67	PA3/A3/ET_MDIO/MTIOC6D/PO19	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS
68	PA2/A2/MTIOC6C/PO18/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B
69	PA1/A1/MTIOC6B/PO17/SSLA2-B	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11

100pin	RX62N（LFQFP）	RX65N（LQFP）
70	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN
71	PE7/D15/MISOB-B/IRQ7	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105
72	PE6/D14/MOSIB-B/IRQ6-A	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104
73	PE5/D13/RSPCKB-B/IRQ5	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103
74	PE4/D12/SSLB0-B	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102
75	PE3/D11/POE8#	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101
76	PE2/D10/POE9#/SSLB3-B	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100
77	PE1/D9/SSLB2-B	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1
78	PE0/D8/SSLB1-B	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0
79	PD7/D7/MTIC5U/POE0#	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107
80	PD6/D6/MTIC5V/POE1#	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106
81	PD5/D5/MTIC5W/POE2#	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113
82	PD4/D4/MTIC11U-B/POE3#	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112
83	PD3/D3/MTIC11V-B/POE4#	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111
84	PD2/D2/MTIC11W-B/POE5#	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110

100pin	RX62N（LFQFP）	RX65N（LQFP）
85	PD1/D1/POE6#	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109
86	PD0/D0/POE7#	PD0/D0[A0/D0]/POE4#/IRQ0/AN108
87	P47/IRQ15-B/AN7	P47/IRQ15-DS/AN007
88	P46/IRQ14/AN6	P46/IRQ14-DS/AN006
89	P45/IRQ13-B/AN5	P45/IRQ13-DS/AN005
90	P44/IRQ12/AN4	P44/IRQ12-DS/AN004
91	P43/IRQ11/AN3	P43/IRQ11-DS/AN003
92	P42/IRQ10/AN2	P42/IRQ10-DS/AN002
93	P41/IRQ9/AN1	P41/IRQ9-DS/AN001
94	VREFL	VREFL0
95	P40/IRQ8/AN0	P40/IRQ8-DS/AN000
96	VREFH	VREFH0
97	AVCC	AVCC0
98	P07/IRQ15-A/ADTRG0#-A	P07/IRQ15/ADTRG0#
99	AVSS	AVSS0
100	P05/DA1/IRQ13-A	P05/IRQ13/DA1

4. Notes on Migration

There are some notes about difference between RX62N Group and RX65N Group.

Description about the Hardware, there is on the < Chapter 4.1 Notes on Pin Design >.

Description about the Software, there is on the <Chapter 4.2 Notes on Function Setting>.

4.1 Notes on Pin Design

4.1.1 Operating modes

The Operating mode has difference between RX62N Group and RX65N Group.

On the RX65N Group, the chip starts up in boot mode (FINE interface) when the MD pin is set to the low level at the time of release from the reset state and then is then switched to the high level within 20 to 100 msec.

Table 4.1 Comparative Listing of Operating modes

RX62N			RX65N		
MD1	MD0	Operating modes	MD	UB	Operating modes
0	1	Boot mode	0	0	Boot mode（SCI Interface）
1	0	USB boot mode	0	1	Boot mode（USB Interface）
-	-	-	0->1	0	Boot mode（FINE Interface）
1	1	Single chip mode	1	-	Single chip mode

4.1.2 VCL Pin (External Capacitor)

Connect a smoothing capacitor rated at 0.22 μF to the VCL pin of the RX65N Group for stabilization of the internal power supply.

4.1.3 VBATT Pin

On the RX65N Group, when the voltage at the VCC pin is dropped, power can be supplied to the realtime clock (RTC) and sub-clock oscillator from the dedicated battery backup power pin (VBATT pin).

Connect the VBATT pin to the VCC pin when do not use the battery backup function or do not use Sub-clock oscillator with realtime-clock(RTC),.

4.1.4 Main Clock Oscillator

When connecting an oscillator to EXTAL pin and XTAL pin of RX65N Group, frequency should be in a range of 8 MHz to 24 MHz

On the RX65N Group, according to the frequency, it is necessary to set the driving ability in main clock oscillator driving ability 2 switching bits (MODRV2[1:0]) of main clock oscillator forced oscillation control register (MOFCR).

4.1.5 Inputting an External Clock

On the RX62N Group, it was permissible, when inputting an external clock, to input on the XTAL pin the reverse phase of the clock input on the EXTAL pin. However, this is not permitted on the RX65N Group. Please keep this in mind when designing systems.

On the RX65N Group, it is necessary to set the main clock oscillator switching bit (MOSEL) of main clock oscillator forced oscillation control register (MOFCR) to 1 when inputting an external clock.

4.1.6 Sub-Clock Oscillator

In the RX62N Group, a crystal oscillator and an external clock can be input to sub-clock.

However, in the RX65N Group, external can not be input to the sub-clock. Please use a crystal oscillator.

On the RX65N Group, according to the load capacitance of oscillator, it is necessary to set the driving capacity in sub-clock oscillator drive capacity control bits (RTCDV[2:0]) of RTC control register 3 (RCR3)

When designing a board using a low CL crystal unit, refer to the application note “Design Guide for Low CL Sub-clock Circuits” (R01AN1187EJ) to reduce the influence from noise..

4.1.7 Correspond to 32-bit Buses

On the RX65N Group does not have Data bidirectional pins (D16-D31).This means that the RX65N Group does not To correspond the Memory with 32-bit Bus width.

4.1.8 Analog Power Pin

There is difference to the Analog Power Pin Functions between RX62N Group and RX65N Group.

RX62N	AVCC	Analog power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	AVSS	Ground pin for the A/D and D/A converters. Connect this pin to the system power supply (0 V).
	VREFH	Reference power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply.
	VREFL	Reference ground pin for the A/D and D/A converters. Make sure to connect this pin to the analog reference power supply (0 V). When the A/D and D/A converters are not in use, connect this pin to the system power supply (0 V).
RX65N	AVCC0	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply.
	AVSS0	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply.
	VREFH0	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply.
	AVSS1	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply.

4.1.9 On-Chip USB DP/DM Pull-Up/Pull-Down Resistors

The RX65N Group has on-chip USB DP/DM pull-up and pull-down resistors. This means that the external connection circuits are different from those of the RX62N Group.

4.1.10 Transition to Boot Mode (USB Interface)

On the RX65N Group, an oscillator is usable in boot mode (USB interface) when its frequency is 20 or 24 MHz and when the setting value of the main clock oscillator driving ability 2 switching bits (MOFCR.MODRV2[1:0]) are 00b in the result of the matching test conducted by the oscillator manufacturer (the recommended setting value)..

4.1.11 Handling of Unused Pins

Indicates unused terminals that need attention when moving from RX62N Group to RX65N Group.

Table 4.2 Handling of Unused Pins

Pin Name	Handling	
	RX62N	RX65N
EMLE	Connect this pin to VSS via a resistor (pulling down).	Connect this pin to VSS via a resistor (pulling down).
BSCANP	Connect this pin to VSS via a resistor (pulling down).	Connect this pin to VSS via a resistor (pulling down).
MD	-	Use this as a mode pin.
MD1,MD0	Use this as a mode pin.	-
MDE	Use this as a mode pin.	-
RES#	Connect this pin to VCC via a resistor (pulling up).	Connect this pin to VCC via a resistor (pulling up).
VCC_USB	-	Connect this pin to VCC
VSS_USB	-	Connect this pin to VSS
USB0_DP	Keep these pins open	Keep these pins open
USB0_DM		
P35/NMI	Connect this pin to VCC via a resistor (pulling up).	Connect this pin to VCC via a resistor (pulling up).
EXTAL	Use this pin as a clock	Connect this pin to VSS via a resistor (pulling down).
XTAL	Keep this pin open	Keep this pin open
XCIN	Connect this pin to VCC via a resistor (pulling up) or connect to this to VSS via a resistor (pulling down).	Connect this pin to VSS via a resistor (pulling down).
XCOUT	Keep this pin open	Keep this pin open
Port 0 to 9, A to F, Port J	For each pin, connect to VCC via a resistor (pulled up) or connect to VSS via a resistor (pulled down) It is also possible to release the terminal with PORTn.ICR as the initial value (input buffer disabled).	If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2
VREFH0	Connect this pin to AVCC.	Connect this pin to AVCC0.
VREFL0	Connect this pin to AVSS.	Connect this pin to AVSS0.

Note 1. Clear the PORTn.PMR bit, the PmnPFS.ISEL bit and the PmnPFS.ASEL bit to 0.

Note 2. In the case of release when the setting is for output, the port is an input over the period from release from the reset state to the pin becoming an output. Since the voltage on the pin is undefined while it is an input, this may lead to an increase in the current drawn.

4.2 Notes on Function Settings

4.2.1 Notes on Using Power-On Reset and PLL Circuit Together

On the RX65N Group, when using a power-on reset and the PLL circuit together, set the LVD1CR1.LVD1IDTSEL[1:0] bits or LVD2CR1.LVD2IDTSEL[1:0] bits to 01b, and select the voltage monitoring interrupt to be generated when a drop (Vcc < Vdet) is detected.
In addition, at the beginning of the interrupt handling routine, set the SCKCR3.CKSEL[2:0] bits to a value other than 100b to select a clock source other than the PLL circuit, then set the PLLCR2.PLLEN bit to 1 to stop the PLL circuit.

4.2.2 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting

On the RX65N Group, when reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 as the value for all bits of reserved areas and all reserved bits. Normal operation cannot be guaranteed if 0 is written to such bits.

4.2.3 Control of Sub-clock oscillator

In the RX65N Group, the operation / stop of the sub-clock oscillator is controlled by the SOSCCR.SOSTP bit and RCR3.RTCEN, and if any bit is set to operate, the sub-clock oscillator is put into operation.

The sub-clock may be used when used as a main-clock, when used as a count source for realtime-clock or both. Therefore, please keep in mind that there are restrictions on setting, including not using the sub-clock.

4.2.4 Rewriting the Register by DMAC and DTC in Sleep Mode

On the RX65N Group, the WDT stops in sleep mode. Do not set up the DMACA and DTC to rewrite any registers related to the WDT while the chip is in sleep mode.

According to the settings of the OFS0.IWDTSLCSTP bit and IWDTCSTPR.SLCSTP bit, the IWDT may also stop in sleep mode. If that is the case, do not set up the DMAC and DTC to rewrite any registers related to the IWDT in sleep mode.

The RSTCKCR register can be set so that the clock source is switched on recovery from sleep mode. For this reason, rewriting the register while the chip is in sleep mode may lead to unintended operation, so do not allow rewriting of the RSTCKCR register in sleep mode.

4.2.5 Setting value of the Port Direction Register(PDR) for each packeges

In the RX65N Group, the initialization of the reserved bits of the Port Direction Register(PDR),, refer to the User's Manual <Chapter 22.4 Initialization of the Port Direction Register>

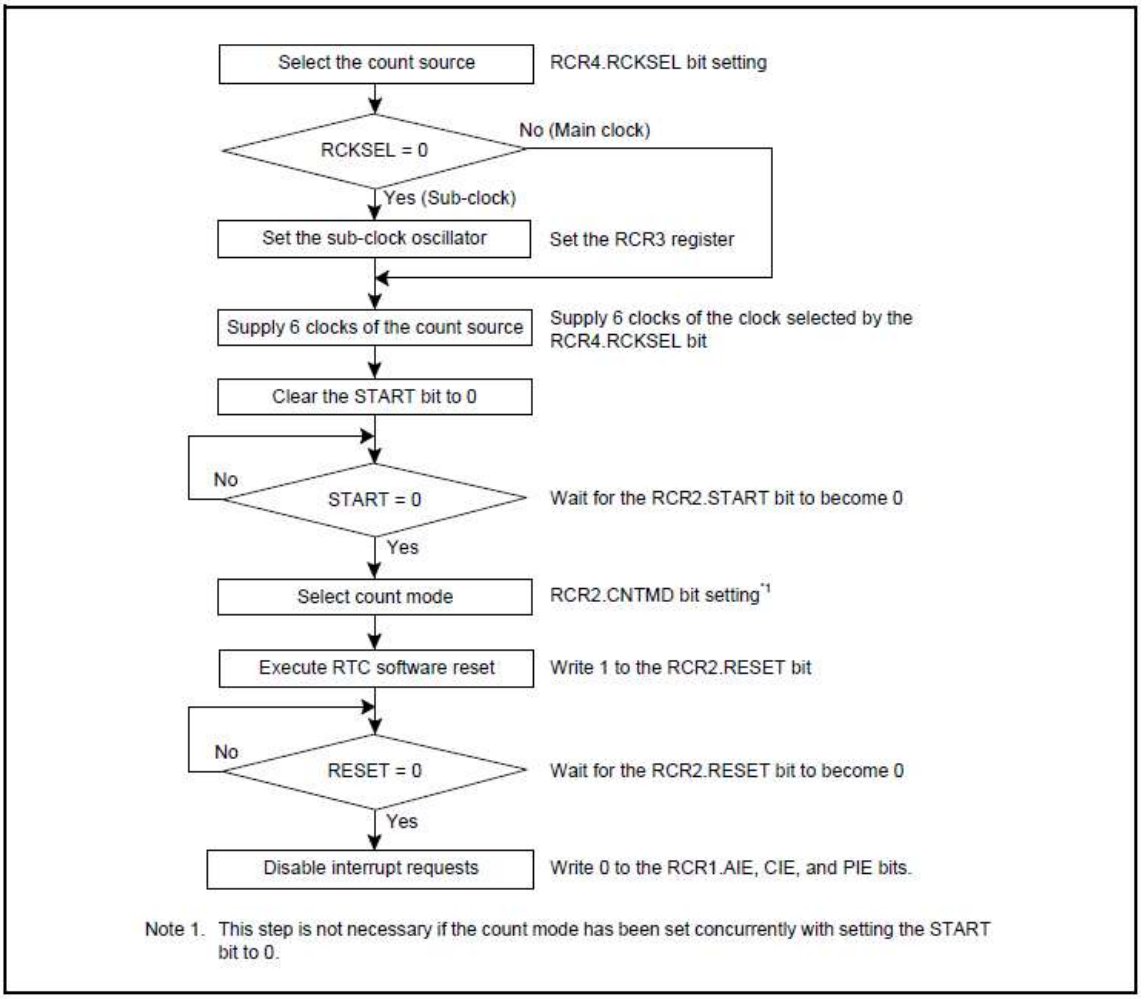
4.2.6 Initialization Procedure When the Realtime Clock is Not to be Used

On the RX65N Group, registers in the RTC are not initialized by a reset. Accordingly, depending on the initial state, the generation of an unintentional interrupt request or operation of the counter may lead to increased power consumption.

For products that do not require a realtime clock, initialize the registers.

Alternatively, when the sub-clock is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (sub-clock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock.

When making the setting to stop the sub-clock, write 0 to the RCR3.RTCEN bit and write 1 to the SOSCCR.SOSTP bit.



4.2.7 Note on Transmit Enable Bit (TE Bit)

On the RX65N Group, when setting the SCR.TE bit to 0 (serial transmission is disabled) while the pin function is “TXDn”, output of the pin becomes high impedance.

Prevent the TXDn line from becoming high impedance by any of the following ways:

(1) Connect a pull-up resistor to the TXDn line.

(2) Change the pin function to “general-purpose I/O port, output” before setting the SCR.TE bit to 0.

Set the SCR.TE bit to 1 before changing the pin function to “TXDn”.

4.2.8 RSPI Notes on Starting Transfer

On the RX65N Group, if the ICU.IRn.IR flag is 1 at the time transfer is to be started, an interrupt request is internally retained after transfer starts, and this can lead to unanticipated behavior of the ICU.IRn.IR flag.

When the ICU.IRn.IR flag is 1 at the time transfer is to start, to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1).

4.2.9 S12AD A/D Conversion Restarting Timing and Termination Timing

On the RX65N Group, it takes a maximum of six ADCLK(in case of RX62N Group, it takes three cycles) cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADCSR.ADST bit to 1. It takes a maximum of two ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADCSR.ADST bit to 0.

4.2.10 S12AD Pin Setting When Using the 12-bit A/D Converter

When using the 12-bit A/D converter unit 0, do not use the P40 to P47, P03, P05, and P07 pins as output pins. We also recommend not using the P00 to P02, P90 to P930, PD0 to PD7, and PE0 to PE7 pins as output pins. If any of the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins is used for an output pin, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

When using the 12-bit A/D conversion unit1, we recommend not using the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins as output pins. If any of the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins is used for an output pins, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

4.2.11 S12AD Caution When Using an External Bus

On the RX65N Group, A/D conversion at the same time as access to an external bus may produce poor results.

In this case, use a software approach, such as performing A/D conversion several times, then obtaining the average after excluding the highest and lowest values.

4.2.12 Note on Usage When Measure against Interference between D/A and A/D Conversion is Enabled

On the RX65N Group, when the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), do not place the 12-bit A/D converter (unit 1) in the module stop state. It may halt D/A conversion in addition to A/D conversion.

4.2.13 D/A Note on Event Link Operation

On the RX65N Group, when the event link function is used, do not use output buffer amplifier.

4.2.14 Initial Setting Procedure when the Output Buffer Amplifier is Used

On the RX65N Group, when using the output buffer amplifier, enable the amplifier output in the following procedure .An example for channel 0 is described below.

(1) Confirm that the DACR.DAE and DACR.DAE0 bits are 0.

(2) Write 0000h to the DACR0 register.

(3) Set the DAA.SWCR.DAASW0 bit to 1.

(4) Set the DAA.SWCR.DAAMP0 bit to 1.

(5) Set the DACR.DAE or DACR.DAOE0 bit to 1. The output buffer amplifier starts the operation.

(6) Wait for at least 3 μ s and then set the DAAWCR.DAASW0 bit to 0.

(7) Write a value to be converted in the DADR0 register.

While the output buffer amplifier is operating, setting the DACR.DAE and DACR.DAOE bits to 0 disables the output buffer amplifier. Repeat the procedure from (1) to (7) to use the output buffer amplifier again.

4.2.15 Supplementary explanation on RAM self-test

On the RX65N Group, when a value is written to RAM and then execute a read access to the same address, the value may be read from the buffer, not from the RAM.

Perform the following operation to ensure that a value will be read from RAM.
To read RAM data at an address of 4-aligned bytes (*) after writing a value to the RAM address of the same 4-aligned bytes:

Write a value to any other RAM address which is out of the 4-aligned bytes, and then execute a read access to the RAM address where you want to read.

4.2.16 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.3 shows The Number of Flash Memory Access Wait States.

Table 4.3 The Number of Flash Memory Access Wait States

Item	ICLK ≤ 50 MHz	50 MHz < ICLK ≤ 100 MHz	100 MHz < ICLK ≤ 200 MHz
Wait states	0 to 2	1 or 2	2

4.2.17 Transferring Firmware to the FCU RAM

On the RX62N Group, FCU commands could only be used if the FCU RAM holds the firmware for the FCU. However, this is not necessary on the RX65N Group.

4.2.18 Command of Flash Memory Usage

On the RX62N Group, the Flash memory can be programmed or erased by issuing FCU commands to FCU.

On the RX65N Group, the Flash memory can be programmed or erased by setting the FACI commands specified in the FACI command issuing area and by controlling the FCU.

エラー! 参照元が見つかりません。 shows エラー! 参照元が見つかりません。

Table 4.4 The Specification Comparison Between FCU Commands and FACI Commands

Item	FCU Commands (RX62N)	FACI commands (RX65N)
Command issuing area	Address for programming/erasure (00E0 0000h to 00FF FFFFh)	FACI command issuing area (007E 0000h)
Available commands	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Lock bit programming • Blank checking	• Program • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Configuration setting

4.2.19 Note of ID Code Protection

On the RX62N Group, when the control code is 52h and the ID code is 50h, 72h, 6Fh, 74h,65h, 63h, 74h, FFh, ..., FFh (from the ID code 1 field), there is no determination of matching and the ID code is always considered to be non-matching. Accordingly, reading, programming, and erasure from the host are prohibited.

On the RX65N Group, when the On-Chip Debugger is connected, the ID Code is authenticated regardless of the setting of SPCC.SPE.

For details of ID code authentication operation please refer to RENESAS TECHINICAL UPDATE（TN-RX*-A166A/E）

5. Reference Documents

User's Manual: Hardware

RX62N Group User's Manual: Hardware Rev.1.40 (R01UH0033EJ0140)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface Rev.1.00 (R01UH0602EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates.

- TN-RX*-A165A/E
- TN-RX*-A166A/E
- TN-RX*-A173A/E
- TN-RX*-A174A/E
- TN-RX*-A176A/E

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jul. 01, 2017	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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