
RL78/F15

R01AN3348EJ0100

Pin assignment of RL78/F15 by model

Rev.1.00

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Introduction

This application note describes pin assignment of each model of the RL78/F15 microcontrollers.

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1. Product grouping definition

Table1.1 shows the product list of RL78F15. The following table show figures and tables to refer to pin configuration and pin assignment for each product.

Table1.1 Products list of RL78/F15

Pin count	Model name	Pin configuration	Pin assignment
144 pins	R5F113TG, R5F113TH, R5F113TJ, R5F113TK, R5F113TL	Figure 2.1	Table 2.1
100 pins	R5F113PG, R5F113PH, R5F113PJ, R5F113PK, R5F113PL	Figure 2.2	Table 2.2
80 pins	R5F113MK, R5F113ML	Figure 2.3	Table 2.3
64 pins	R5F113LK, R5F113LL	Figure 2.4	Table 2.4
48 pins	R5F113GK, R5F113GL	Figure 2.5	Table 2.5

2. RL78/F15 products pin assignment

The pin configuration and pin assignment for products of RL78/F15 are illustrated and listed according to the number of pins included.

2.1 Products (144 pins) of RL78/F15

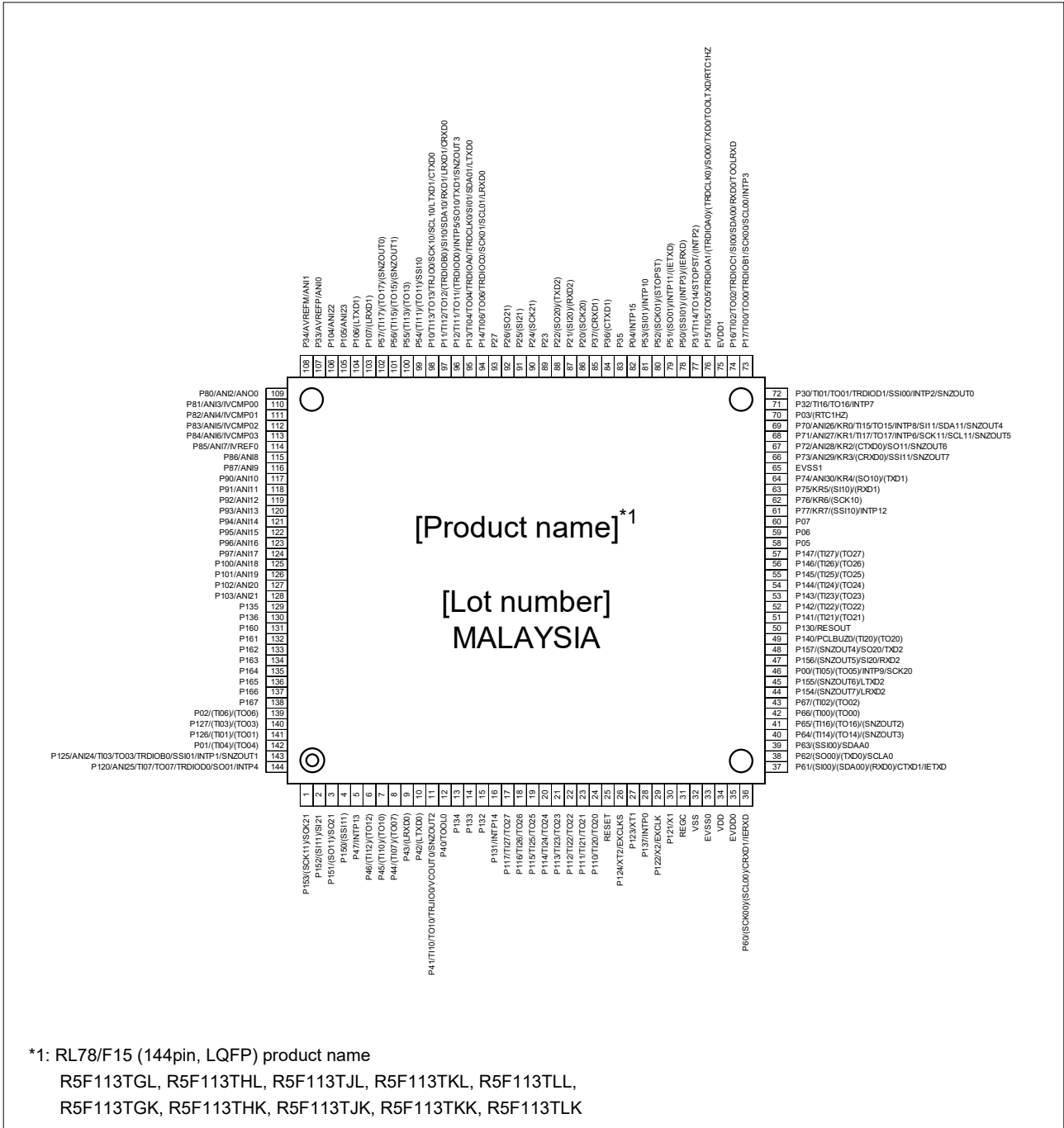


Figure 2.1 Pin configuration for RL78F15 products (144 pins)

Table 2.1 Pin assignment for RL78F15 products (144 pins) (1/3)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
1		P153			(SCK11)/SCK21		
2		P152			(SI11)/SI21		
3		P151			(SO11)/SO21		
4		P150			(SSI11)		
5		P47				INTP13	
6		P46		(TI12)/(TO12)			
7		P45		(TI10)/(TO10)			
8		P44		(TI07)/(TO07)			
9		P43			(LRXD0)		
10		P42			(LTXD0)		
11		P41	VCOU0	TI10/TO10/TRJIO0			SNZOUT2
12	TOOL0	P40					
13		P134					
14		P133					
15		P132					
16		P131				INTP14	
17		P117		TI27/TO27			
18		P116		TI26/TO26			
19		P115		TI25/TO25			
20		P114		TI24/TO24			
21		P113		TI23/TO23			
22		P112		TI22/TO22			
23		P111		TI21/TO21			
24		P110		TI20/TO20			
25	RESET						
26	XT2/EXCLKS	P124					
27	XT1	P123					
28		P137				INTP0	
29	X2/EXCLK	P122					
30	X1	P121					
31	REGC						
32	VSS						
33	EVSS0						
34	VDD						
35	EVDD0						
36		P60			(SCK00)/(SCL00)/CRXD1/IERXD		
37		P61			(SI00)/(SDA00)/(RXD0)/ CTXD1/IETXD		
38		P62			(SO00)/(TXD0)/SCLA0		
39		P63			(SSI00)/SDAA0		
40		P64		(TI14)/(TO14)			(SNZOUT3)
41		P65		(TI16)/(TO16)			(SNZOUT2)
42		P66		(TI00)/(TO00)			
43		P67		(TI02)/(TO02)			
44		P154			LRXD2		(SNZOUT7)
45		P155			LTXD2		(SNZOUT6)
46		P00		(TI05)/(TO05)	SCK20	INTP9	
47		P156			SI20/RXD2		(SNZOUT5)
48		P157			SO20/TXD2		(SNZOUT4)
49		P140		(TI20)/(TO20)			PCLBUZ0
50		P130					RESOUT
51		P141		(TI21)/(TO21)			
52		P142		(TI22)/(TO22)			
53		P143		(TI23)/(TO23)			
54		P144		(TI24)/(TO24)			
55		P145		(TI25)/(TO25)			
56		P146		(TI26)/(TO26)			
57		P147		(TI27)/(TO27)			
58		P05					
59		P06					
60		P07					

Table 2.1 Pin assignment for RL78F15 products (144 pins) (2/3)

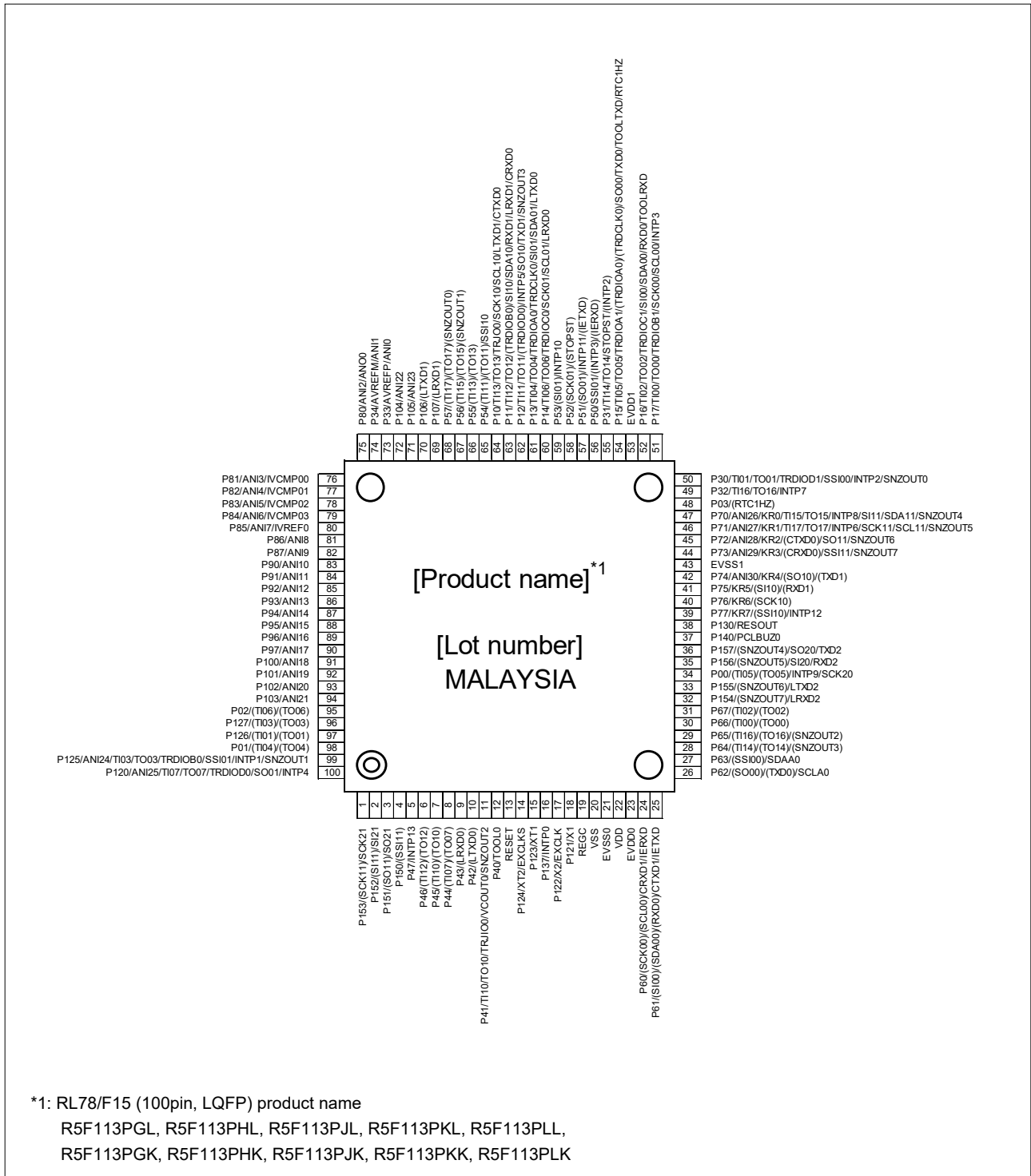
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
61		P77			(SSI10)	INTP12/KR7	
62		P76			(SCK10)	KR6	
63		P75			(SI10)/(RXD1)	KR5	
64		P74	ANI30		(SO10)/(TXD1)	KR4	
65	EVSS1						
66		P73	ANI29		(CRXD0)/SSI11	KR3	SNZOUT7
67		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
68		P71	ANI27	TI17/TO17	SCK11/SCL11	INTP6/KR1	SNZOUT5
69		P70	ANI26	TI15/TO15	SI11/SDA11	INTP8/KR0	SNZOUT4
70		P03					(RTC1HZ)
71		P32		TI16/TO16		INTP7	
72		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
73		P17		TI00/TO00/TRDI0B1	SCK00/SCL00	INTP3	
74		P16		TI02/TO02/TRDI0C1	SI00/SDA00/RXD0		TOOLRXD
75	EVDD1						
76		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/ RTC1HZ
77		P31		TI14/TO14		(INTP2)	STOPST
78		P50			(SSI01)/(IERXD)	(INTP3)	
79		P51			(SO01)/(IETXD)	INTP11	
80		P52			(SCK01)		(STOPST)
81		P53			(SI01)	INTP10	
82		P04				INTP15	
83		P35					
84		P36			(CTXD1)		
85		P37			(CRXD1)		
86		P20			(SCK20)		
87		P21			(SI20)/(RXD2)		
88		P22			(SO20)/(TXD2)		
89		P23					
90		P24			(SCK21)		
91		P25			(SI21)		
92		P26			(SO21)		
93		P27					
94		P14		TI06/TO06/TRDI0C0	SCK01/SCL01/LRXD0		
95		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
96		P12		TI11/TO11/(TRDI0D0)	SO10/TXD1	INTP5	SNZOUT3
97		P11		TI12/TO12/(TRDI0B0)	SI10/SDA10/RXD1/ LRXD1/CRXD0		
98		P10		TI13/TO13/TRJ00	SCK10/SCL10/LTXD1/ CTXD0		
99		P54		(TI11)/(TO11)	SSI10		
100		P55		(TI13)/(TO13)			
101		P56		(TI15)/(TO15)			(SNZOUT1)
102		P57		(TI17)/(TO17)			(SNZOUT0)
103		P107			(LRXD1)		
104		P106			(LTXD1)		
105		P105	ANI23				
106		P104	ANI22				
107		P33	AVREFP/ANI0				
108		P34	AVREFM/ANI1				
109		P80	ANI2/ANO0				
110		P81	ANI3/IVCMP00				
111		P82	ANI4/IVCMP01				
112		P83	ANI5/IVCMP02				
113		P84	ANI6/IVCMP03				
114		P85	ANI7/IVREF0				
115		P86	ANI8				
116		P87	ANI9				
117		P90	ANI10				
118		P91	ANI11				
119		P92	ANI12				
120		P93	ANI13				

Table 2.1 Pin assignment for RL78F15 products (144 pins) (3/3)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
121		P94	ANI14				
122		P95	ANI15				
123		P96	ANI16				
124		P97	ANI17				
125		P100	ANI18				
126		P101	ANI19				
127		P102	ANI20				
128		P103	ANI21				
129		P135					
130		P136					
131		P160					
132		P161					
133		P162					
134		P163					
135		P164					
136		P165					
137		P166					
138		P167					
139		P02		(TI06)/(TO06)			
140		P127		(TI03)/(TO03)			
141		P126		(TI01)/(TO01)			
142		P01		(TI04)/(TO04)			
143		P125	ANI24	TI03/TO03/TRDI0B0	SSI01	INTP1	SNZOUT1
144		P120	ANI25	TI07/TO07/TRDI0D0	SO01	INTP4	

- Cautions
1. Shaded functions are allocated as the multiple pins.
 Functions in parentheses are not assigned after reset release.
 Functions in parentheses can be assigned via settings in the PIORx registers.
 2. Only the STOPST function can be assigned via settings in the STPSTC register.

2.2 Products (100 pins) of RL78/F15



*1: RL78/F15 (100pin, LQFP) product name
R5F113PGL, R5F113PHL, R5F113PJL, R5F113PKL, R5F113PLL,
R5F113PGK, R5F113PHK, R5F113PJK, R5F113PKK, R5F113PLK

Figure 2.2 Pin configuration for RL78F15 products (100 pins)

Table 2.2 Pin assignment for RL78F15 products (100 pins) (1/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
1		P153			(SCK11)/SCK21		
2		P152			(SI11)/SI21		
3		P151			(SO11)/SO21		
4		P150			(SSI11)		
5		P47				INTP13	
6		P46		(TI12)/(TO12)			
7		P45		(TI10)/(TO10)			
8		P44		(TI07)/(TO07)			
9		P43			(LRXD0)		
10		P42			(LTXD0)		
11		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
12	TOOL0	P40					
13	RESET						
14	XT2/EXCLKS	P124					
15	XT1	P123					
16		P137				INTP0	
17	X2/EXCLK	P122					
18	X1	P121					
19	REGC						
20	VSS						
21	EVSS0						
22	VDD						
23	EVDD0						
24		P60			(SCK00)/(SCL00)/CRXD1 /IERXD		
25		P61			(SI00)/(SDA00)/(RXD0)/ CTXD1/IETXD		
26		P62			(SO00)/(TXD0)/SCLA0		
27		P63			(SSI00)/SDAA0		
28		P64		(TI14)/(TO14)			(SNZOUT3)
29		P65		(TI16)/(TO16)			(SNZOUT2)
30		P66		(TI00)/(TO00)			
31		P67		(TI02)/(TO02)			
32		P154			LRXD2		(SNZOUT7)
33		P155			LTXD2		(SNZOUT6)
34		P00		(TI05)/(TO05)	SCK20	INTP9	
35		P156			SI20/RXD2		(SNZOUT5)
36		P157			SO20/TXD2		(SNZOUT4)
37		P140					PCLBUZ0
38		P130					RESOUT
39		P77			(SSI10)	INTP12/KR7	
40		P76			(SCK10)	KR6	
41		P75			(SI10)/(RXD1)	KR5	
42		P74	ANI30		(SO10)/(TXD1)	KR4	
43	EVSS1						
44		P73	ANI29		(CRXD0)/SSI11	KR3	SNZOUT7
45		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
46		P71	ANI27	TI17/TO17	SCK11/SCL11	INTP6/KR1	SNZOUT5
47		P70	ANI26	TI15/TO15	SI11/SDA11	INTP8/KR0	SNZOUT4
48		P03					(RTC1HZ)
49		P32		TI16/TO16		INTP7	
50		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
51		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
52		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
53	EVDD1						
54		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/ RTC1HZ
55		P31		TI14/TO14		(INTP2)	STOPST
56		P50			(SSI01)/(IERXD)	(INTP3)	
57		P51			(SO01)/(IETXD)	INTP11	

Table 2.2 Pin assignment for RL78F15 products (100 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
58		P52			(SCK01)		(STOPST)
59		P53			(SI01)	INTP10	
60		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
61		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
62		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
63		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/ LRXD1/CRXD0		
64		P10		TI13/TO13/TRJO0	SCK10/SCL10/LTXD1/ CTXD0		
65		P54		(TI11)/(TO11)	SSI10		
66		P55		(TI13)/(TO13)			
67		P56		(TI15)/(TO15)			(SNZOUT1)
68		P57		(TI17)/(TO17)			(SNZOUT0)
69		P107			(LRXD1)		
70		P106			(LTXD1)		
71		P105	ANI23				
72		P104	ANI22				
73		P33	AVREFP/ANI0				
74		P34	AVREFM/ANI1				
75		P80	ANI2/ANO0				
76		P81	ANI3/IVCMP00				
77		P82	ANI4/IVCMP01				
78		P83	ANI5/IVCMP02				
79		P84	ANI6/IVCMP03				
80		P85	ANI7/IVREF0				
81		P86	ANI8				
82		P87	ANI9				
83		P90	ANI10				
84		P91	ANI11				
85		P92	ANI12				
86		P93	ANI13				
87		P94	ANI14				
88		P95	ANI15				
89		P96	ANI16				
90		P97	ANI17				
91		P100	ANI18				
92		P101	ANI19				
93		P102	ANI20				
94		P103	ANI21				
95		P02		(TI06)/(TO06)			
96		P127		(TI03)/(TO03)			
97		P126		(TI01)/(TO01)			
98		P01		(TI04)/(TO04)			
99		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1
100		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	

- Cautions
1. Shaded functions are allocated as the multiple pins.
Functions in parentheses are not assigned after reset release.
Functions in parentheses can be assigned via settings in the PIORx registers.
 2. Only the STOPST function can be assigned via settings in the STPSTC register.

2.3 Products (80 pins) of RL78/F15

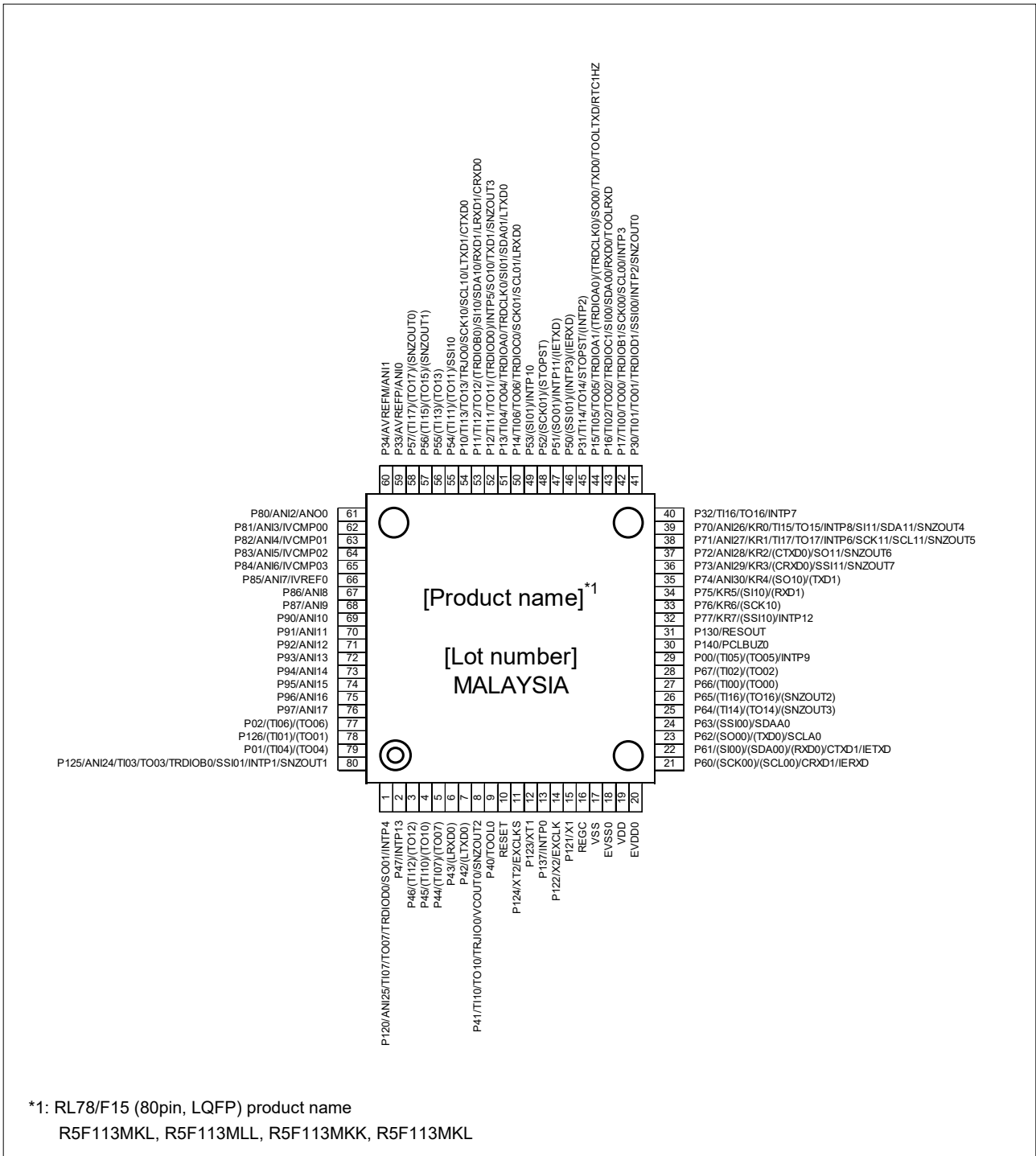


Figure 2.3 Pin configuration for RL78F15 products (80 pins)

Table 2.3 Pin assignment for RL78F15 products (80 pins) (1/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P47				INTP13	
3		P46		(TI12)/(TO12)			
4		P45		(TI10)/(TO10)			
5		P44		(TI07)/(TO07)			
6		P43			(LRXD0)		
7		P42			(LTXD0)		
8		P41	VCOU0	TI10/TO10/TRJIO0			SNZOUT2
9	TOOL0	P40					
10	RESET						
11	XT2/EXCLKS	P124					
12	XT1	P123					
13		P137				INTP0	
14	X2/EXCLK	P122					
15	X1	P121					
16	REGC						
17	VSS						
18	EVSS0						
19	VDD						
20	EVDD0						
21		P60			(SCK00)/(SCL00)/CRXD1/ IERXD		
22		P61			(SI00)/(SDA00)/(RXD0)/ CTXD1/IETXD		
23		P62			(SO00)/(TXD0)/SCLA0		
24		P63			(SSI00)/SDAA0		
25		P64		(TI14)/(TO14)			(SNZOUT3)
26		P65		(TI16)/(TO16)			(SNZOUT2)
27		P66		(TI00)/(TO00)			
28		P67		(TI02)/(TO02)			
29		P00		(TI05)/(TO05)		INTP9	
30		P140					PCLBUZ0
31		P130					RESOUT
32		P77			(SSI10)	KR7/INTP12	
33		P76			(SCK10)	KR6	
34		P75			(SI10)/(RXD1)	KR5	
35		P74	ANI30		(SO10)/(TXD1)	KR4	
36		P73	ANI29		(CRXD0)/SSI11	KR3	SNZOUT7
37		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
38		P71	ANI27	TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
39		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
40		P32		TI16/TO16		INTP7	
41		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
42		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
43		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
44		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/ RTC1HZ
45		P31		TI14/TO14		(INTP2)	STOPST
46		P50			(SSI01)/(IERXD)	(INTP3)	
47		P51			(SO01)/(IETXD)	INTP11	
48		P52			(SCK01)		(STOPST)
49		P53			(SI01)	INTP10	
50		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
51		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
52		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
53		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/ LRXD1/CRXD0		
54		P10		TI13/TO13/TRJO0	SCK10/SCL10/LTXD1/ CTXD0		
55		P54		(TI11)/(TO11)	SSI10		
56		P55		(TI13)/(TO13)			

Table 2.3 Pin assignment for RL78F15 products (80 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
57		P56		(TI15)/(TO15)			(SNZOUT1)
58		P57		(TI17)/(TO17)			(SNZOUT0)
59		P33	AVREFP/ANI0				
60		P34	AVREFM/ANI1				
61		P80	ANI2/AN00				
62		P81	ANI3/IVCMP00				
63		P82	ANI4/IVCMP01				
64		P83	ANI5/IVCMP02				
65		P84	ANI6/IVCMP03				
66		P85	ANI7/IVREF0				
67		P86	ANI8				
68		P87	ANI9				
69		P90	ANI10				
70		P91	ANI11				
71		P92	ANI12				
72		P93	ANI13				
73		P94	ANI14				
74		P95	ANI15				
75		P96	ANI16				
76		P97	ANI17				
77		P02		(TI06)/(TO06)			
78		P126		(TI01)/(TO01)			
79		P01		(TI04)/(TO04)			
80		P125	ANI24	TI03/TO03/TRDI0B0	SSI01	INTP1	SNZOUT1

- Cautions
1. Shaded functions are allocated as the multiple pins.
 Functions in parentheses are not assigned after reset release.
 Functions in parentheses can be assigned via settings in the PIORx registers.
 2. Only the STOPST function can be assigned via settings in the STPSTC register.

2.4 Products (64 pins) of RL78/F15

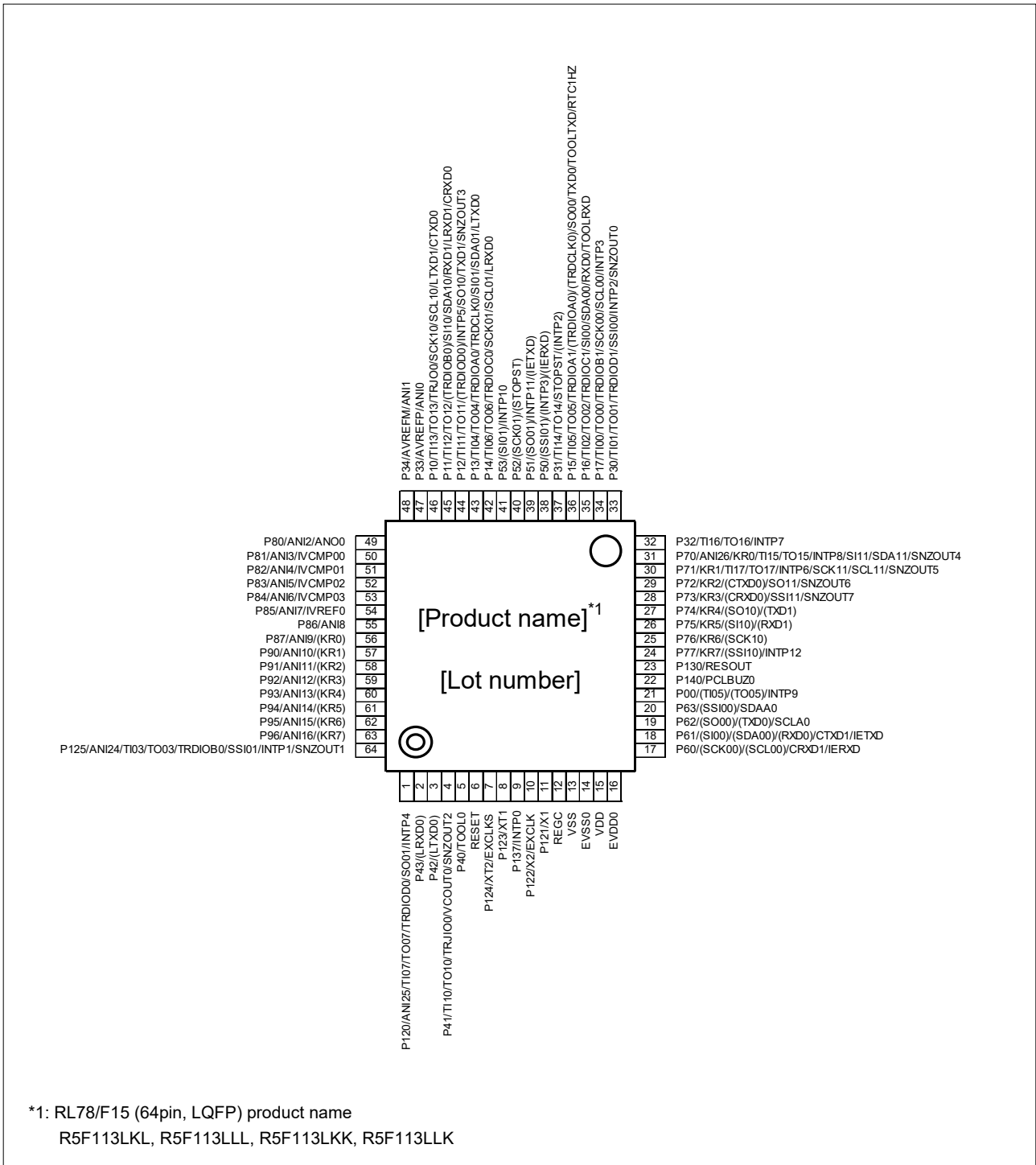


Figure 2.4 Pin configuration for RL78F15 products (64 pins)

Table 2.4 Pin assignment for RL78F15 products (64 pins) (1/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P43			(LRXD0)		
3		P42			(LTXD0)		
4		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
5	TOOL0	P40					
6	RESET						
7	XT2/EXCLKS	P124					
8	XT1	P123					
9		P137				INTP0	
10	X2/EXCLK	P122					
11	X1	P121					
12	REGC						
13	VSS						
14	EVSS0						
15	VDD						
16	EVDD0						
17		P60			(SCK00)/(SCL00)/CRXD1/ IERXD		
18		P61			(SI00)/(SDA00)/(RXD0)/ CTXD1/IETXD		
19		P62			(SO00)/(TXD0)/SCLA0		
20		P63			(SSI00)/SDAA0		
21		P00		(TI05)/(TO05)		INTP9	
22		P140					PCLBUZ0
23		P130					RESOUT
24		P77			(SSI10)	KR7/INTP12	
25		P76			(SCK10)	KR6	
26		P75			(SI10)/(RXD1)	KR5	
27		P74			(SO10)/(TXD1)	KR4	
28		P73			(CRXD0)/SSI11	KR3	SNZOUT7
29		P72			(CTXD0)/SO11	KR2	SNZOUT6
30		P71		TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
31		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
32		P32		TI16/TO16		INTP7	
33		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
34		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
35		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
36		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/ RTC1HZ
37		P31		TI14/TO14		(INTP2)	STOPST
38		P50			(SSI01)/(IERXD)	(INTP3)	
39		P51			(SO01)/(IETXD)	INTP11	
40		P52			(SCK01)		(STOPST)
41		P53			(SI01)	INTP10	
42		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
43		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
44		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
45		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/ LRXD1/CRXD0		
46		P10		TI13/TO13/TRJIO0	SCK10/SCL10/LTXD1/ CTXD0		
47		P33	AVREFP/ANI0				
48		P34	AVREFM/ANI1				
49		P80	ANI2/AN00				
50		P81	ANI3/IVCMP00				
51		P82	ANI4/IVCMP01				
52		P83	ANI5/IVCMP02				
53		P84	ANI6/IVCMP03				
54		P85	ANI7/IVREF0				
55		P86	ANI8				

Table 2.4 Pin assignment for RL78F15 products (64 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
56		P87	ANI9			(KR0)	
57		P90	ANI10			(KR1)	
58		P91	ANI11			(KR2)	
59		P92	ANI12			(KR3)	
60		P93	ANI13			(KR4)	
61		P94	ANI14			(KR5)	
62		P95	ANI15			(KR6)	
63		P96	ANI16			(KR7)	
64		P125	ANI24	TI03/TO03/TRDI0B0	SSI01	INTP1	SNZOUT1

- Cautions
1. Shaded functions are allocated as the multiple pins.
 Functions in parentheses are not assigned after reset release.
 Functions in parentheses can be assigned via settings in the PIORx registers.
 2. Only the STOPST function can be assigned via settings in the STPSTC register.

2.5 Products (48 pins) of RL78/F15

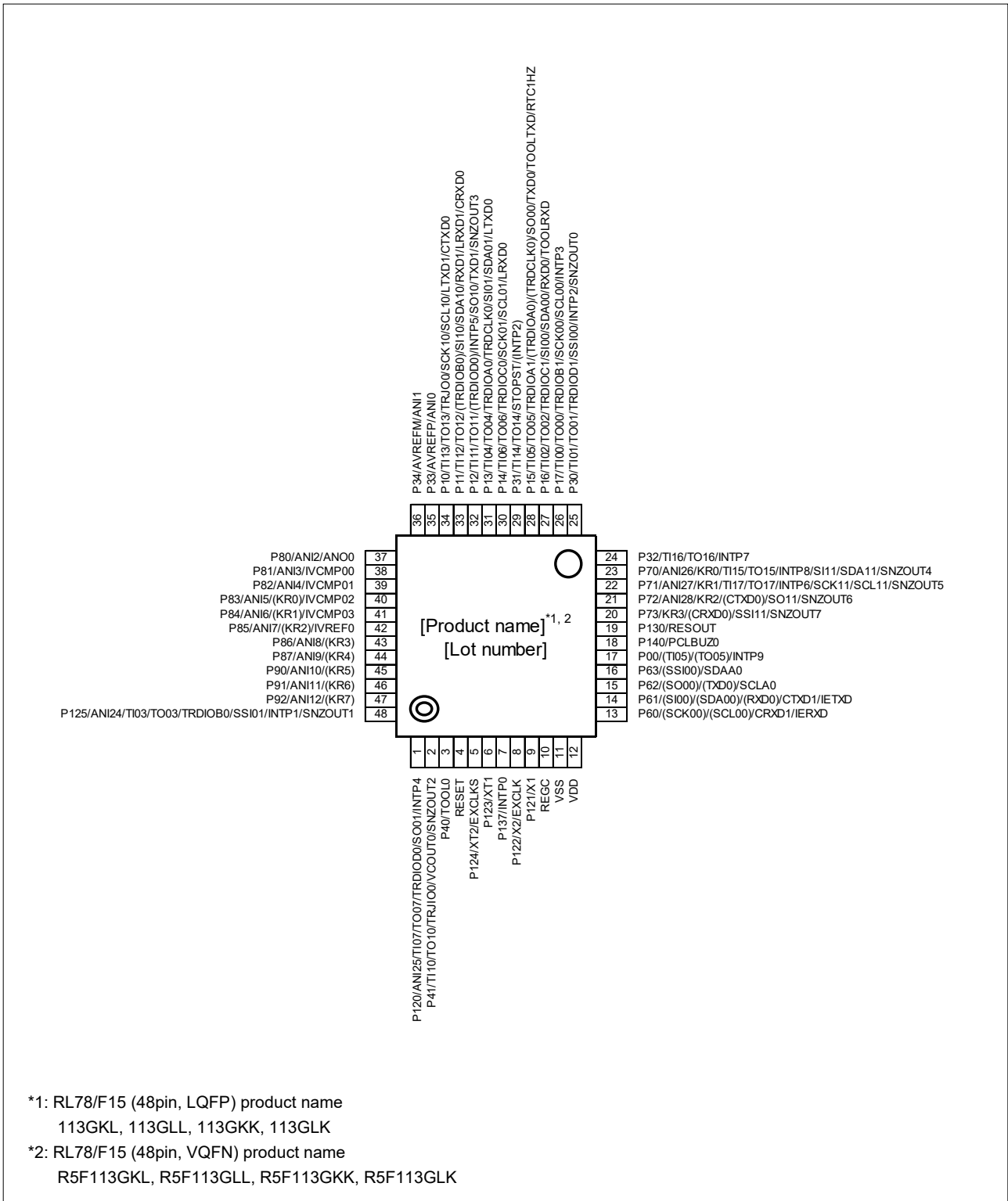


Figure 2.5 Pin configuration for RL78F15 products (48 pins)

Table 2.5 Pin assignment for RL78F15 products (48 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/IICA/CAN/LIN/IEBus	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5	XT2/EXCLKS	P124					
6	XT1	P123					
7		P137				INTP0	
8	X2/EXCLK	P122					
9	X1	P121					
10	REGC						
11	VSS						
12	VDD						
13		P60			(SCK00)/(SCL00)/CRXD1/ IERXD		
14		P61			(SI00)/(SDA00)/(RXD0)/ CTXD1/IETXD		
15		P62			(SO00)/(TXD0)/SCLA0		
16		P63			(SSI00)/SDAA0		
17		P00		(TI05)/(TO05)		INTP9	
18		P140					PCLBUZ0
19		P130					RESOUT
20		P73			(CRXD0)/SSI11	KR3	SNZOUT7
21		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
22		P71	ANI27	TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
23		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
24		P32		TI16/TO16		INTP7	
25		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
26		P17		TI00/TO00/TRDIOD1	SCK00/SCL00	INTP3	
27		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
28		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/ RTC1HZ
29		P31		TI14/TO14		(INTP2)	STOPST
30		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
31		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
32		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
33		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/ LRXD1/CRXD0		
34		P10		TI13/TO13/TRJIO0	SCK10/SCL10/LTXD1/ CTXD0		
35		P33	AVREFP/ANI0				
36		P34	AVREFM/ANI1				
37		P80	ANI2/ANO0				
38		P81	ANI3/IVCMP00				
39		P82	ANI4/IVCMP01				
40		P83	ANI5/IVCMP02			(KR0)	
41		P84	ANI6/IVCMP03			(KR1)	
42		P85	ANI7/IVREF0			(KR2)	
43		P86	ANI8			(KR3)	
44		P87	ANI9			(KR4)	
45		P90	ANI10			(KR5)	
46		P91	ANI11			(KR6)	
47		P92	ANI12			(KR7)	
48		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution Shaded functions are allocated as the multiple pins.
 Functions in parentheses are not assigned after reset release.
 Functions in parentheses can be assigned via settings in the PIORx registers.

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Revision History

Rev.	Date	Description	
		Page	Summary
Rev. 1.00	2017. 6.30		1 st edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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