RL78/F13, F14

Pin assignment of RL78/F13, F14 by model

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Introduction

This application note describes pin assignment of each model of the RL78/F13 and F14 microcontrollers.

In this application note, the products are classified into the following five groups according to the product model, pin count and code flash memory size.

Group A: RL78/F13 (LIN incorporated) products with 20, 30, 32, 48, or 64 pins and 16 Kbytes to 64 Kbytes of code flash memory
Group B: RL78/F13 (LIN incorporated) products with 48 or 64 pins and 96 Kbytes to 128 Kbytes of code flash memory, or RL78/F13 (LIN incorporated) products with 80 pins and 64 Kbytes to 128 Kbytes of code flash memory
Group C: RL78/F13 (CAN and LIN incorporated) products with 30, 32, 48, 64, or 80 pins and 32 Kbytes to 128 Kbytes of code flash memory
Group D: RL78/F14 products with 30, 32, 48, 64, or 80 pins and 48 Kbytes to 96 Kbytes of code flash memory
Group E: RL78/F14 products with 48, 64 or 80 pins and 128 Kbytes to 256 Kbytes of code flash memory, or RL78/F14 products with 100 pins and 64 Kbytes to 256 Kbytes of code flash memory

Contents

1. Product grouping definition

Table 1.1 to Table 1.5 show the grouping definition for each model. The following tables show figures and tables to refer to pin configuration and pin assignment for each product.

Table 1.1 List of Group A products of RL78/F13 (LIN incorporated)

Pin count	Model name	Pin configuration	Pin assignment
64 pins	R5F10ALC, R5F10ALD, R5F10ALE	Figure 2.1	Table 2.1
48 pins	R5F10AGA, R5F10AGC, R5F10AGD, R5F10AGE	Figure 2.2	Table 2.2
32 pins	R5F10ABA, R5F10ABC, R5F10ABD, R5F10ABE	Figure 2.3	Table 2.3
30 pins	R5F10AAA, R5F10AAC, R5F10AAD, R5F10AAE	Figure 2.4	Table 2.4
20 pins	R5F10A6A, R5F10A6C, R5F10A6D, R5F10A6E	Figure 2.5	Table 2.5

Table 1.2 List of Group B products of RL78/F13 (LIN incorporated)

Pin count	Model name	Pin configuration	Pin assignment
80 pins	R5F10AME, R5F10AMF, R5F10AMG	Figure 3.1	Table 3.1
64 pins	R5F10ALF, R5F10ALG	Figure 3.2	Table 3.2
48 pins	R5F10AGF, R5F10AGG	Figure 3.3	Table 3.3

Table 1.3 List of Group C products of RL78/F13 (CAN and LIN incorporated)

Pin count	Model name	Pin configuration	Pin assignment
80 pins	R5F10BME, R5F10BMF, R5F10BMG	Figure 4.1	Table 4.1
64 pins	R5F10BLC, R5F10BLD, R5F10BLE, R5F10BLF, R5F10BLG	Figure 4.2	Table 4.2
48 pins	R5F10BGC, R5F10BGD, R5F10BGE, R5F10BGF, R5F10BGG	Figure 4.3	Table 4.3
32 pins	R5F10BBC, R5F10BBD, R5F10BBE, R5F10BBF, R5F10BBG	Figure 4.4	Table 4.4
30 pins	R5F10BAC, R5F10BAD, R5F10BAE, R5F10BAF, R5F10BAG	Figure 4.5	Table 4.5

Table 1.4 List of Group D products of RL78/F14

Pin count	Model name	Pin configuration	Pin assignment
80 pins	R5F10PME, R5F10PMF	Figure 5.1	Table 5.1
64 pins	R5F10PLE, R5F10PLF	Figure 5.2	Table 5.2
48 pins	R5F10PGD, R5F10PGE, R5F10PGF	Figure 5.3	Table 5.3
32 pins	R5F10PBD, R5F10PBE	Figure 5.4	Table 5.4
30 pins	R5F10PAD, R5F10PAE	Figure 5.5	Table 5.5

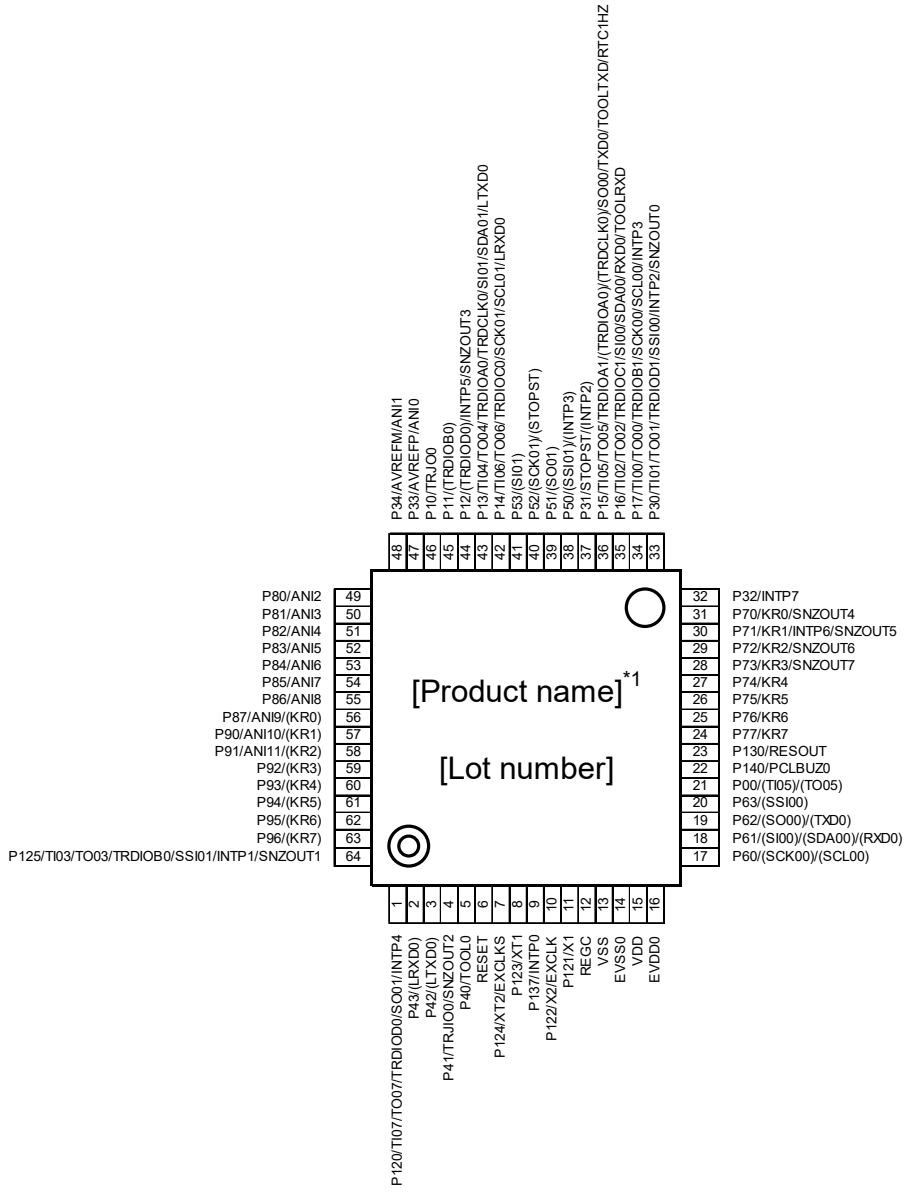
Table 1.5 List of Group E products of RL78/F14

Pin count	Model name	Pin configuration	Pin assignment
100 pins	R5F10PPE, R5F10PPF, R5F10PPG, R5F10PPH, R5F10PPJ	Figure 6.1	Table 6.1
80 pins	R5F10PMG, R5F10PMH, R5F10PMJ	Figure 6.2	Table 6.2
64 pins	R5F10PLG, R5F10PLH, R5F10PLJ	Figure 6.3	Table 6.3
48 pins	R5F10PGG, R5F10PGH, R5F10PGJ	Figure 6.4	Table 6.4

2. RL78/F13 (LIN incorporated) pin assignment for Group A products

The pin configuration and pin assignment for Group A products of RL78/F13 (LIN incorporated) are illustrated and listed according to the number of pins included.

2.1 Group A products (64 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group A (64pin, LQFP) product name
R5F10ALCL, R5F10ALDL, R5F10ALEL, R5F10ALCK, R5F10ALDK, R5F10ALEK,
R5F10ALCY, R5F10ALDY, R5F10ALEY

Figure 2.1 RL78/F13 (LIN incorporated) pin configuration for Group A products (64 pins)

Table 2.1 RL78/F13 (LIN incorporated) pin assignment for Group A products (64 pins) (1/2)

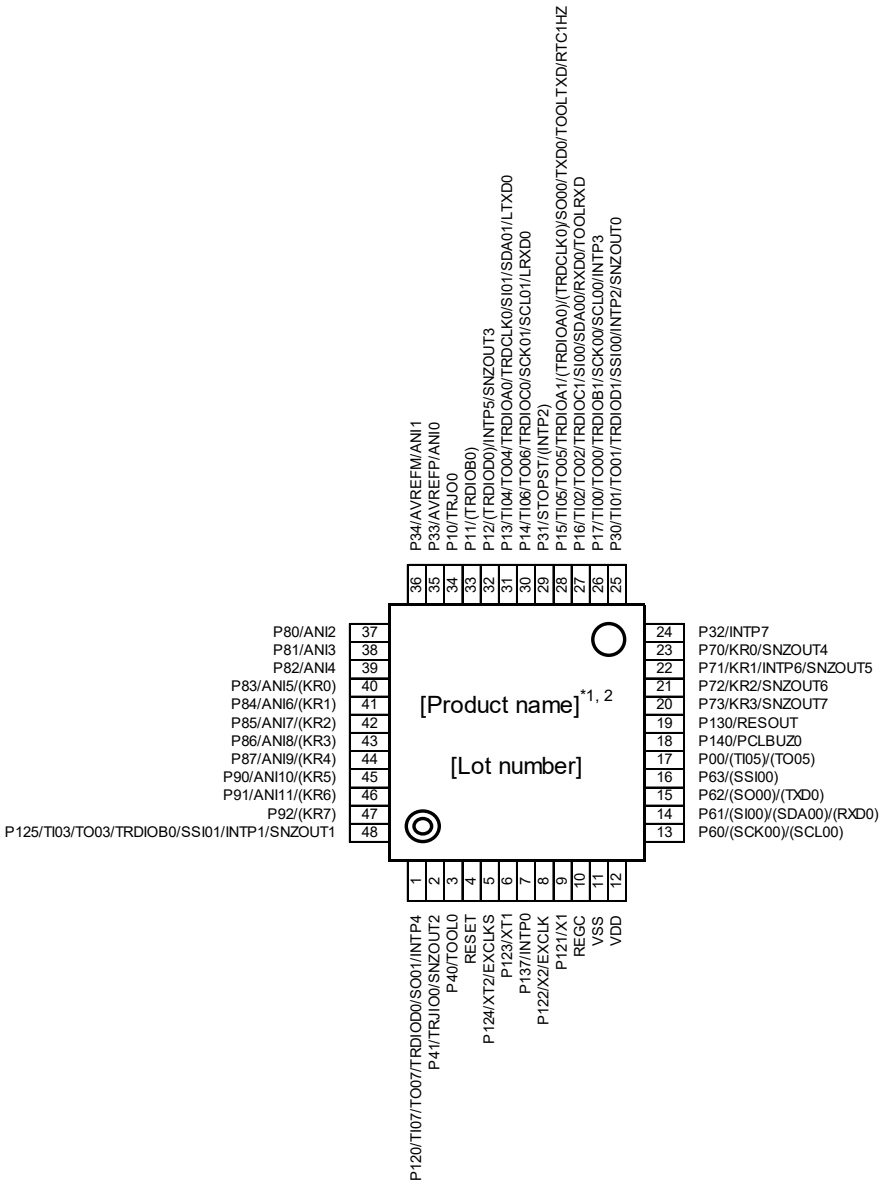
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120		TI07/TO07/TRDIOD0	SO01	INTP4	
2		P43			(LRXD0)		
3		P42			(LTXD0)		
4		P41		TRJIO0			SNZOUT2
5	TOOL0	P40					
6	RESET						
7	XT2/EXCLKS	P124					
8	XT1	P123					
9		P137				INTP0	
10	X2/EXCLK	P122					
11	X1	P121					
12	REGC						
13	VSS						
14	EVSS0						
15	VDD						
16	EVDD0						
17		P60			(SCK00)/(SCL00)		
18		P61			(SI00)/(SDA00)/(RXD0)		
19		P62			(SO00)/(TXD0)		
20		P63			(SSI00)		
21		P00		(TI05)/(TO05)			
22		P140					PCLBUZ0
23		P130					RESOUT
24		P77				KR7	
25		P76				KR6	
26		P75				KR5	
27		P74				KR4	
28		P73				KR3	SNZOUT7
29		P72				KR2	SNZOUT6
30		P71				KR1/INTP6	SNZOUT5
31		P70				KR0	SNZOUT4
32		P32				INTP7	
33		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
34		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
35		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
36		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
37		P31				(INTP2)	STOPST
38		P50			(SSI01)	(INTP3)	
39		P51			(SO01)		
40		P52			(SCK01)		(STOPST)
41		P53			(SI01)		
42		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
43		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
44		P12		(TRDIOD0)		INTP5	SNZOUT3
45		P11		(TRDIOB0)			
46		P10		TRJO0			
47		P33	AVREFP/ANI0				
48		P34	AVREFM/ANI1				
49		P80	ANI2				
50		P81	ANI3				
51		P82	ANI4				
52		P83	ANI5				
53		P84	ANI6				
54		P85	ANI7				
55		P86	ANI8				

Table 2.1 RL78/F13 (LIN incorporated) pin assignment for Group A products (64 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
56		P87	ANI9			(KR0)	
57		P90	ANI10			(KR1)	
58		P91	ANI11			(KR2)	
59		P92				(KR3)	
60		P93				(KR4)	
61		P94				(KR5)	
62		P95				(KR6)	
63		P96				(KR7)	
64		P125		TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

2.2 Group A product (48 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group A (48pin, LQFP) product name
10AGAL, 10AGCL, 10AGDL, 10AGEL, 10AGAK, 10AGCK, 10AGDK, 10AGEK,
10AGAY, 10AGCY, 10AGDY, 10AGEY

*2: RL78/F13 group A (48pin, VQFN) product name
R5F10AGAL, R5F10AGCL, R5F10AGDL, R5F10AGEL, R5F10AGAK, R5F10AGCK,
R5F10AGDK, R5F10AGEK, R5F10AGAY, R5F10AGCY, R5F10AGDY, R5F10AGEY

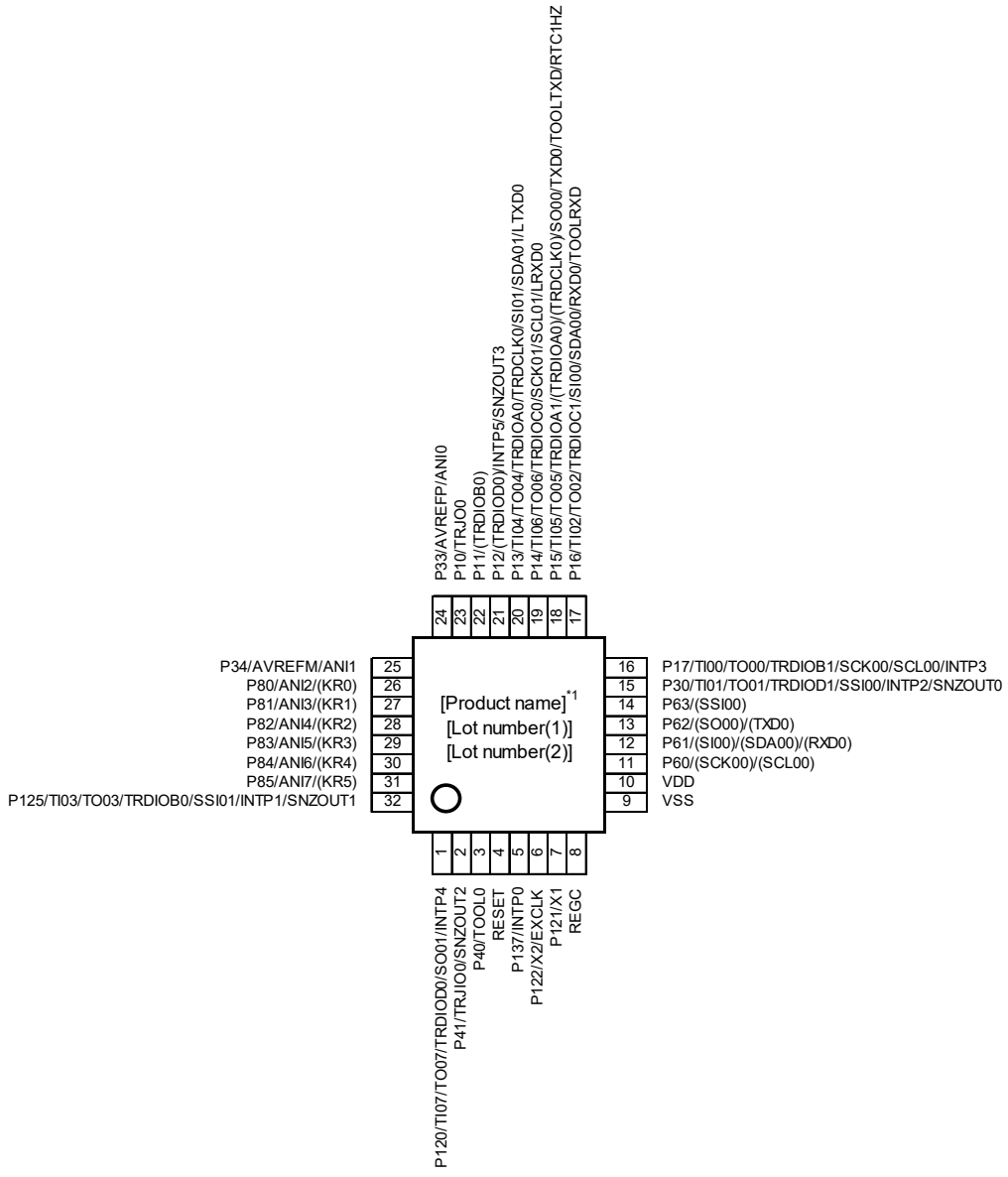
Figure 2.2 RL78/F13 (LIN incorporated) pin configuration for Group A products (48 pins)

Table 2.2 RL78/F13 (LIN incorporated) pin assignment for Group A products (48 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120		TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41		TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5	XT2/EXCLKS	P124					
6	XT1	P123					
7		P137				INTP0	
8	X2/EXCLK	P122					
9	X1	P121					
10	REGC						
11	VSS						
12	VDD						
13		P60			(SCK00)/(SCL00)		
14		P61			(SI00)/(SDA00)/(RXD0)		
15		P62			(SO00)/(TXD0)		
16		P63			(SSI00)		
17		P00		(TI05)/(TO05)			
18		P140					PCLBUZ0
19		P130					RESOUT
20		P73				KR3	SNZOUT7
21		P72				KR2	SNZOUT6
22		P71				KR1/INTP6	SNZOUT5
23		P70				KR0	SNZOUT4
24		P32				INTP7	
25		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
26		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
27		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
28		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
29		P31				(INTP2)	STOPST
30		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
31		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
32		P12		(TRDIOD0)		INTP5	SNZOUT3
33		P11		(TRDIOB0)			
34		P10		TRJO0			
35		P33	AVREFP/ANI0				
36		P34	AVREFM/ANI1				
37		P80	ANI2				
38		P81	ANI3				
39		P82	ANI4				
40		P83	ANI5			(KR0)	
41		P84	ANI6			(KR1)	
42		P85	ANI7			(KR2)	
43		P86	ANI8			(KR3)	
44		P87	ANI9			(KR4)	
45		P90	ANI10			(KR5)	
46		P91	ANI11			(KR6)	
47		P92				(KR7)	
48		P125		TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

2.3 Group A product (32 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group A (32pin, VQFN) product name
10AAL, 10ACL, 10ADL, 10AEL, 10AAK, 10ACK, 10ADK, 10AEK,
10AAY, 10ACY, 10ADY, 10AEY

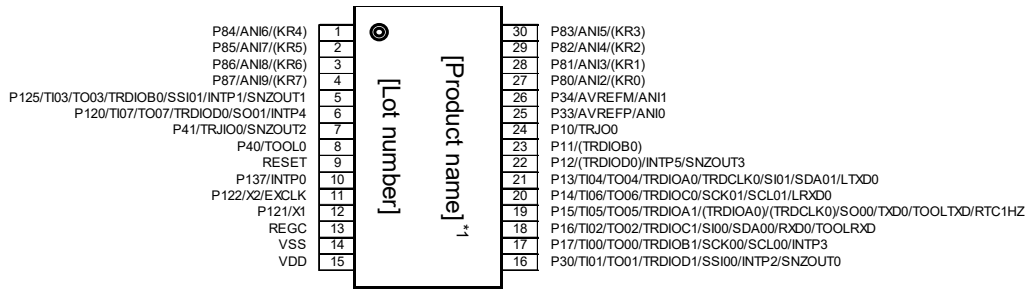
Figure 2.3 RL78/F13 (LIN incorporated) pin configuration for Group A products (32 pins)

Table 2.3 RL78/F13 (LIN incorporated) pin assignment for Group A products (32 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120		TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41		TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5		P137				INTP0	
6	X2/EXCLK	P122					
7	X1	P121					
8	REGC						
9	VSS						
10	VDD						
11		P60			(SCK00)/(SCL00)		
12		P61			(SI00)/(SDA00)/(RXD0)		
13		P62			(SO00)/(TXD0)		
14		P63			(SSI00)		
15		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
16		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
17		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
18		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
19		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
20		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
21		P12		(TRDIOD0)		INTP5	SNZOUT3
22		P11		(TRDIOB0)			
23		P10		TRJO0			
24		P33	AVREFP/ANI0				
25		P34	AVREFM/ANI1				
26		P80	ANI2			(KR0)	
27		P81	ANI3			(KR1)	
28		P82	ANI4			(KR2)	
29		P83	ANI5			(KR3)	
30		P84	ANI6			(KR4)	
31		P85	ANI7			(KR5)	
32		P125		TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

2.4 Group A products (30 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group A (30pin, SSOP) product name

R5F10AAAL, R5F10AACL, R5F10AADL, R5F10AAEL, R5F10AAAK, R5F10AACK,

R5F10AADK, R5F10AAEK, R5F10AAAY, R5F10AACY, R5F10AADY, R5F10AAEY

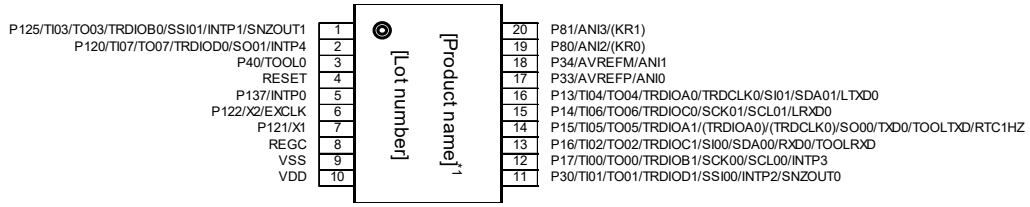
Figure 2.4 RL78/F13 (LIN incorporated) pin configuration for Group A products (30 pins)

Table 2.4 RL78/F13 (LIN incorporated) pin assignment for Group A products (30 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P84	ANI6			(KR4)	
2		P85	ANI7			(KR5)	
3		P86	ANI8			(KR6)	
4		P87	ANI9			(KR7)	
5		P125		TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1
6		P120		TI07/TO07/TRDIOD0	SO01	INTP4	
7		P41		TRJIO0			SNZOUT2
8	TOOL0	P40					
9	RESET						
10		P137				INTP0	
11	X2/EXCLK	P122					
12	X1	P121					
13	REGC						
14	VSS						
15	VDD						
16		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
17		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
18		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
19		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
20		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
21		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
22		P12		(TRDIOD0)		INTP5	SNZOUT3
23		P11		(TRDIOB0)			
24		P10		TRJO0			
25		P33	AVREFP/ANI0				
26		P34	AVREFM/ANI1				
27		P80	ANI2			(KR0)	
28		P81	ANI3			(KR1)	
29		P82	ANI4			(KR2)	
30		P83	ANI5			(KR3)	

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

2.5 Group A products (20 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group A (20pin, SSOP) product name

R5F10A6AL, R5F10A6CL, R5F10A6DL, R5F10A6EL, R5F10A6AK, R5F10A6CK,

R5F10A6DK, R5F10A6EK, R5F10A6AY, R5F10A6CY, R5F10A6DY, R5F10A6EY

Figure 2.5 RL78/F13 (LIN incorporated) pin configuration for Group A products (20 pins)

Table 2.5 RL78/F13 (LIN incorporated) pin assignment for Group A products (20 pins)

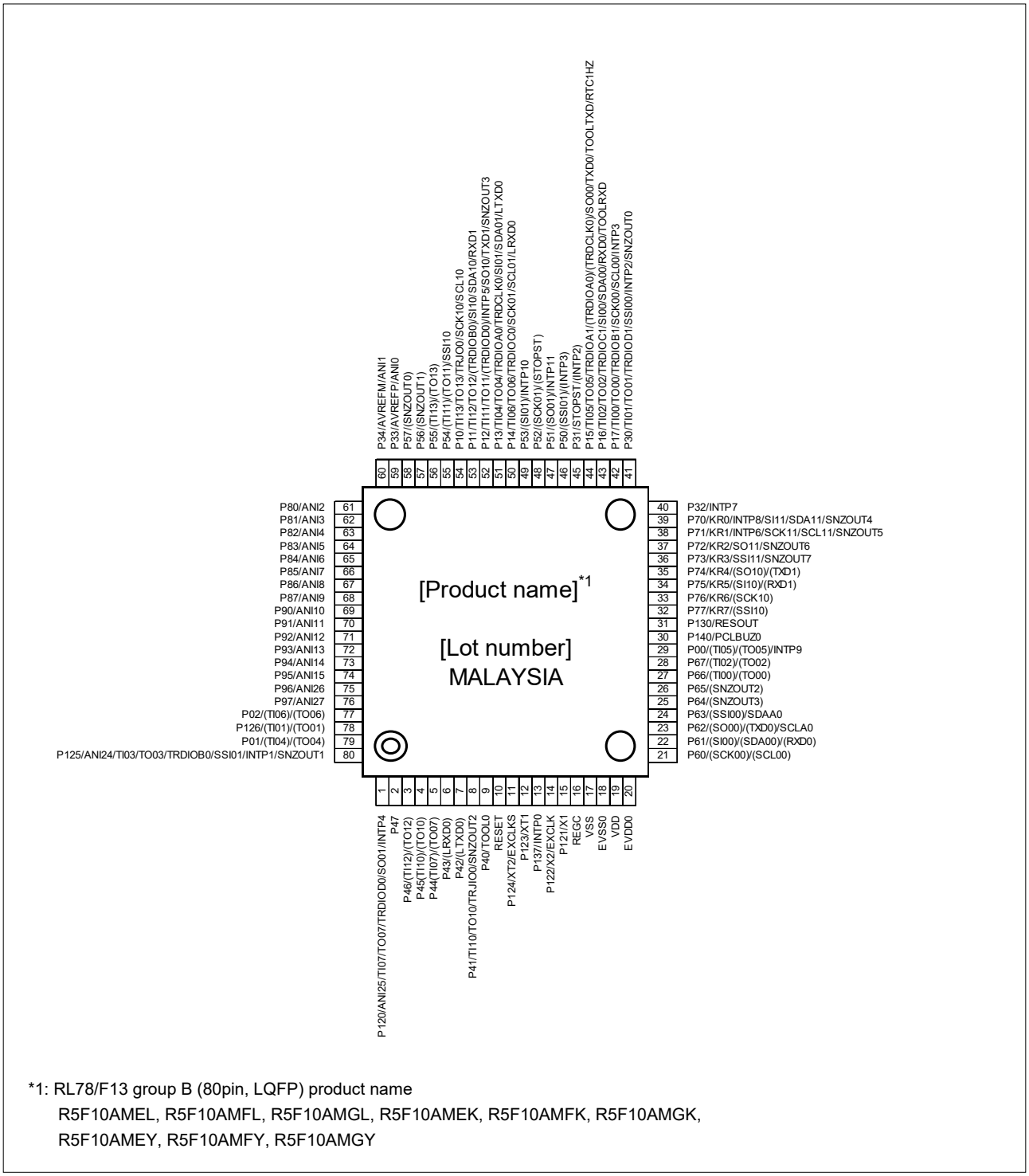
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P125		TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1
2		P120		TI07/TO07/TRDIOD0	SO01	INTP4	
3	TOOL0	P40					
4	RESET						
5		P137				INTP0	
6	X2/EXCLK	P122					
7	X1	P121					
8	REGC						
9	VSS						
10	VDD						
11		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
12		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
13		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
14		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
15		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
16		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
17		P33	AVREFP/ANI0				
18		P34	AVREFM/ANI1				
19		P80	ANI2			(KR0)	
20		P81	ANI3			(KR1)	

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

3. RL78/F13 (LIN incorporated) pin assignment for Group B products

The pin configuration and pin assignment for Group B products of RL78/F13 (LIN incorporated) are illustrated and listed according to the number of pins included.

3.1 Group B products (80 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group B (80pin, LQFP) product name
R5F10AMEL, R5F10AMFL, R5F10AMGL, R5F10AMEK, R5F10AMFK, R5F10AMGK,
R5F10AMEY, R5F10AMFY, R5F10AMGY

Figure 3.1 RL78/F13 (LIN incorporated) pin configuration for Group B products (80 pins)

Table 3.1 RL78/F13 (LIN incorporated) pin assignment for Group B products (80 pins) (1/2)

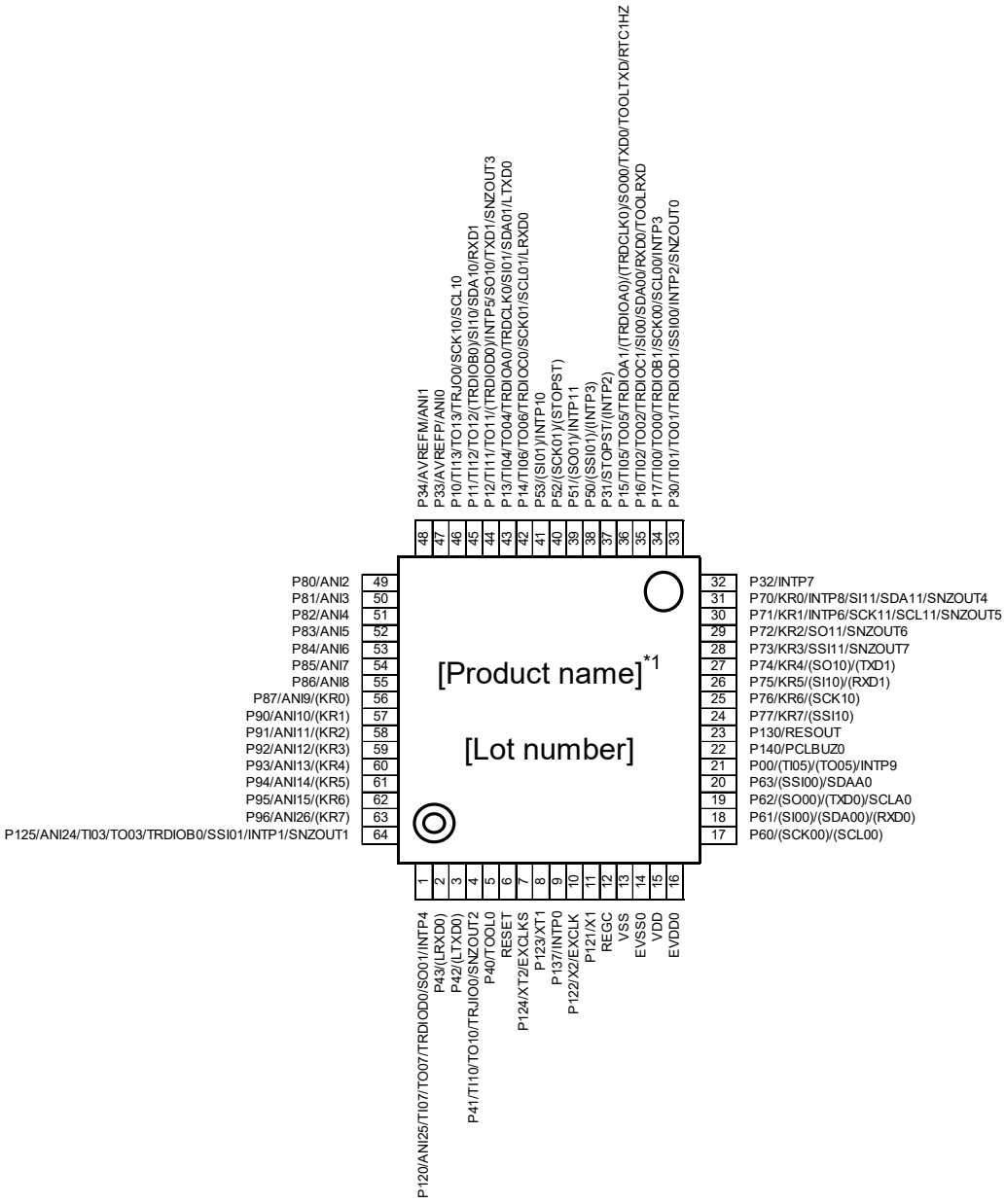
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P47					
3		P46		(TI12)/(TO12)			
4		P45		(TI10)/(TO10)			
5		P44		(TI07)/(TO07)			
6		P43			(LRXD0)		
7		P42			(LTXD0)		
8		P41		TI10/TO10/TRJIO0			SNZOUT2
9	TOOL0	P40					
10	RESET						
11	XT2/EXCLKS	P124					
12	XT1	P123					
13		P137				INTP0	
14	X2/EXCLK	P122					
15	X1	P121					
16	REGC						
17	VSS						
18	EVSS0						
19	VDD						
20	EVDD0						
21		P60			(SCK00)/(SCL00)		
22		P61			(SI00)/(SDA00)/(RXD0)		
23		P62			(SO00)/(TXD0)/SCLA0		
24		P63			(SSI00)/SDAA0		
25		P64					(SNZOUT3)
26		P65					(SNZOUT2)
27		P66		(TI00)/(TO00)			
28		P67		(TI02)/(TO02)			
29		P00		(TI05)/(TO05)		INTP9	
30		P140					PCLBUZ0
31		P130					RESOUT
32		P77			(SSI10)	KR7	
33		P76			(SCK10)	KR6	
34		P75			(SI10)/(RXD1)	KR5	
35		P74			(SO10)/(TXD1)	KR4	
36		P73			SSI11	KR3	SNZOUT7
37		P72			SO11	KR2	SNZOUT6
38		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
39		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
40		P32				INTP7	
41		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
42		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
43		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
44		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
45		P31				(INTP2)	STOPST
46		P50			(SSI01)	(INTP3)	
47		P51			(SO01)	INTP11	
48		P52			(SCK01)		(STOPST)
49		P53			(SI01)	INTP10	
50		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
51		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
52		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
53		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1		
54		P10		TI13/TO13/TRJO0	SCK10/SCL10		
55		P54		(TI11)/(TO11)	SSI10		
56		P55		(TI13)/(TO13)			

Table 3.1 RL78/F13 (LIN incorporated) pin assignment for Group B products (80 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
57		P56					(SNZOUT1)
58		P57					(SNZOUT0)
59		P33	AVREFP/ANI0				
60		P34	AVREFM/ANI1				
61		P80	ANI2				
62		P81	ANI3				
63		P82	ANI4				
64		P83	ANI5				
65		P84	ANI6				
66		P85	ANI7				
67		P86	ANI8				
68		P87	ANI9				
69		P90	ANI10				
70		P91	ANI11				
71		P92	ANI12				
72		P93	ANI13				
73		P94	ANI14				
74		P95	ANI15				
75		P96	ANI26				
76		P97	ANI27				
77		P02		(TI06)/(TO06)			
78		P126		(TI01)/(TO01)			
79		P01		(TI04)/(TO04)			
80		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

3.2 Group B products (64 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group B (64pin, LQFP) product name
R5F10ALFL, R5F10ALGL, R5F10ALFK, R5F10ALGK, R5F10ALFY, R5F10ALGY

Figure 3.2 RL78/F13 (LIN incorporated) pin configuration for Group B products (64 pins)

Table 3.2 RL78/F13 (LIN incorporated) pin assignment for Group B products (64 pins) (1/2)

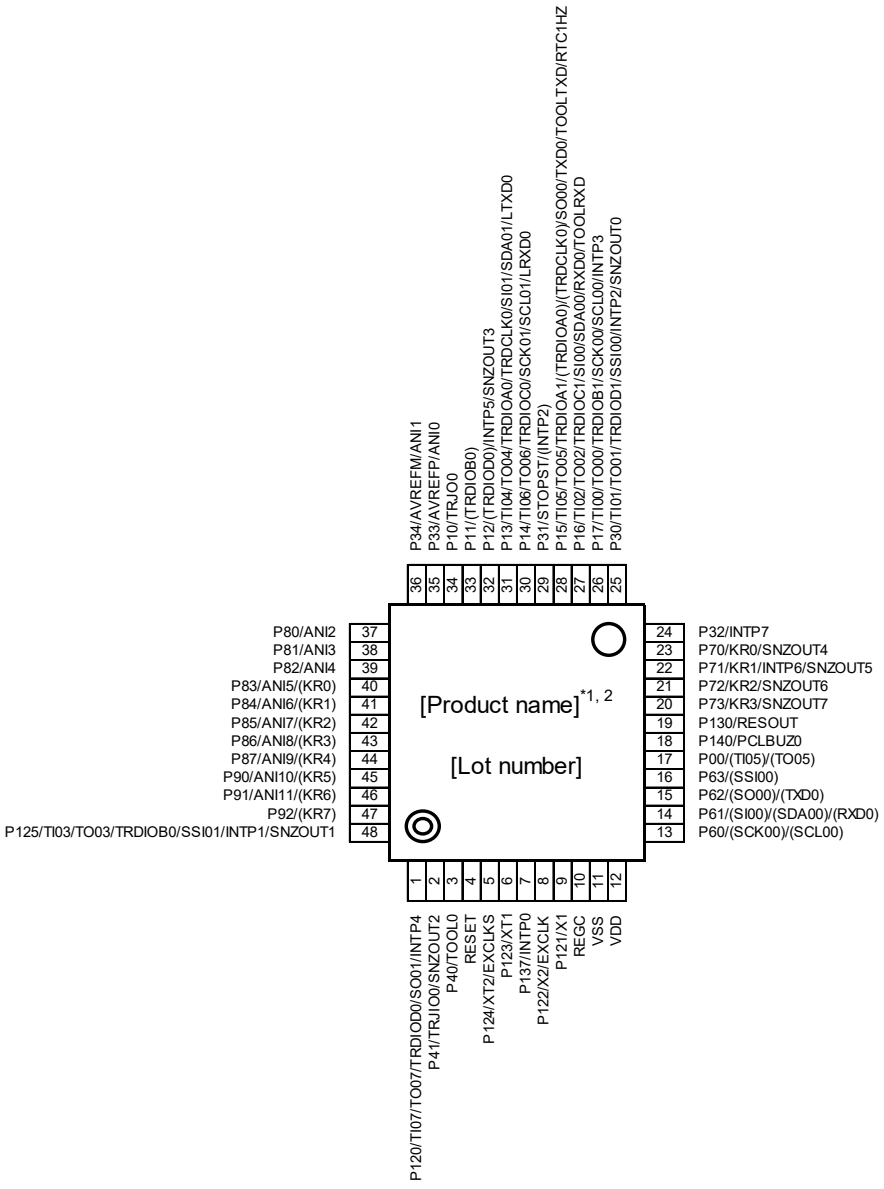
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P43			(LRXD0)		
3		P42			(LTXD0)		
4		P41		TI10/TO10/TRJIO0			SNZOUT2
5	TOOL0	P40					
6	RESET						
7	XT2/EXCLKS	P124					
8	XT1	P123					
9		P137				INTP0	
10	X2/EXCLK	P122					
11	X1	P121					
12	REGC						
13	VSS						
14	EVSS0						
15	VDD						
16	EVDD0						
17		P60			(SCK00)/(SCL00)		
18		P61			(SI00)/(SDA00)/(RXD0)		
19		P62			(SO00)/(TXD0)/SCLA0		
20		P63			(SSI00)/SDAA0		
21		P00		(TI05)/(TO05)		INTP9	
22		P140					PCLBUZ0
23		P130					RESOUT
24		P77			(SSI10)	KR7	
25		P76			(SCK10)	KR6	
26		P75			(SI10)/(RXD1)	KR5	
27		P74			(SO10)/(TXD1)	KR4	
28		P73			SSI11	KR3	SNZOUT7
29		P72			SO11	KR2	SNZOUT6
30		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
31		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
32		P32				INTP7	
33		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
34		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
35		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
36		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
37		P31				(INTP2)	STOPST
38		P50			(SSI01)	(INTP3)	
39		P51			(SO01)	INTP11	
40		P52			(SCK01)		(STOPST)
41		P53			(SI01)	INTP10	
42		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
43		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
44		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
45		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1		
46		P10		TI13/TO13/TRJO0	SCK10/SCL10		
47		P33	AVREFP/ANI0				
48		P34	AVREFM/ANI1				
49		P80	ANI2				
50		P81	ANI3				
51		P82	ANI4				
52		P83	ANI5				
53		P84	ANI6				
54		P85	ANI7				
55		P86	ANI8				

Table 3.2 RL78/F13 (LIN incorporated) pin assignment for Group B products (64 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
56		P87	ANI9			(KR0)	
57		P90	ANI10			(KR1)	
58		P91	ANI11			(KR2)	
59		P92	ANI12			(KR3)	
60		P93	ANI13			(KR4)	
61		P94	ANI14			(KR5)	
62		P95	ANI15			(KR6)	
63		P96	ANI26			(KR7)	
64		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

3.3 Group B product (48 pins) of RL78/F13 (LIN incorporated)



*1: RL78/F13 group B (48pin, LQFP) product name
10AGFL, 10AGGL, 10AGFK, 10AGGK, 10AGFY, 10AGGY
*2: RL78/F13 group B (48pin, VQFN) product name
R5F10AGFL, R5F10AGGL, R5F10AGFK, R5F10AGGK, R5F10AGFY, R5F10AGGY

Figure 3.3 RL78/F13 (LIN incorporated) pin configuration for Group B products (48 pins)

Table 3.3 RL78/F13 (LIN incorporated) pin assignment for Group B products (48 pins)

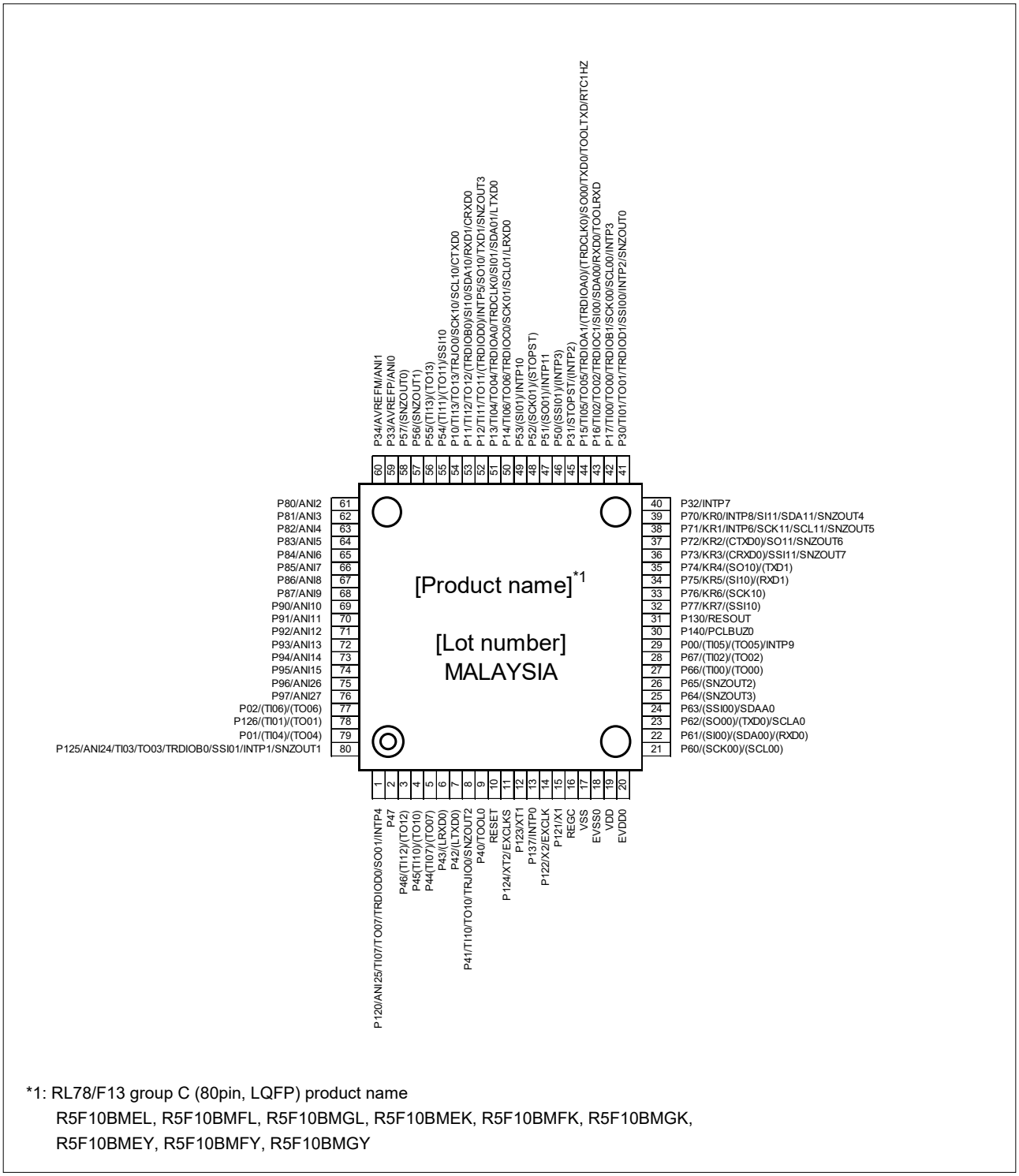
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41		TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5	XT2/EXCLKS	P124					
6	XT1	P123					
7		P137				INTP0	
8	X2/EXCLK	P122					
9	X1	P121					
10	REGC						
11	VSS						
12	VDD						
13		P60			(SCK00)/(SCL00)		
14		P61			(SI00)/(SDA00)/(RXD0)		
15		P62			(SO00)/(TXD0)/SCLA0		
16		P63			(SSI00)/SDAA0		
17		P00		(TI05)/(TO05)		INTP9	
18		P140					PCLBUZ0
19		P130					RESOUT
20		P73			SSI11	KR3	SNZOUT7
21		P72			SO11	KR2	SNZOUT6
22		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
23		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
24		P32				INTP7	
25		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
26		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
27		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
28		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
29		P31				(INTP2)	STOPST
30		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
31		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
32		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
33		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1		
34		P10		TI13/TO13/TRJO0	SCK10/SCL10		
35		P33	AVREFP/ANI0				
36		P34	AVREFM/ANI1				
37		P80	ANI2				
38		P81	ANI3				
39		P82	ANI4				
40		P83	ANI5			(KR0)	
41		P84	ANI6			(KR1)	
42		P85	ANI7			(KR2)	
43		P86	ANI8			(KR3)	
44		P87	ANI9			(KR4)	
45		P90	ANI10			(KR5)	
46		P91	ANI11			(KR6)	
47		P92	ANI12			(KR7)	
48		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

4. RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products

The pin assignment and pin configuration for Group C products of RL78/F13 (CAN and LIN incorporated) are illustrated and listed according to the number of pins included.

4.1 Group C products (80 pins) of RL78/F13 (CAN and LIN incorporated)



*1: RL78/F13 group C (80pin, LQFP) product name
R5F10BMEL, R5F10BMFL, R5F10BMGL, R5F10BMEK, R5F10BMFK, R5F10BMGK,
R5F10BMEY, R5F10BMFY, R5F10BMGY

Figure 4.1 RL78/F13 (CAN and LIN incorporated) pin configuration for Group C products (80 pins)

Table 4.1 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (80 pins) (1/2)

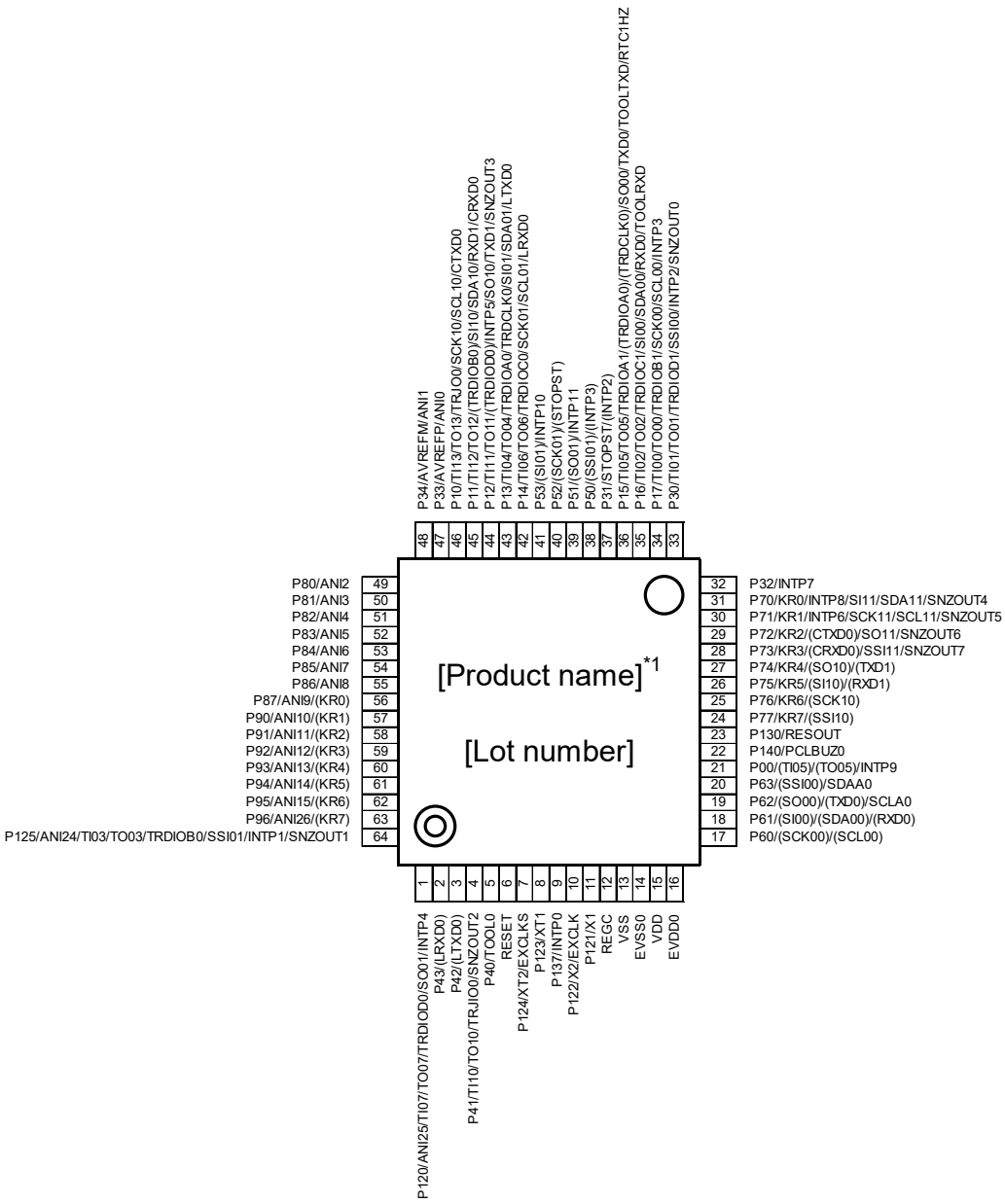
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P47					
3		P46		(TI12)/(TO12)			
4		P45		(TI10)/(TO10)			
5		P44		(TI07)/(TO07)			
6		P43			(LRXD0)		
7		P42			(LTXD0)		
8		P41		TI10/TO10/TRJIO0			SNZOUT2
9	TOOL0	P40					
10	RESET						
11	XT2/EXCLKS	P124					
12	XT1	P123					
13		P137				INTP0	
14	X2/EXCLK	P122					
15	X1	P121					
16	REGC						
17	VSS						
18	EVSS0						
19	VDD						
20	EVDD0						
21		P60			(SCK00)/(SCL00)		
22		P61			(SI00)/(SDA00)/(RXD0)		
23		P62			(SO00)/(TXD0)/SCLA0		
24		P63			(SSI00)/SDAA0		
25		P64					(SNZOUT3)
26		P65					(SNZOUT2)
27		P66		(TI00)/(TO00)			
28		P67		(TI02)/(TO02)			
29		P00		(TI05)/(TO05)		INTP9	
30		P140					PCLBUZ0
31		P130					RESOUT
32		P77			(SSI10)	KR7	
33		P76			(SCK10)	KR6	
34		P75			(SI10)/(RXD1)	KR5	
35		P74			(SO10)/(TXD1)	KR4	
36		P73			(CRXD0)/SSI11	KR3	SNZOUT7
37		P72			(CTXD0)/SO11	KR2	SNZOUT6
38		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
39		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
40		P32				INTP7	
41		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
42		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
43		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
44		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
45		P31				(INTP2)	STOPST
46		P50			(SSI01)	(INTP3)	
47		P51			(SO01)	INTP11	
48		P52			(SCK01)		(STOPST)
49		P53			(SI01)	INTP10	
50		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
51		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
52		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
53		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
54		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
55		P54		(TI11)/(TO11)	SSI10		
56		P55		(TI13)/(TO13)			

Table 4.1 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (80 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
57		P56					(SNZOUT1)
58		P57					(SNZOUT0)
59		P33	AVREFP/ANI0				
60		P34	AVREFM/ANI1				
61		P80	ANI2				
62		P81	ANI3				
63		P82	ANI4				
64		P83	ANI5				
65		P84	ANI6				
66		P85	ANI7				
67		P86	ANI8				
68		P87	ANI9				
69		P90	ANI10				
70		P91	ANI11				
71		P92	ANI12				
72		P93	ANI13				
73		P94	ANI14				
74		P95	ANI15				
75		P96	ANI26				
76		P97	ANI27				
77		P02		(TI06)/(TO06)			
78		P126		(TI01)/(TO01)			
79		P01		(TI04)/(TO04)			
80		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

4.2 Group C products (64 pins) of RL78/F13 (CAN and LIN incorporated)



*1: RL78/F13 group C (64pin, LQFP) product name
R5F10BLCL, R5F10BLDL, R5F10BLEL, R5F10BLFL, R5F10BLGL, R5F10BLCK, R5F10BLDK, R5F10BLEK, R5F10BLFK, R5F10BLGK, R5F10BLCY, R5F10BLDY, R5F10BLEY, R5F10BLFY, R5F10BLGY

Figure 4.2 RL78/F13 (CAN and LIN incorporated) pin configuration for Group C products (64 pins)

Table 4.2 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (64 pins) (1/2)

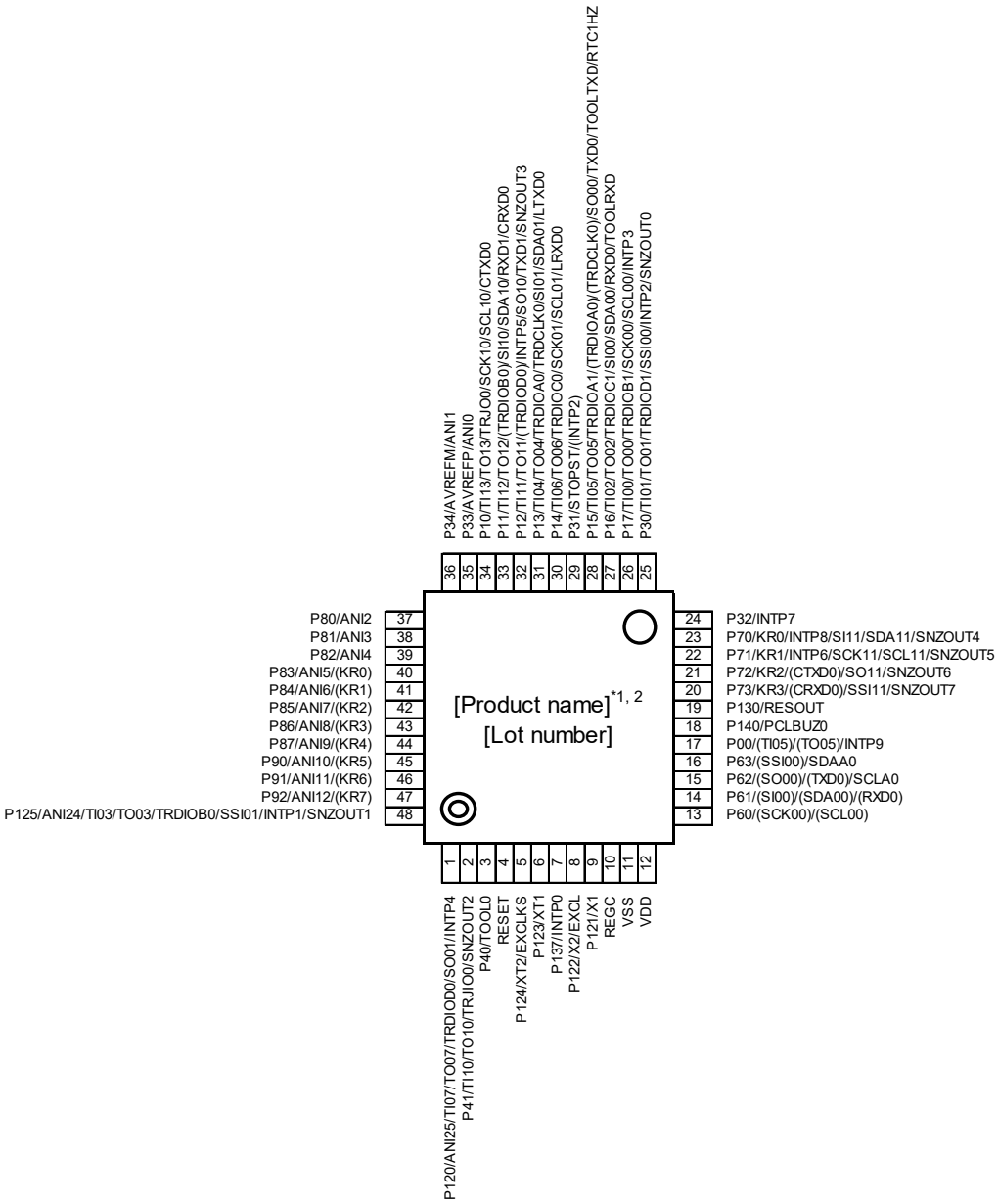
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P43			(LRXD0)		
3		P42			(LTXD0)		
4		P41		TI10/TO10/TRJIO0			SNZOUT2
5	TOOL0	P40					
6	RESET						
7	XT2/EXCLKS	P124					
8	XT1	P123					
9		P137				INTP0	
10	X2/EXCLK	P122					
11	X1	P121					
12	REGC						
13	VSS						
14	EVSS0						
15	VDD						
16	EVDD0						
17		P60			(SCK00)/(SCL00)		
18		P61			(SI00)/(SDA00)/(RXD0)		
19		P62			(SO00)/(TXD0)/SCLA0		
20		P63			(SSI00)/SDAA0		
21		P00		(TI05)/(TO05)		INTP9	
22		P140					PCLBUZ0
23		P130					RESOUT
24		P77			(SSI10)	KR7	
25		P76			(SCK10)	KR6	
26		P75			(SI10)/(RXD1)	KR5	
27		P74			(SO10)/(TXD1)	KR4	
28		P73			(CRXD0)/SSI11	KR3	SNZOUT7
29		P72			(CTXD0)/SO11	KR2	SNZOUT6
30		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
31		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
32		P32				INTP7	
33		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
34		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
35		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
36		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
37		P31				(INTP2)	STOPST
38		P50			(SSI01)	(INTP3)	
39		P51			(SO01)	INTP11	
40		P52			(SCK01)		(STOPST)
41		P53			(SI01)	INTP10	
42		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
43		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
44		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
45		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
46		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
47		P33	AVREFP/ANI0				
48		P34	AVREFM/ANI1				
49		P80	ANI2				
50		P81	ANI3				
51		P82	ANI4				
52		P83	ANI5				
53		P84	ANI6				
54		P85	ANI7				
55		P86	ANI8				

Table 4.2 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (64 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
56		P87	ANI9			(KR0)	
57		P90	ANI10			(KR1)	
58		P91	ANI11			(KR2)	
59		P92	ANI12			(KR3)	
60		P93	ANI13			(KR4)	
61		P94	ANI14			(KR5)	
62		P95	ANI15			(KR6)	
63		P96	ANI26			(KR7)	
64		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

4.3 Group C products (48 pins) of RL78/F13 (CAN and LIN incorporated)



*1: RL78/F13 group C (48pin, LQFP) product name
10BGCL, 10BGDL, 10BGEL, 10BGFL, 10BGGL, 10BGCK, 10BGDK, 10BGEK, 10BGFK, 10BGGK, 10BGCY, 10BGDY, 10BGEY, 10BGFY, 10BGGY

*2: RL78/F13 group C (48pin, VQFN) product name
R5F10BGCL, R5F10BGDL, R5F10BGEL, R5F10BGFL, R5F10BGGL, R5F10BGCK, R5F10BGDK, R5F10BGEK, R5F10BGFK, R5F10BGGK, R5F10BGCY, R5F10BGDY, R5F10BGEY, R5F10BGFY, R5F10BGGY

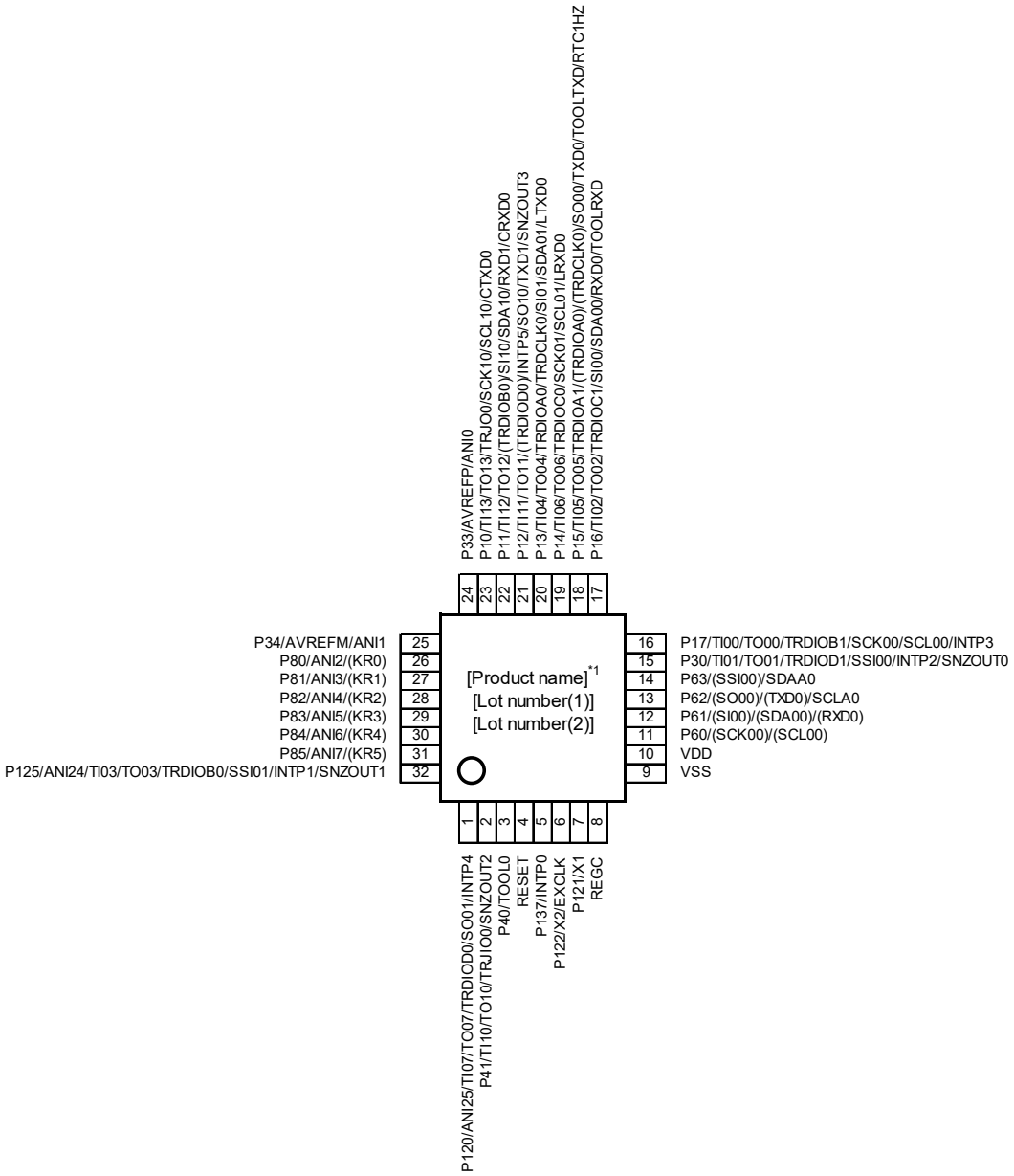
Figure 4.3 RL78/F13 (CAN and LIN incorporated) pin configuration for Group C products (48 pins)

Table 4.3 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (48 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41		TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5	XT2/EXCLKS	P124					
6	XT1	P123					
7		P137				INTP0	
8	X2/EXCLK	P122					
9	X1	P121					
10	REGC						
11	VSS						
12	VDD						
13		P60			(SCK00)/(SCL00)		
14		P61			(SI00)/(SDA00)/(RXD0)		
15		P62			(SO00)/(TXD0)/SCLA0		
16		P63			(SSI00)/SDAA0		
17		P00		(TI05)/(TO05)		INTP9	
18		P140					PCLBUZ0
19		P130					RESOUT
20		P73			(CRXD0)/SSI11	KR3	SNZOUT7
21		P72			(CTXD0)/SO11	KR2	SNZOUT6
22		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
23		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
24		P32				INTP7	
25		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
26		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
27		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
28		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
29		P31				(INTP2)	STOPST
30		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
31		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
32		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
33		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
34		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
35		P33	AVREFP/ANI0				
36		P34	AVREFM/ANI1				
37		P80	ANI2				
38		P81	ANI3				
39		P82	ANI4				
40		P83	ANI5			(KR0)	
41		P84	ANI6			(KR1)	
42		P85	ANI7			(KR2)	
43		P86	ANI8			(KR3)	
44		P87	ANI9			(KR4)	
45		P90	ANI10			(KR5)	
46		P91	ANI11			(KR6)	
47		P92	ANI12			(KR7)	
48		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

4.4 Group C products (32 pins) of RL78/F13 (CAN and LIN incorporated)



*1: RL78/F13 group C (32pin, VQFN) product name
10BCL, 10BDL, 10BEL, 10BFL, 10BGL, 10BCK, 10BDK, 10BEK, 10BFK, 10BGK,
10BCY, 10BDY, 10BEY, 10BFY, 10BGY

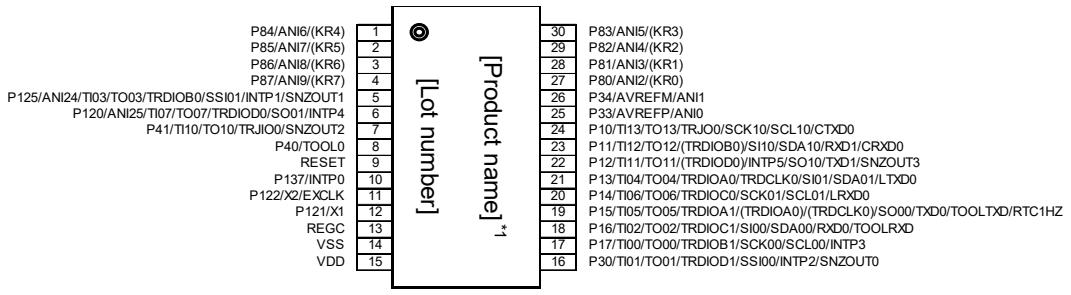
Figure 4.4 RL78/F13 (CAN and LIN incorporated) pin configuration for Group C products (32 pins)

Table 4.4 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (32 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41		TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5		P137				INTP0	
6	X2/EXCLK	P122					
7	X1	P121					
8	REGC						
9	VSS						
10	VDD						
11		P60			(SCK00)/(SCL00)		
12		P61			(SI00)/(SDA00)/(RXD0)		
13		P62			(SO00)/(TXD0)/SCLA0		
14		P63			(SSI00)/SDAA0		
15		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
16		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
17		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
18		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
19		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
20		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
21		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
22		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
23		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
24		P33	AVREFP/ANI0				
25		P34	AVREFM/ANI1				
26		P80	ANI2			(KR0)	
27		P81	ANI3			(KR1)	
28		P82	ANI4			(KR2)	
29		P83	ANI5			(KR3)	
30		P84	ANI6			(KR4)	
31		P85	ANI7			(KR5)	
32		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

4.5 Group C products (30 pins) of RL78/F13 (CAN and LIN incorporated)



*1: RL78/F13 group C (30pin, SSOP) product name
R5F10BACL, R5F10BADL, R5F10BAEL, R5F10BAFL, R5F10BAGL, R5F10BACK, R5F10BADK, R5F10BAEK, R5F10BAFK, R5F10BAGK, R5F10BACY, R5F10BADY, R5F10BAEY, R5F10BAFY, R5F10BAGY

Figure 4.5 RL78/F13 (CAN and LIN incorporated) pin configuration for Group C products (30 pins)

Table 4.5 RL78/F13 (CAN and LIN incorporated) pin assignment for Group C products (30 pins)

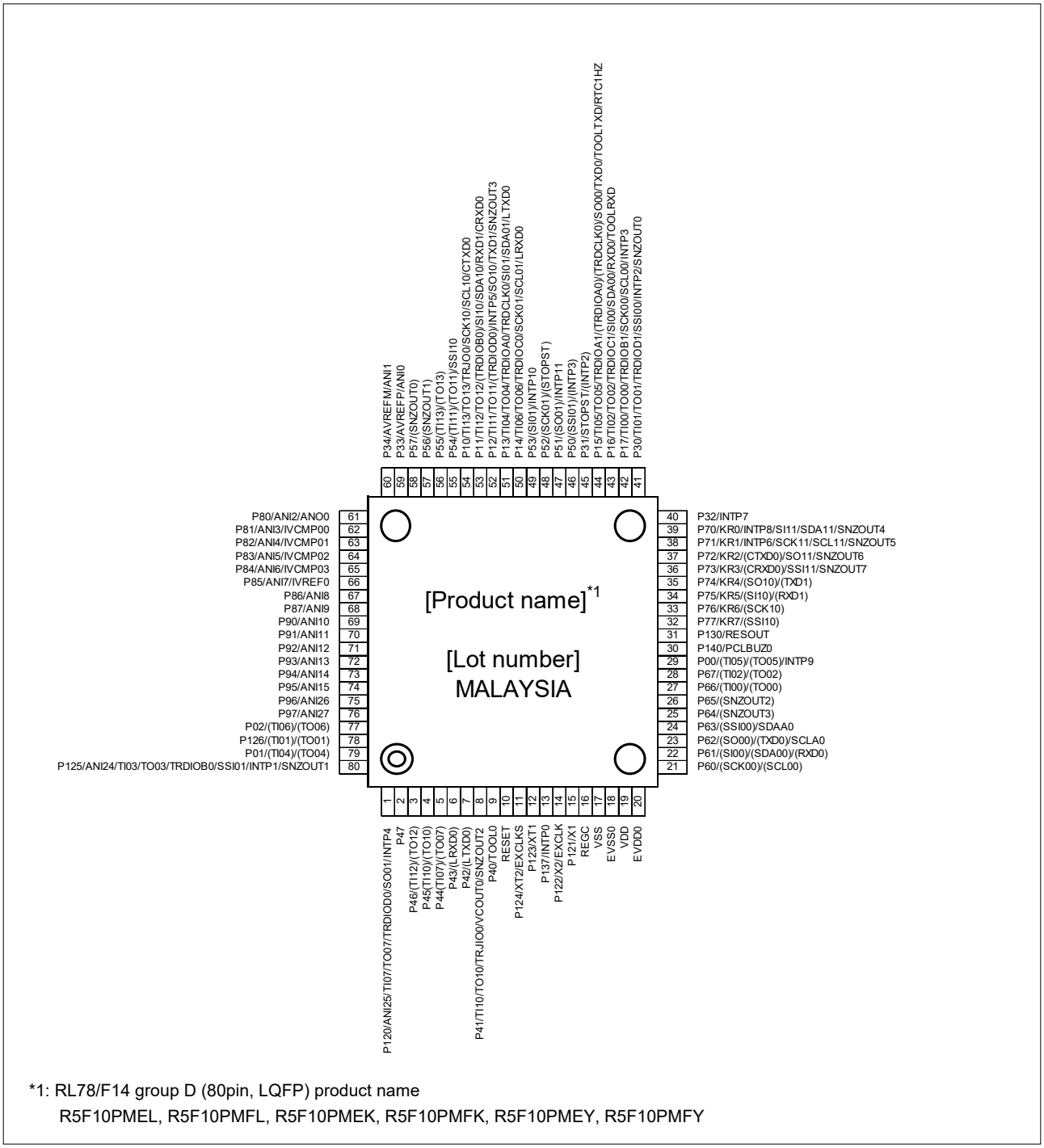
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P84	ANI6			(KR4)	
2		P85	ANI7			(KR5)	
3		P86	ANI8			(KR6)	
4		P87	ANI9			(KR7)	
5		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1
6		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
7		P41		TI10/TO10/TRJIO0			SNZOUT2
8	TOOL0	P40					
9	RESET						
10		P137				INTP0	
11	X2/EXCLK	P122					
12	X1	P121					
13	REGC						
14	VSS						
15	VDD						
16		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
17		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
18		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
19		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
20		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
21		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
22		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
23		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
24		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
25		P33	AVREFP/ANI0				
26		P34	AVREFM/ANI1				
27		P80	ANI2			(KR0)	
28		P81	ANI3			(KR1)	
29		P82	ANI4			(KR2)	
30		P83	ANI5			(KR3)	

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

5. RL78/F14 pin assignment for Group D products

The pin configuration and pin assignment for Group D products of RL78/F14 are illustrated and listed according to the number of pins included.

5.1 Group D products (80 pins) of RL78/F14



*1: RL78/F14 group D (80pin, LQFP) product name
R5F10PMEL, R5F10PMFL, R5F10PMEK, R5F10PMFK, R5F10PMEY, R5F10PMFY

Figure 5.1 RL78/F14 pin configuration for Group D products (80 pins)

Table 5.1 RL78/F14 pin assignment for Group D products (80 pins) (1/2)

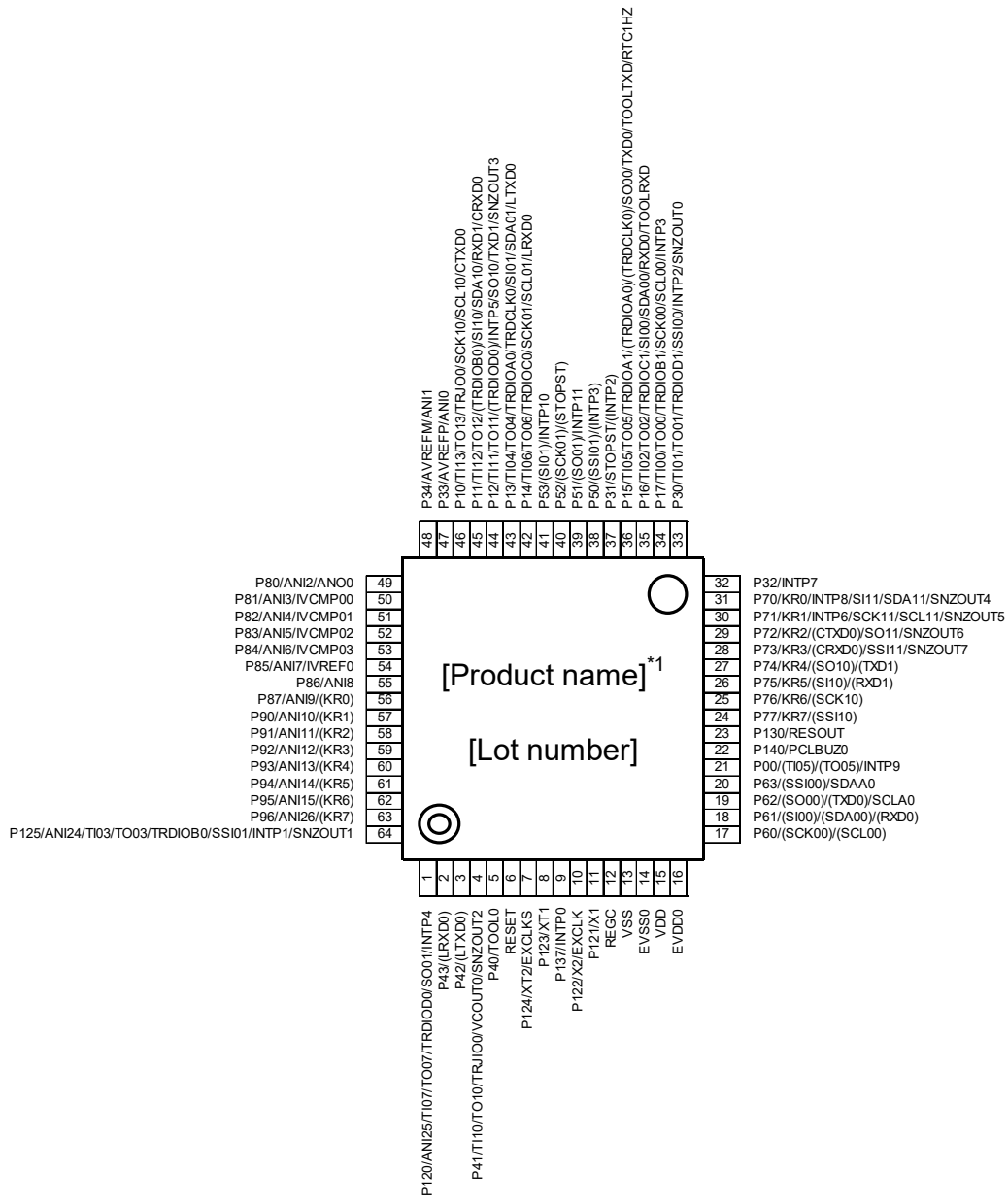
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P47					
3		P46		(TI12)/(TO12)			
4		P45		(TI10)/(TO10)			
5		P44		(TI07)/(TO07)			
6		P43			(LRXD0)		
7		P42			(LTXD0)		
8		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
9	TOOL0	P40					
10	RESET						
11	XT2/EXCLKS	P124					
12	XT1	P123					
13		P137				INTP0	
14	X2/EXCLK	P122					
15	X1	P121					
16	REGC						
17	VSS						
18	EVSS0						
19	VDD						
20	EVDD0						
21		P60			(SCK00)/(SCL00)		
22		P61			(SI00)/(SDA00)/(RXD0)		
23		P62			(SO00)/(TXD0)/SCLA0		
24		P63			(SSI00)/SDAA0		
25		P64					(SNZOUT3)
26		P65					(SNZOUT2)
27		P66		(TI00)/(TO00)			
28		P67		(TI02)/(TO02)			
29		P00		(TI05)/(TO05)		INTP9	
30		P140					PCLBUZ0
31		P130					RESOUT
32		P77			(SSI10)	KR7	
33		P76			(SCK10)	KR6	
34		P75			(SI10)/(RXD1)	KR5	
35		P74			(SO10)/(TXD1)	KR4	
36		P73			(CRXD0)/SSI11	KR3	SNZOUT7
37		P72			(CTXD0)/SO11	KR2	SNZOUT6
38		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
39		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
40		P32				INTP7	
41		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
42		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
43		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
44		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
45		P31				(INTP2)	STOPST
46		P50			(SSI01)	(INTP3)	
47		P51			(SO01)	INTP11	
48		P52			(SCK01)		(STOPST)
49		P53			(SI01)	INTP10	
50		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
51		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
52		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
53		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
54		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
55		P54		(TI11)/(TO11)	SSI10		
56		P55		(TI13)/(TO13)			

Table 5.1 RL78/F14 pin assignment for Group D products (80 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
57		P56					(SNZOUT1)
58		P57					(SNZOUT0)
59		P33	AVREFP/ANI0				
60		P34	AVREFM/ANI1				
61		P80	ANI2/ANO0				
62		P81	ANI3/IVCMP00				
63		P82	ANI4/IVCMP01				
64		P83	ANI5/IVCMP02				
65		P84	ANI6/IVCMP03				
66		P85	ANI7/IVREF0				
67		P86	ANI8				
68		P87	ANI9				
69		P90	ANI10				
70		P91	ANI11				
71		P92	ANI12				
72		P93	ANI13				
73		P94	ANI14				
74		P95	ANI15				
75		P96	ANI26				
76		P97	ANI27				
77		P02		(TI06)/(TO06)			
78		P126		(TI01)/(TO01)			
79		P01		(TI04)/(TO04)			
80		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

5.2 Group D products (64 pins) of RL78/F14



*1: RL78/F14 group D (64pin, LQFP) product name
R5F10PLEL, R5F10PLFL, R5F10PLEK, R5F10PLFK, R5F10PLEY, R5F10PLFY

Figure 5.2 RL78/F14 pin configuration for Group D products (64 pins)

Table 5.2 RL78/F14 pin assignment for Group D products (64 pins) (1/2)

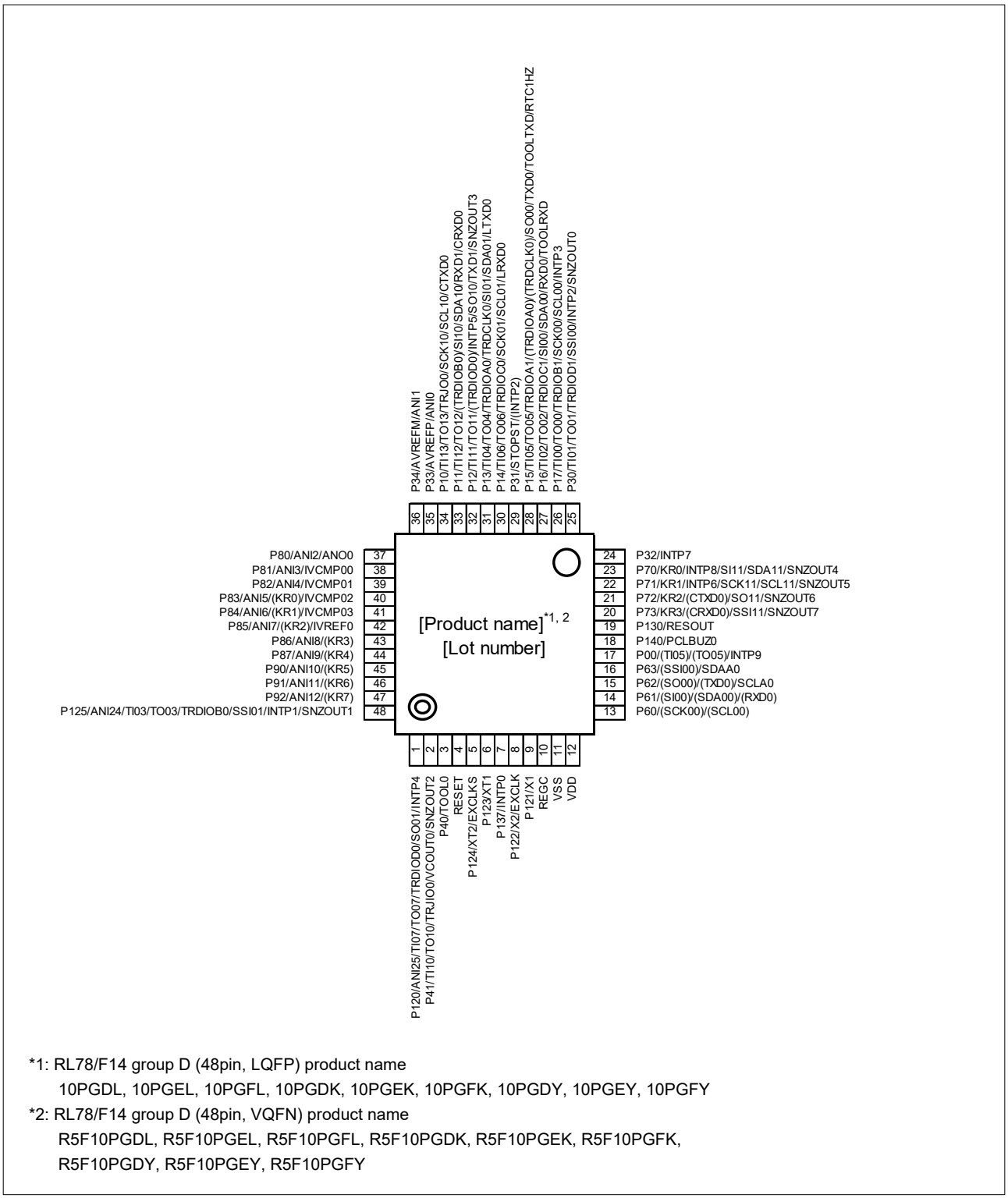
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P43			(LRXD0)		
3		P42			(LTXD0)		
4		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
5	TOOL0	P40					
6	RESET						
7	XT2/EXCLKS	P124					
8	XT1	P123					
9		P137				INTP0	
10	X2/EXCLK	P122					
11	X1	P121					
12	REGC						
13	VSS						
14	EVSS0						
15	VDD						
16	EVDD0						
17		P60			(SCK00)/(SCL00)		
18		P61			(SI00)/(SDA00)/(RXD0)		
19		P62			(SO00)/(TXD0)/SCLA0		
20		P63			(SSI00)/SDAA0		
21		P00		(TI05)/(TO05)		INTP9	
22		P140					PCLBUZ0
23		P130					RESOUT
24		P77			(SSI10)	KR7	
25		P76			(SCK10)	KR6	
26		P75			(SI10)/(RXD1)	KR5	
27		P74			(SO10)/(TXD1)	KR4	
28		P73			(CRXD0)/SSI11	KR3	SNZOUT7
29		P72			(CTXD0)/SO11	KR2	SNZOUT6
30		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
31		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
32		P32				INTP7	
33		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
34		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
35		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
36		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
37		P31				(INTP2)	STOPST
38		P50			(SSI01)	(INTP3)	
39		P51			(SO01)	INTP11	
40		P52			(SCK01)		(STOPST)
41		P53			(SI01)	INTP10	
42		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
43		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
44		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
45		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
46		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
47		P33	AVREFP/ANI0				
48		P34	AVREFM/ANI1				
49		P80	ANI2/ANO0				
50		P81	ANI3/IVCMP00				
51		P82	ANI4/IVCMP01				
52		P83	ANI5/IVCMP02				
53		P84	ANI6/IVCMP03				
54		P85	ANI7/IVREF0				
55		P86	ANI8				

Table 5.2 RL78/F14 pin assignment for Group D products (64 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
56		P87	ANI9			(KR0)	
57		P90	ANI10			(KR1)	
58		P91	ANI11			(KR2)	
59		P92	ANI12			(KR3)	
60		P93	ANI13			(KR4)	
61		P94	ANI14			(KR5)	
62		P95	ANI15			(KR6)	
63		P96	ANI26			(KR7)	
64		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

5.3 Group D products (48 pins) of RL78/F14



*1: RL78/F14 group D (48pin, LQFP) product name
10PGDL, 10PGEL, 10PGFL, 10PGDK, 10PGEK, 10PGFK, 10PGDY, 10PGEY, 10PGFY

*2: RL78/F14 group D (48pin, VQFN) product name
R5F10PGDL, R5F10PGEL, R5F10PGFL, R5F10PGDK, R5F10PGEK, R5F10PGFK,
R5F10PGDY, R5F10PGEY, R5F10PGFY

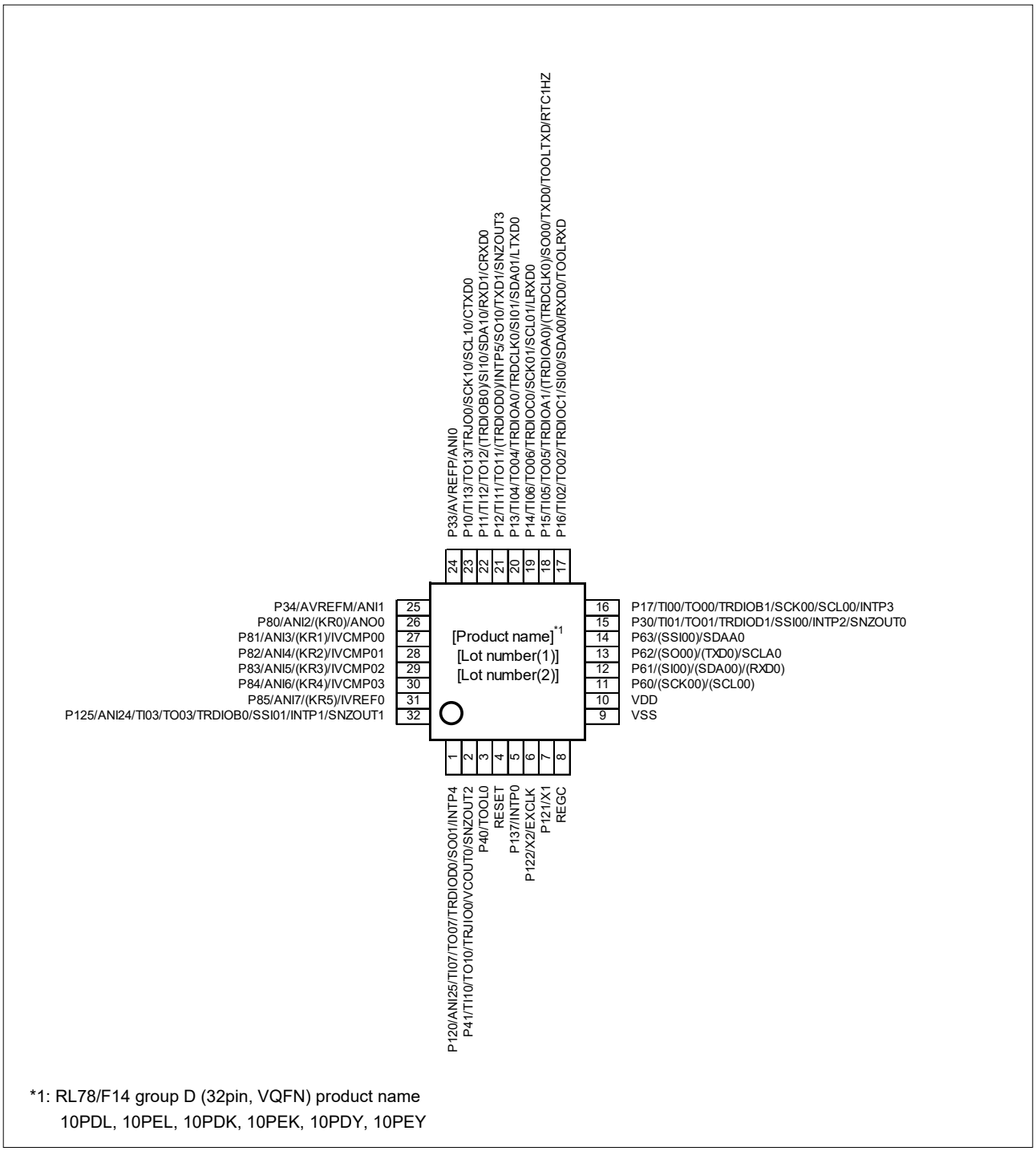
Figure 5.3 RL78/F14 pin configuration for Group D products (48 pins)

Table 5.3 RL78/F14 pin assignment for Group D products (48 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5	XT2/EXCLKS	P124					
6	XT1	P123					
7		P137				INTP0	
8	X2/EXCLK	P122					
9	X1	P121					
10	REGC						
11	VSS						
12	VDD						
13		P60			(SCK00)/(SCL00)		
14		P61			(SI00)/(SDA00)/(RXD0)		
15		P62			(SO00)/(TXD0)/SCLA0		
16		P63			(SSI00)/SDAA0		
17		P00		(TI05)/(TO05)		INTP9	
18		P140					PCLBUZ0
19		P130					RESOUT
20		P73			(CRXD0)/SSI11	KR3	SNZOUT7
21		P72			(CTXD0)/SO11	KR2	SNZOUT6
22		P71			SCK11/SCL11	KR1/INTP6	SNZOUT5
23		P70			SI11/SDA11	KR0/INTP8	SNZOUT4
24		P32				INTP7	
25		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
26		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
27		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
28		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
29		P31				(INTP2)	STOPST
30		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
31		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
32		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
33		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
34		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
35		P33	AVREFP/ANI0				
36		P34	AVREFM/ANI1				
37		P80	ANI2/ANO0				
38		P81	ANI3/IVCMP00				
39		P82	ANI4/IVCMP01				
40		P83	ANI5/IVCMP02			(KR0)	
41		P84	ANI6/IVCMP03			(KR1)	
42		P85	ANI7/IVREF0			(KR2)	
43		P86	ANI8			(KR3)	
44		P87	ANI9			(KR4)	
45		P90	ANI10			(KR5)	
46		P91	ANI11			(KR6)	
47		P92	ANI12			(KR7)	
48		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

5.4 Group D products (32 pins) of RL78/F14



*1: RL78/F14 group D (32pin, VQFN) product name
10PDL, 10PEL, 10PDK, 10PEK, 10PDY, 10PEY

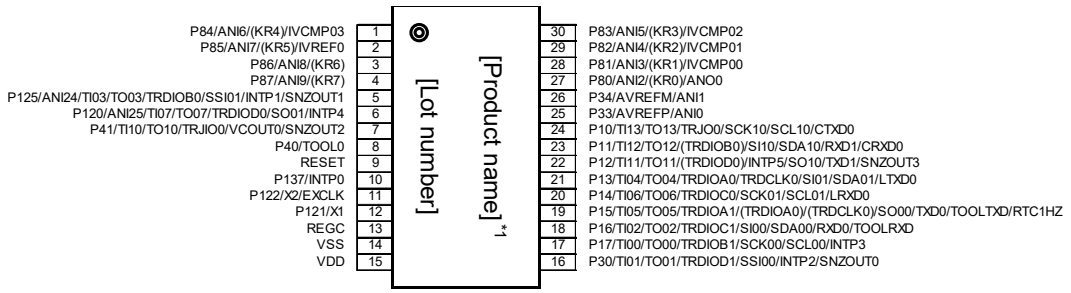
Figure 5.4 RL78/F14 pin configuration for Group D products (32 pins)

Table 5.4 RL78/F14 pin assignment for Group D products (32 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5		P137				INTP0	
6	X2/EXCLK	P122					
7	X1	P121					
8	REGC						
9	VSS						
10	VDD						
11		P60			(SCK00)/(SCL00)		
12		P61			(SI00)/(SDA00)/(RXD0)		
13		P62			(SO00)/(TXD0)/SCLA0		
14		P63			(SSI00)/SDAA0		
15		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
16		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
17		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
18		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
19		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
20		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
21		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
22		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
23		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
24		P33	AVREFP/ANI0				
25		P34	AVREFM/ANI1				
26		P80	ANI2/ANO0			(KR0)	
27		P81	ANI3/IVCMP00			(KR1)	
28		P82	ANI4/IVCMP01			(KR2)	
29		P83	ANI5/IVCMP02			(KR3)	
30		P84	ANI6/IVCMP03			(KR4)	
31		P85	ANI7/IVREF0			(KR5)	
32		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

5.5 Group D products (30 pins) of RL78/F14



*1: RL78/F14 group D (30pin, SSOP) product name
R5F10PADL, R5F10PAEL, R5F10PADK, R5F10PAEK, R5F10PADY, R5F10PAEY

Figure 5.5 RL78/F14 pin configuration for Group D products (30 pins)

Table 5.5 RL78/F14 pin assignment for Group D products (30 pins)

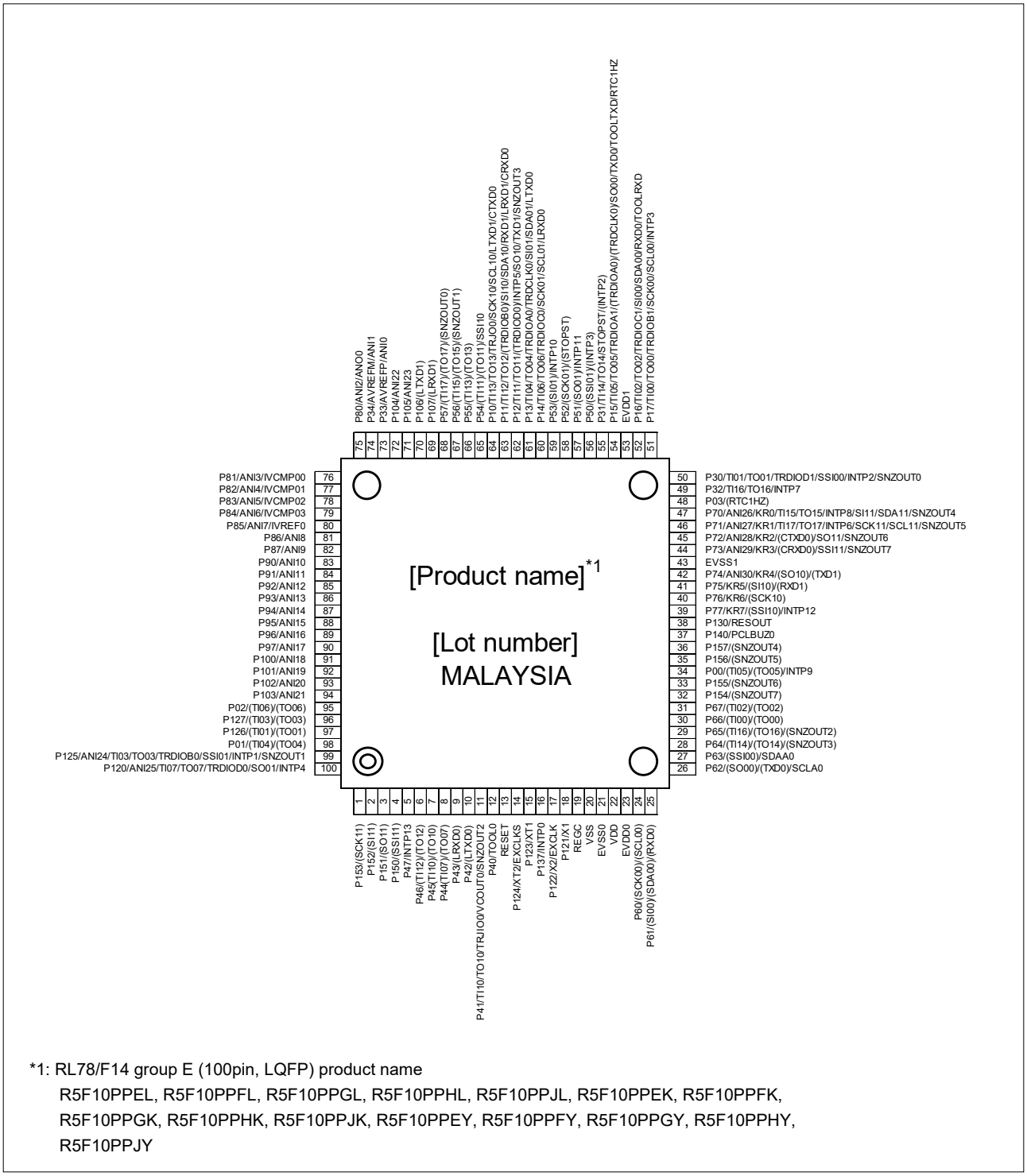
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P84	ANI6/IVCMP03			(KR4)	
2		P85	ANI7/IVREF0			(KR5)	
3		P86	ANI8			(KR6)	
4		P87	ANI9			(KR7)	
5		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1
6		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
7		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
8	TOOL0	P40					
9	RESET						
10		P137				INTP0	
11	X2/EXCLK	P122					
12	X1	P121					
13	REGC						
14	VSS						
15	VDD						
16		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
17		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
18		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
19		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
20		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
21		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
22		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
23		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/CRXD0		
24		P10		TI13/TO13/TRJO0	SCK10/SCL10/CTXD0		
25		P33	AVREFP/ANI0				
26		P34	AVREFM/ANI1				
27		P80	ANI2/ANO0			(KR0)	
28		P81	ANI3/IVCMP00			(KR1)	
29		P82	ANI4/IVCMP01			(KR2)	
30		P83	ANI5/IVCMP02			(KR3)	

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

6. RL78/F14 pin assignment for Group E products

The pin configuration and pin assignment for Group E products of RL78/F14 are illustrated and listed according to the number of pins used.

6.1 Group E products (100 pins) of RL78/F14



*1: RL78/F14 group E (100pin, LQFP) product name
R5F10PPEL, R5F10PPFL, R5F10PPGL, R5F10PPHL, R5F10PPJL, R5F10PPEK, R5F10PPFK, R5F10PPGK, R5F10PPHK, R5F10PPJK, R5F10PPEY, R5F10PPFY, R5F10PPGY, R5F10PPHY, R5F10PPJY

Figure 6.1 RL78/F14 pin configuration for Group E products (100 pins)

Table 6.1 RL78/F14 pin assignment for Group E (100 pins) (1/2)

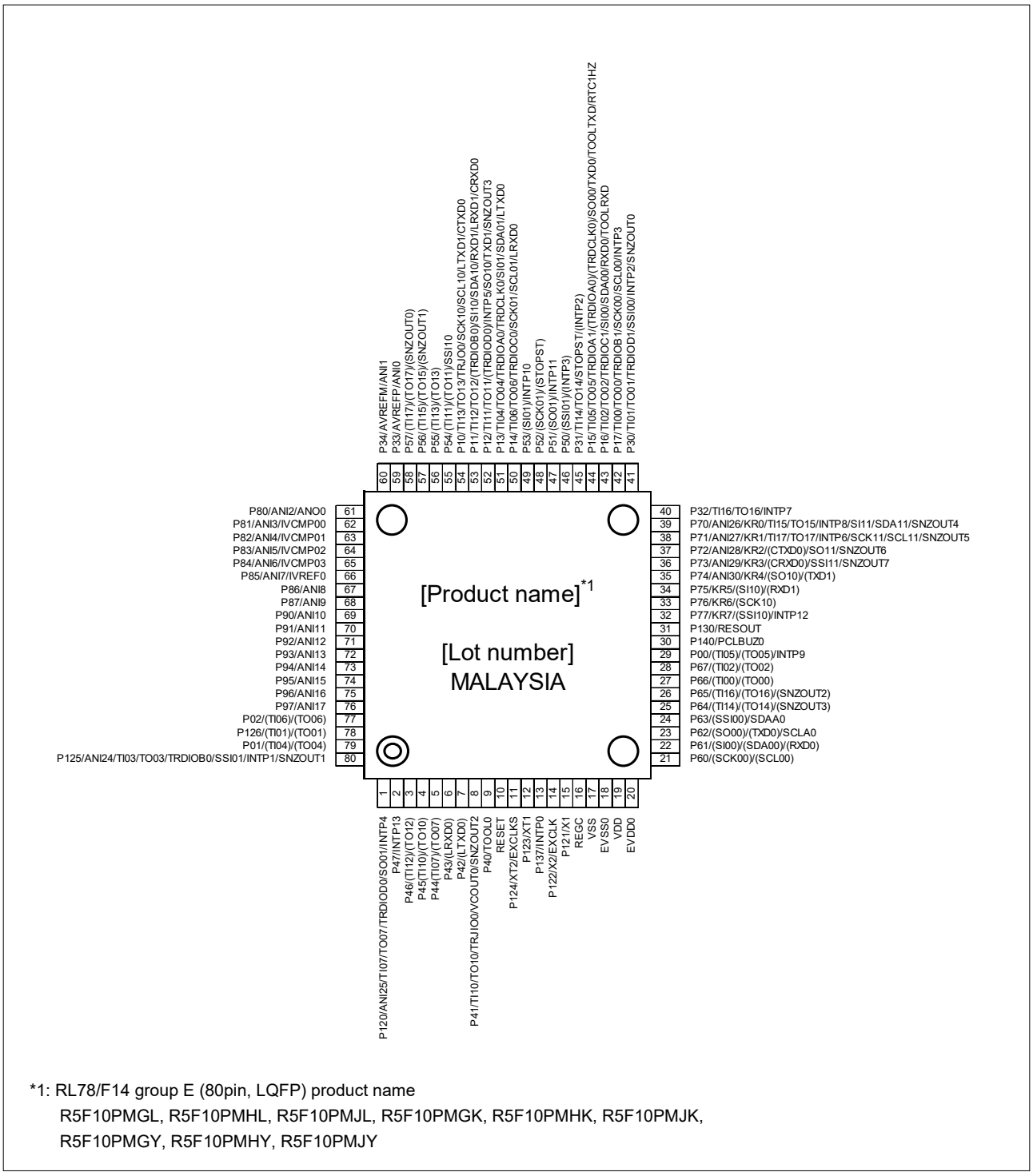
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P153			(SCK11)		
2		P152			(SI11)		
3		P151			(SO11)		
4		P150			(SSI11)		
5		P47				INTP13	
6		P46		(TI12)/(TO12)			
7		P45		(TI10)/(TO10)			
8		P44		(TI07)/(TO07)			
9		P43			(LRXD0)		
10		P42			(LTXD0)		
11		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
12	TOOL0	P40					
13	RESET						
14	XT2/EXCLKS	P124					
15	XT1	P123					
16		P137				INTP0	
17	X2/EXCLK	P122					
18	X1	P121					
19	REGC						
20	VSS						
21	EVSS0						
22	VDD						
23	EVDD0						
24		P60			(SCK00)/(SCL00)		
25		P61			(SI00)/(SDA00)/(RXD0)		
26		P62			(SO00)/(TXD0)/SCLA0		
27		P63			(SSI00)/SDAA0		
28		P64		(TI14)/(TO14)			(SNZOUT3)
29		P65		(TI16)/(TO16)			(SNZOUT2)
30		P66		(TI00)/(TO00)			
31		P67		(TI02)/(TO02)			
32		P154					(SNZOUT7)
33		P155					(SNZOUT6)
34		P00		(TI05)/(TO05)		INTP9	
35		P156					(SNZOUT5)
36		P157					(SNZOUT4)
37		P140					PCLBUZ0
38		P130					RESOUT
39		P77			(SSI10)	KR7/INTP12	
40		P76			(SCK10)	KR6	
41		P75			(SI10)/(RXD1)	KR5	
42		P74	ANI30		(SO10)/(TXD1)	KR4	
43	EVSS1						
44		P73	ANI29		(CRXD0)/SSI11	KR3	SNZOUT7
45		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
46		P71	ANI27	TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
47		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
48		P03					(RTC1HZ)
49		P32		TI16/TO16		INTP7	
50		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
51		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
52		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
53	EVDD1						
54		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
55		P31		TI14/TO14		(INTP2)	STOPST
56		P50			(SSI01)	(INTP3)	
57		P51			(SO01)	INTP11	

Table 6.1 RL78/F14 pin assignment for Group E (100 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
58		P52			(SCK01)		(STOPST)
59		P53			(SI01)	INTP10	
60		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
61		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
62		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
63		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/LRXD1/ CRXD0		
64		P10		TI13/TO13/TRJO0	SCK10/SCL10/LTXD1/CTXD0		
65		P54		(TI11)/(TO11)	SSI10		
66		P55		(TI13)/(TO13)			
67		P56		(TI15)/(TO15)			(SNZOUT1)
68		P57		(TI17)/(TO17)			(SNZOUT0)
69		P107			(LRXD1)		
70		P106			(LTXD1)		
71		P105	ANI23				
72		P104	ANI22				
73		P33	AVREFP/ANI0				
74		P34	AVREFM/ANI1				
75		P80	ANI2/ANO0				
76		P81	ANI3/IVCMP00				
77		P82	ANI4/IVCMP01				
78		P83	ANI5/IVCMP02				
79		P84	ANI6/IVCMP03				
80		P85	ANI7/IVREF0				
81		P86	ANI8				
82		P87	ANI9				
83		P90	ANI10				
84		P91	ANI11				
85		P92	ANI12				
86		P93	ANI13				
87		P94	ANI14				
88		P95	ANI15				
89		P96	ANI16				
90		P97	ANI17				
91		P100	ANI18				
92		P101	ANI19				
93		P102	ANI20				
94		P103	ANI21				
95		P02		(TI06)/(TO06)			
96		P127		(TI03)/(TO03)			
97		P126		(TI01)/(TO01)			
98		P01		(TI04)/(TO04)			
99		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1
100		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

6.2 Group E products (80 pins) of RL78/F14



*1: RL78/F14 group E (80pin, LQFP) product name
R5F10PMGL, R5F10PMHL, R5F10PMJL, R5F10PMGK, R5F10PMHK, R5F10PMJK,
R5F10PMGY, R5F10PMHY, R5F10PMJY

Figure 6.2 RL78/F14 pin configuration for Group E products (80 pins)

Table 6.2 RL78/F14 pin assignment for Group E products (80 pins) (1/2)

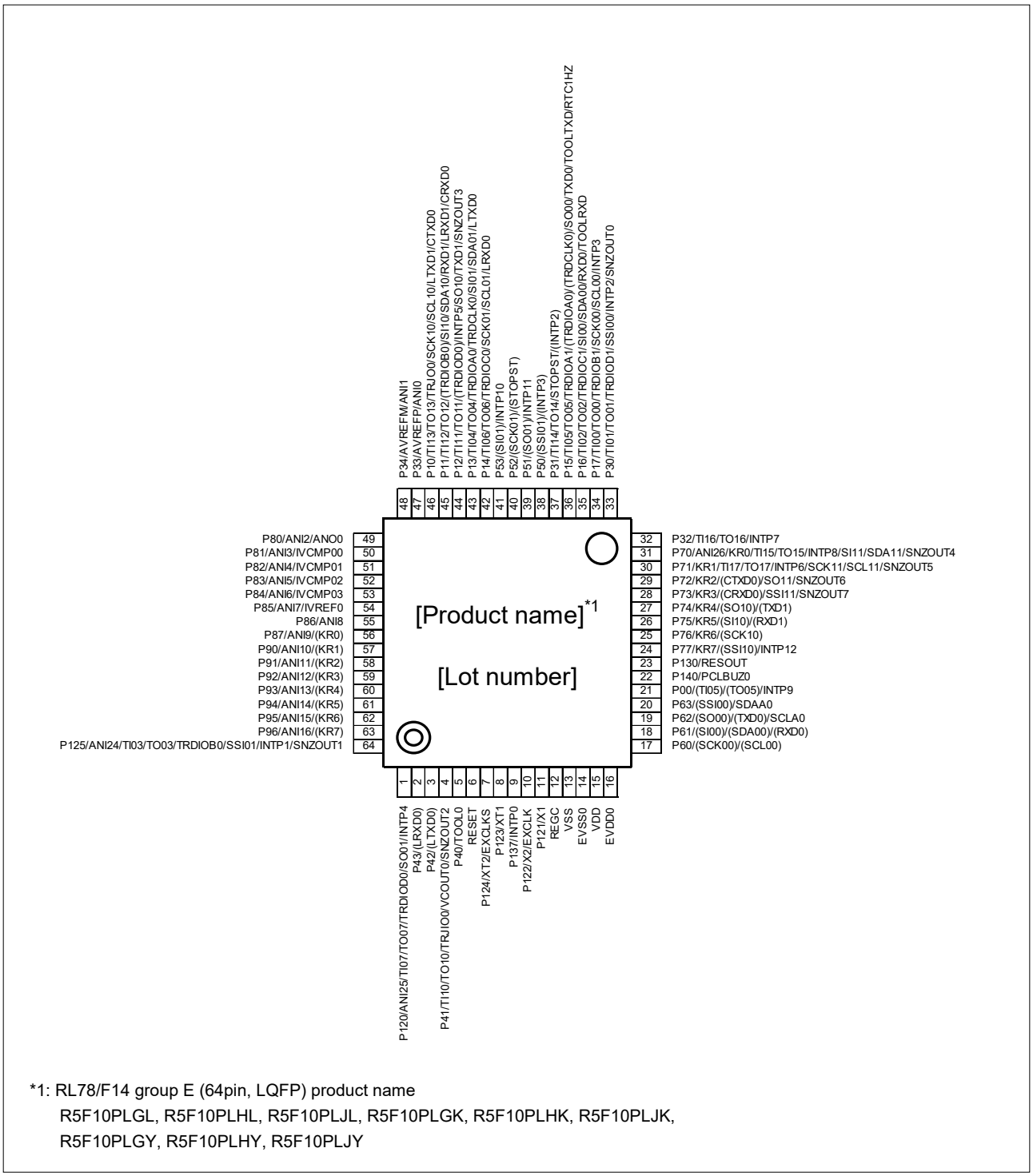
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P47				INTP13	
3		P46		(TI12)/(TO12)			
4		P45		(TI10)/(TO10)			
5		P44		(TI07)/(TO07)			
6		P43			(LRXD0)		
7		P42			(LTXD0)		
8		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
9	TOOL0	P40					
10	RESET						
11	XT2/EXCLKS	P124					
12	XT1	P123					
13		P137				INTP0	
14	X2/EXCLK	P122					
15	X1	P121					
16	REGC						
17	VSS						
18	EVSS0						
19	VDD						
20	EVDD0						
21		P60			(SCK00)/(SCL00)		
22		P61			(SI00)/(SDA00)/(RXD0)		
23		P62			(SO00)/(TXD0)/SCLA0		
24		P63			(SSI00)/SDAA0		
25		P64		(TI14)/(TO14)			(SNZOUT3)
26		P65		(TI16)/(TO16)			(SNZOUT2)
27		P66		(TI00)/(TO00)			
28		P67		(TI02)/(TO02)			
29		P00		(TI05)/(TO05)		INTP9	
30		P140					PCLBUZ0
31		P130					RESOUT
32		P77			(SSI10)	KR7/INTP12	
33		P76			(SCK10)	KR6	
34		P75			(SI10)/(RXD1)	KR5	
35		P74	ANI30		(SO10)/(TXD1)	KR4	
36		P73	ANI29		(CRXD0)/SSI11	KR3	SNZOUT7
37		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
38		P71	ANI27	TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
39		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
40		P32		TI16/TO16		INTP7	
41		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
42		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
43		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
44		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
45		P31		TI14/TO14		(INTP2)	STOPST
46		P50			(SSI01)	(INTP3)	
47		P51			(SO01)	INTP11	
48		P52			(SCK01)		(STOPST)
49		P53			(SI01)	INTP10	
50		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
51		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
52		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
53		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/LRXD1/ CRXD0		
54		P10		TI13/TO13/TRJO0	SCK10/SCL10/LTXD1/CTXD0		
55		P54		(TI11)/(TO11)	SSI10		
56		P55		(TI13)/(TO13)			

Table 6.2 RL78/F14 pin assignment for Group E products (80 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
57		P56		(TI15)/(TO15)			(SNZOUT1)
58		P57		(TI17)/(TO17)			(SNZOUT0)
59		P33	AVREFP/ANI0				
60		P34	AVREFM/ANI1				
61		P80	ANI2/ANO0				
62		P81	ANI3/IVCMP00				
63		P82	ANI4/IVCMP01				
64		P83	ANI5/IVCMP02				
65		P84	ANI6/IVCMP03				
66		P85	ANI7/IVREF0				
67		P86	ANI8				
68		P87	ANI9				
69		P90	ANI10				
70		P91	ANI11				
71		P92	ANI12				
72		P93	ANI13				
73		P94	ANI14				
74		P95	ANI15				
75		P96	ANI16				
76		P97	ANI17				
77		P02		(TI06)/(TO06)			
78		P126		(TI01)/(TO01)			
79		P01		(TI04)/(TO04)			
80		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

6.3 Group E products (64 pins) of RL78/F14



*1: RL78/F14 group E (64pin, LQFP) product name
R5F10PLGL, R5F10PLHL, R5F10PLJL, R5F10PLGK, R5F10PLHK, R5F10PLJK,
R5F10PLGY, R5F10PLHY, R5F10PLJY

Figure 6.3 RL78/F14 pin configuration for Group E products (64 pins)

Table 6.3 RL78/F14 pin assignment for Group E products (64 pins) (1/2)

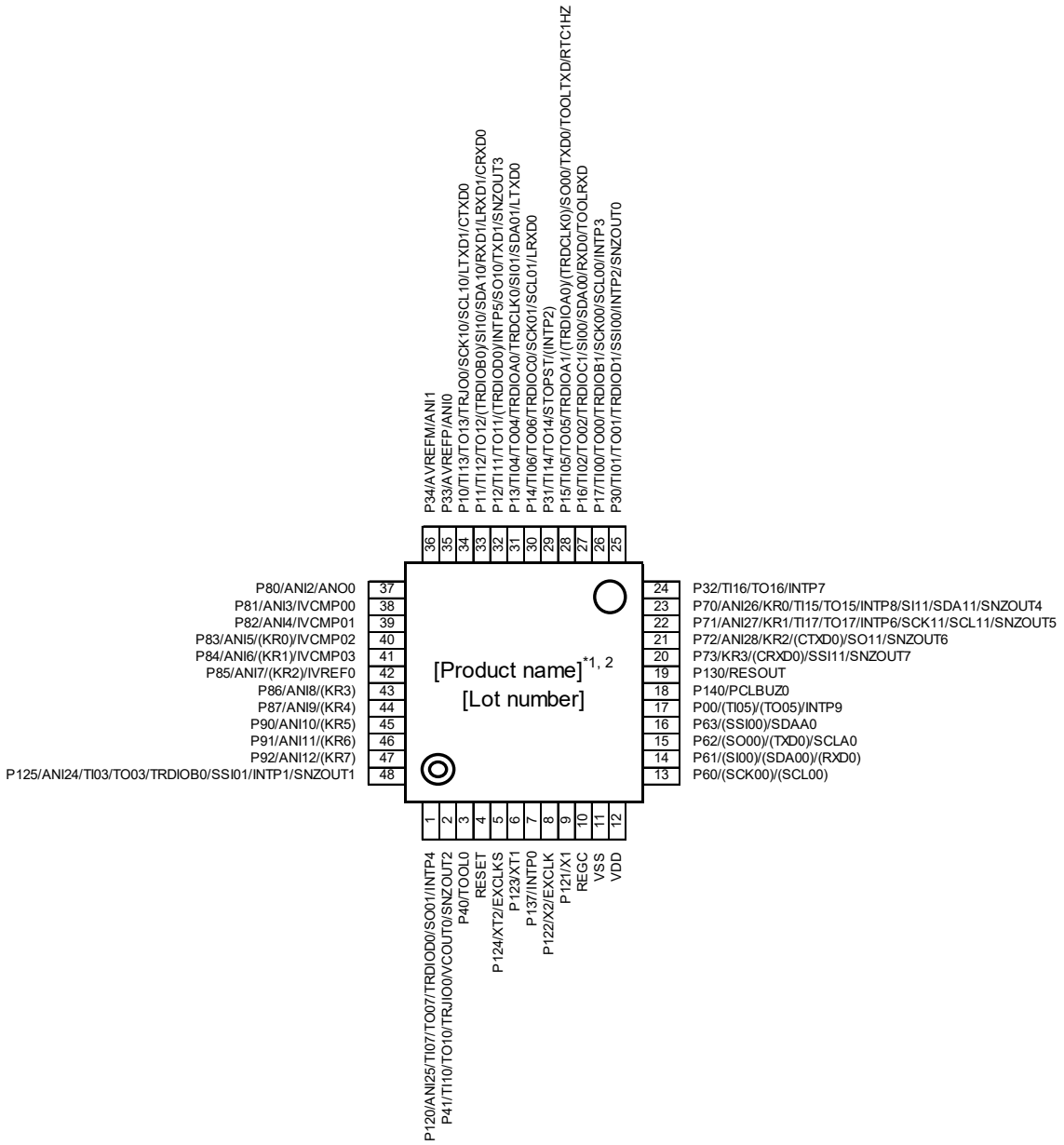
Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P43			(LRXD0)		
3		P42			(LTXD0)		
4		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
5	TOOL0	P40					
6	RESET						
7	XT2/EXCLKS	P124					
8	XT1	P123					
9		P137				INTP0	
10	X2/EXCLK	P122					
11	X1	P121					
12	REGC						
13	VSS						
14	EVSS0						
15	VDD						
16	EVDD0						
17		P60			(SCK00)/(SCL00)		
18		P61			(SI00)/(SDA00)/(RXD0)		
19		P62			(SO00)/(TXD0)/SCLA0		
20		P63			(SSI00)/SDAA0		
21		P00		(TI05)/(TO05)		INTP9	
22		P140					PCLBUZ0
23		P130					RESOUT
24		P77			(SSI10)	KR7/INTP12	
25		P76			(SCK10)	KR6	
26		P75			(SI10)/(RXD1)	KR5	
27		P74			(SO10)/(TXD1)	KR4	
28		P73			(CRXD0)/SSI11	KR3	SNZOUT7
29		P72			(CTXD0)/SO11	KR2	SNZOUT6
30		P71		TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
31		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
32		P32		TI16/TO16		INTP7	
33		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
34		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
35		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
36		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
37		P31		TI14/TO14		(INTP2)	STOPST
38		P50			(SSI01)	(INTP3)	
39		P51			(SO01)	INTP11	
40		P52			(SCK01)		(STOPST)
41		P53			(SI01)	INTP10	
42		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
43		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
44		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
45		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/LRXD1/ CRXD0		
46		P10		TI13/TO13/TRJO0	SCK10/SCL10/LTXD1/CTXD0		
47		P33	AVREFP/ANI0				
48		P34	AVREFM/ANI1				
49		P80	ANI2/ANO0				
50		P81	ANI3/IVCMP00				
51		P82	ANI4/IVCMP01				
52		P83	ANI5/IVCMP02				
53		P84	ANI6/IVCMP03				
54		P85	ANI7/IVREF0				
55		P86	ANI8				

Table 6.3 RL78/F14 pin assignment for Group E products (64 pins) (2/2)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
56		P87	ANI9			(KR0)	
57		P90	ANI10			(KR1)	
58		P91	ANI11			(KR2)	
59		P92	ANI12			(KR3)	
60		P93	ANI13			(KR4)	
61		P94	ANI14			(KR5)	
62		P95	ANI15			(KR6)	
63		P96	ANI16			(KR7)	
64		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Cautions 1. The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.
2. Be sure to set the STPSTC register only when using the STOPST function.

6.4 Group E products (48 pins) of RL78/F14



*1: RL78/F14 group E (48pin, LQFP) product name
10PGGL, 10PGHL, 10PGJL, 10PGGK, 10PGHK, 10PGJK, 10PGGY, 10PGHY, 10PGJY

*2: RL78/F14 group E (48pin, VQFN) product name
R5F10PGGL, R5F10PGHL, R5F10PGJL, R5F10PGGK, R5F10PGHK, R5F10PGJK,
R5F10PGGY, R5F10PGHY, R5F10PGJY

Figure 6.4 RL78/F14 pin configuration for Group E products (48 pins)

Table 6.4 RL78/F14 pin assignment for Group E products (48 pins)

Pin	SYS	PORT	AD/DA/CMP	TAU/TRJ/TRD	SAU/CAN/LIN	INTP/KR	OTHER
1		P120	ANI25	TI07/TO07/TRDIOD0	SO01	INTP4	
2		P41	VCOUT0	TI10/TO10/TRJIO0			SNZOUT2
3	TOOL0	P40					
4	RESET						
5	XT2/EXCLKS	P124					
6	XT1	P123					
7		P137				INTP0	
8	X2/EXCLK	P122					
9	X1	P121					
10	REGC						
11	VSS						
12	VDD						
13		P60			(SCK00)/(SCL00)		
14		P61			(SI00)/(SDA00)/(RXD0)		
15		P62			(SO00)/(TXD0)/SCLA0		
16		P63			(SSI00)/SDAA0		
17		P00		(TI05)/(TO05)		INTP9	
18		P140					PCLBUZ0
19		P130					RESOUT
20		P73			(CRXD0)/SSI11	KR3	SNZOUT7
21		P72	ANI28		(CTXD0)/SO11	KR2	SNZOUT6
22		P71	ANI27	TI17/TO17	SCK11/SCL11	KR1/INTP6	SNZOUT5
23		P70	ANI26	TI15/TO15	SI11/SDA11	KR0/INTP8	SNZOUT4
24		P32		TI16/TO16		INTP7	
25		P30		TI01/TO01/TRDIOD1	SSI00	INTP2	SNZOUT0
26		P17		TI00/TO00/TRDIOB1	SCK00/SCL00	INTP3	
27		P16		TI02/TO02/TRDIOC1	SI00/SDA00/RXD0		TOOLRXD
28		P15		TI05/TO05/TRDIOA1/ (TRDIOA0)/(TRDCLK0)	SO00/TXD0		TOOLTXD/RTC1HZ
29		P31		TI14/TO14		(INTP2)	STOPST
30		P14		TI06/TO06/TRDIOC0	SCK01/SCL01/LRXD0		
31		P13		TI04/TO04/TRDIOA0/ TRDCLK0	SI01/SDA01/LTXD0		
32		P12		TI11/TO11/(TRDIOD0)	SO10/TXD1	INTP5	SNZOUT3
33		P11		TI12/TO12/(TRDIOB0)	SI10/SDA10/RXD1/LRXD1/ CRXD0		
34		P10		TI13/TO13/TRJO0	SCK10/SCL10/LTXD1/CTXD0		
35		P33	AVREFP/ANI0				
36		P34	AVREFM/ANI1				
37		P80	ANI2/ANO0				
38		P81	ANI3/IVCMP00				
39		P82	ANI4/IVCMP01				
40		P83	ANI5/IVCMP02			(KR0)	
41		P84	ANI6/IVCMP03			(KR1)	
42		P85	ANI7/IVREF0			(KR2)	
43		P86	ANI8			(KR3)	
44		P87	ANI9			(KR4)	
45		P90	ANI10			(KR5)	
46		P91	ANI11			(KR6)	
47		P92	ANI12			(KR7)	
48		P125	ANI24	TI03/TO03/TRDIOB0	SSI01	INTP1	SNZOUT1

Caution The pin functions indicated by the shaded are allocated to the multiple pins.
The functions in parentheses are not assigned after reset release.
Be sure to set the PIORx registers when using the function in parentheses.

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Revision History

Rev.	Date	Description	
		Page	Summary
Rev. 1.00	2014.12.15		1st edition
Rev. 1.01	2017. 6.30	3, 6, 8, 10, 11, 12, 15, 18, 20, 23, 26, 28, 30, 31, 34, 37, 39, 41, 42, 45, 48, 51	Updated all of the pin configuration figures

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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SALES OFFICES

Renesas Electronics Corporation

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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