# PCIe Gen 5 and 6 CC/SRIS/SRNS Clocking with VersaClock 7 Devices

VersaClock 7 (VC7) is Renesas latest family of configurable clock generators with an internal crystal oscillator for PCIe and networking applications in high-end computing, wired infrastructure, and data center equipment. This application note describes how to configure a VC7 device to operate in different modes to fit in PCIe common-clocking (CC) or independent clocking (IR) architectures.

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# 1. Introduction

PCIe stands for Peripheral Component Interconnect Express. It is an industry standard developed by the PCI Special Interest Group (PCI-SIG). PCIe was originally developed for data transfer between CPU and peripheral devices in PC motherboards. It has been adopted to a much broader scope of applications including blade servers, storage, embedded systems, and communication networks. PCIe has evolved multiple generations from its first debut of PCIe Gen 1.1 (in 2003) to PCIe Gen 5.0 (in 2019) and Gen 6.0 (in 2021).

PCIe systems use 100MHz, usually in HCSL format, as a reference clock (REFCLK) to transmit data between two PCIe devices. REFCLK is expected to meet ±300ppm stability in PCIe Gen 1-6 (±100ppm in PCIe Gen 5). The PCIe standard supports multiple clocking architectures that include Common Clock, Data Clock, Separate Reference Independent Spread (SRIS), and Separate Reference No Spread (SRNS).

The following list explains the Common Clock and Independent Reference (IR) clocking architectures:

- Common-Clocked (CC). The Root Complex (RC) and Endpoint (EP) devices use a common reference clock from the same PLL. If one of the clocks is from a zero delay buffer then both clocks are not from the same PLL and it is IR architecture. If the transport delay delta is greater than 12ns, it is considered IR architecture.
- Independent Reference (IR). The RC and EP devices use Independent reference clocks.
  - Separate Reference with Independent Spread (SRIS): The RC and EP may not each use spread modulation. If just one uses spread modulation, it is considered to be SRIS.
  - Separate Reference No Spread (SRNS): Neither the RC nor EP uses spread modulation.

Common clock is ubiquitous and is well defined. IR, on the other hand, has been discussed for years and is much more nebulous because the filtering functions limits have not been defined. It is up to the system design engineer to set the requirements. There are no specified limits. IR is driven by desire to not route clocks over cables and connectors especially for optical cables because of the additional cost. Spread Spectrum Clocking (SSC) complicates IR because larger data buffers are needed.

The following diagrams illustrate the different PCIe clocking architectures.

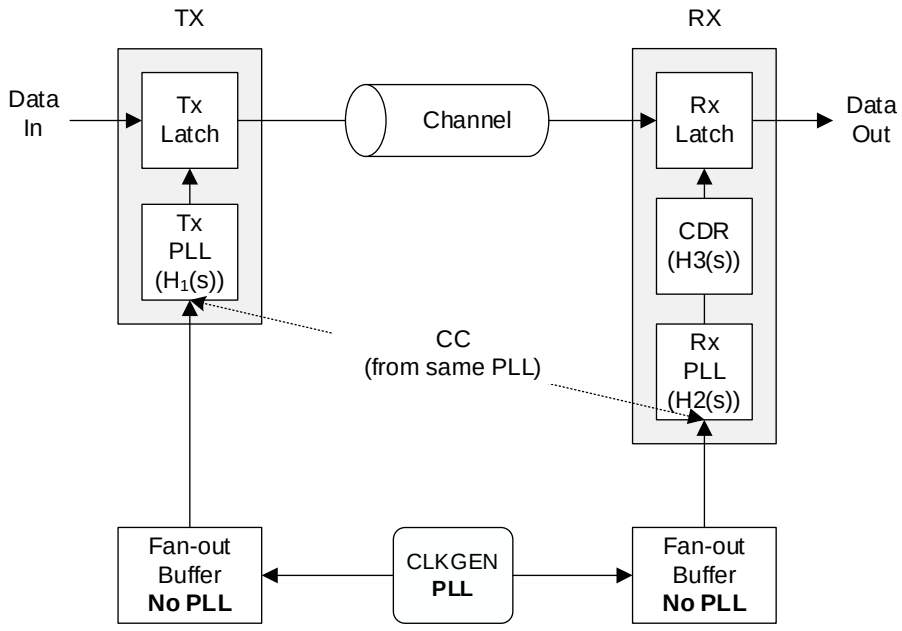


**Figure 1. Common REFCLK Architecture**

In Common clock architecture, clock channel additive jitter must be considered in overall jitter requirement budgeting. The following table shows the impact of clock channel additive jitter imposed on the REFCLK jitter specifications in order to meet PCIe receiver's input limit.

**Table 1. REFCLK Jitter Spec Definition with Clock Channel Additive Jitter in Common Clock Architecture**

| | Clock Out Jitter | Additive Channel Jitter | Receiver Input Limit |
|---|---|---|---|
| Gen 4 (ps, RMS) | 0.5 | 0.49 | 0.7 |
| Gen 5 (ps, RMS) | 0.15 | 0.20 | 0.25 |
| Gen 6 (ps, RMS) | 0.10 | 0.11 | 0.15 |

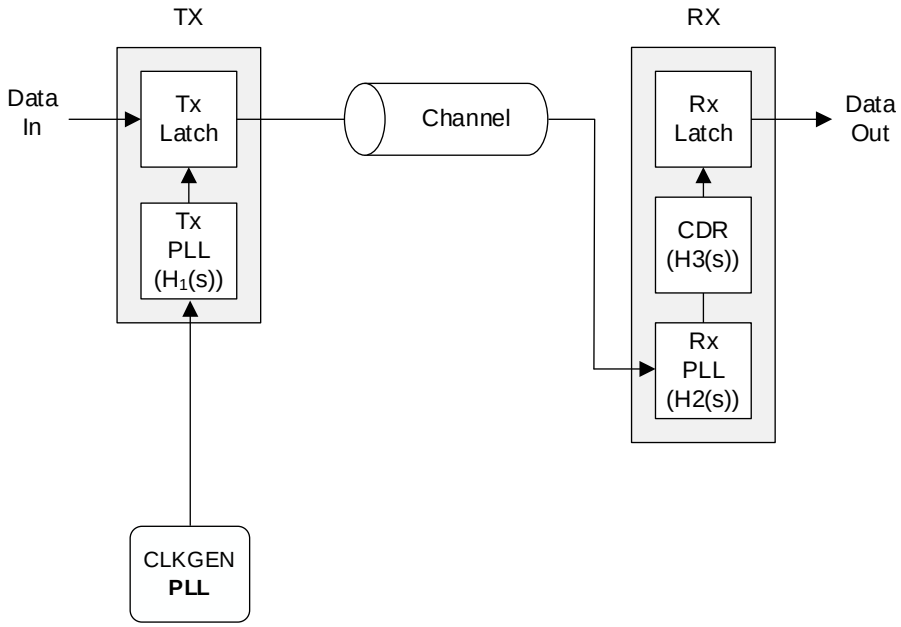


**Figure 2. Data Clock Architecture**

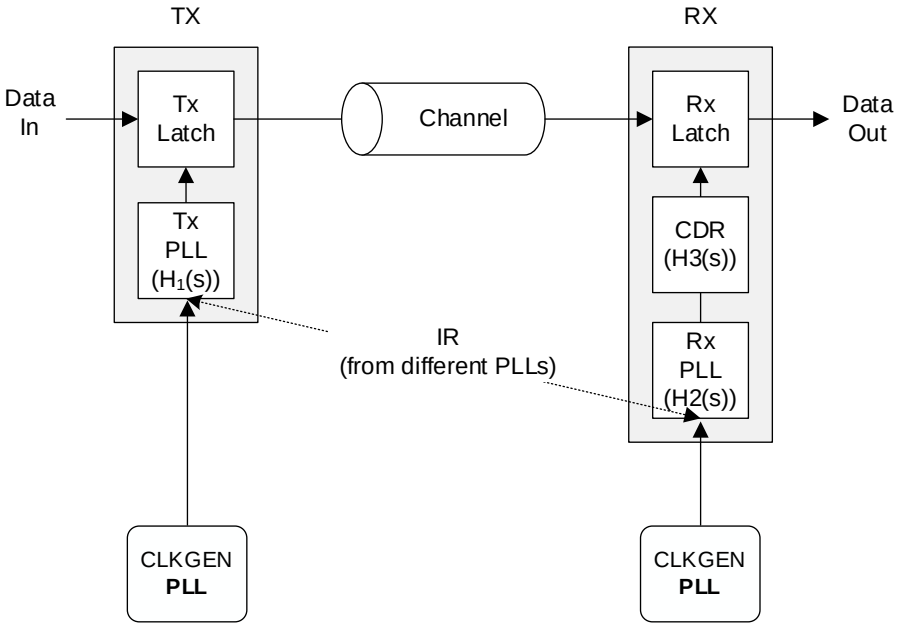


**Figure 3. IR Architecture 1: Separate Clock Generators**

Each may or may not use SSC. Additive channel is essentially none and can be ignored

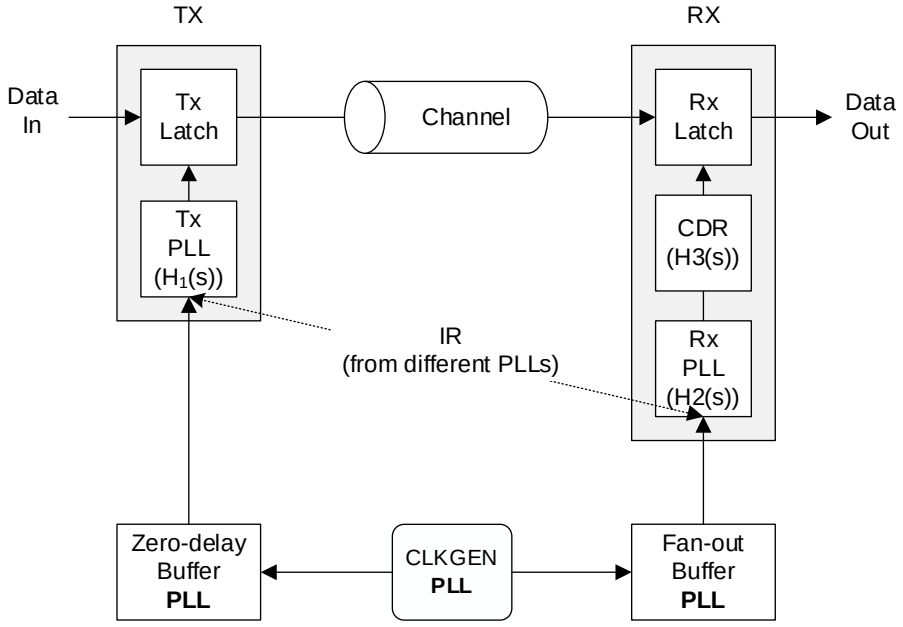


**Figure 4. IR Architecture 2: RC and EP Clocks are not from the Same PLL**

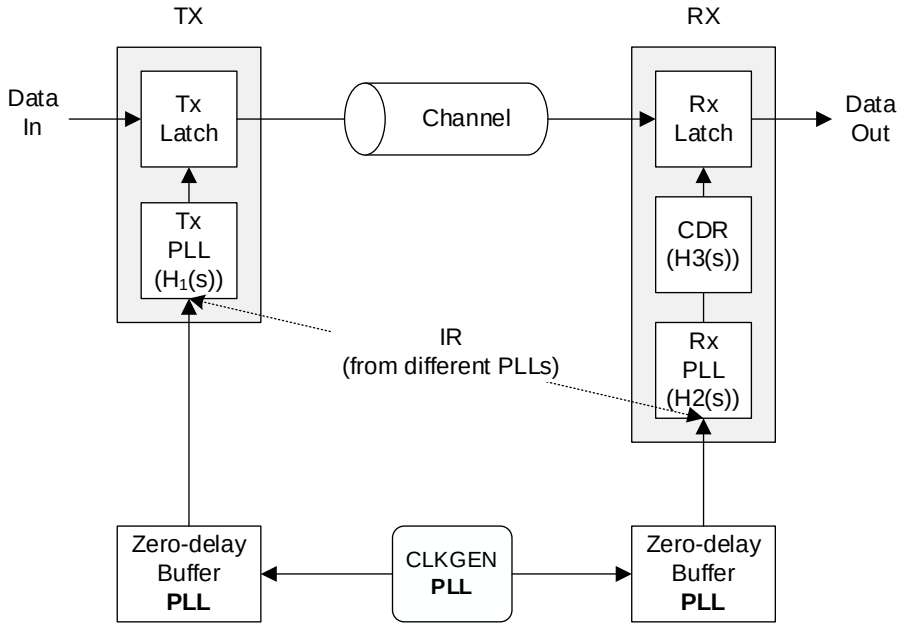


**Figure 5. IR Architecture 3: RC and EP Clocks are not from the Same PLL**

# 2. Using VersaClock 7 for CC and SRIS/SRNS Clocking

VC7 devices can be configured to operate in different modes to fit in PCIe common-clocking (CC) or independent reference (IR) architectures.

## 2.1 Synthesizer Mode

VC7 devices support synthesizer mode operation. When in synthesizer mode, a clock reference (either a crystal or an input clock) is required as the reference for APLL. Spread spectrum can be enabled on two spread-modulation engines: SS0 and SS1. SS0 is the clock source for FOD0 and SS1 for FOD1. The two spread-modulation engines can be separately configured.

As a result, a single VC7 device output can be used as an independent reference clock for RC or EP in SRIS or SRNS clocking.

Complete the following procedure to configure a VC7 device in synthesizer mode:

1. In the RICBox GUI, select Synthesizer mode in the **Operation Mode** box. For RC21008A or RC21012A, synthesizer mode is the only option. In RC31008A or RC31012A, select Synthesizer mode instead of JA mode.

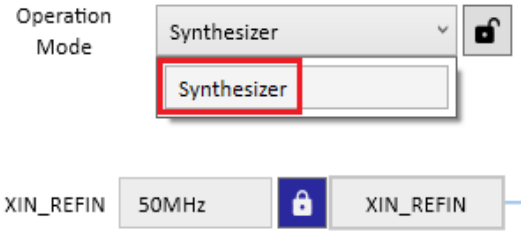


**Figure 6. Setting Operation Mode: Synthesizer Mode**

2. Configure an output (i.e., OUT1) as 100MHz, LP-HCSL. Choose IOD1 or FOD0 or FOD1. If spread is required, choose FOD0 or FOD1; otherwise, choose IOD1 for a performance premium (i.e., better phase noise).

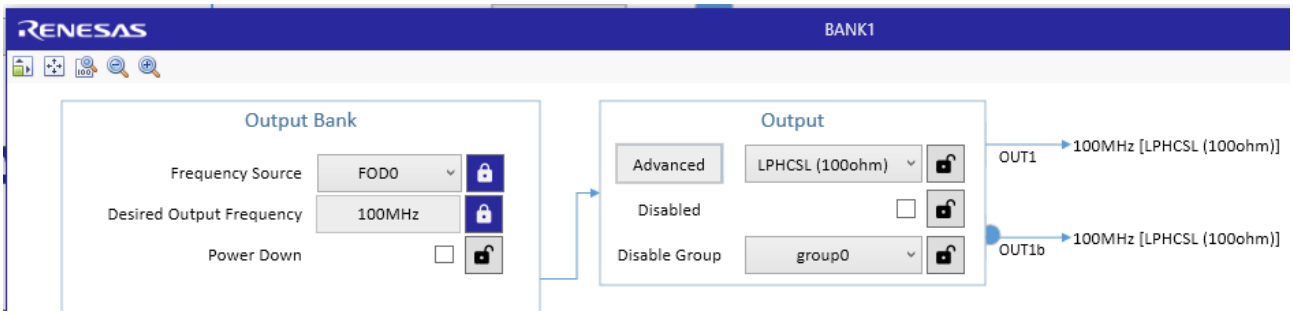


**Figure 7. Selecting Fractional/Integer Output Divider for an Output Clock**

3. If spread spectrum is required, enable Spread Spectrum.
   - Step 1 – Click on the setting button (the gear) on the side bar.
   - Step 2 – Select SSC tab on the top bar.
   - Step 3 – Select SS0 if spread spectrum is desired on output sourcing from FOD0; likewise, select FOD1 if spread spectrum is desired on output sourcing from FOD1.
     i. When SS0/SS1 is selected, enable the spread spectrum in the pull-down menu.
     ii. Select Down spread (default) or Center spread from the “ssc_mode” selections.
     iii. Enter the amount of the spread “percent_spread_fod0” box. Enter 0.005 for 0.5%, 0.0025 for 0.25% and so forth. No sign is needed as “down spread” or “center spread” is specified above.

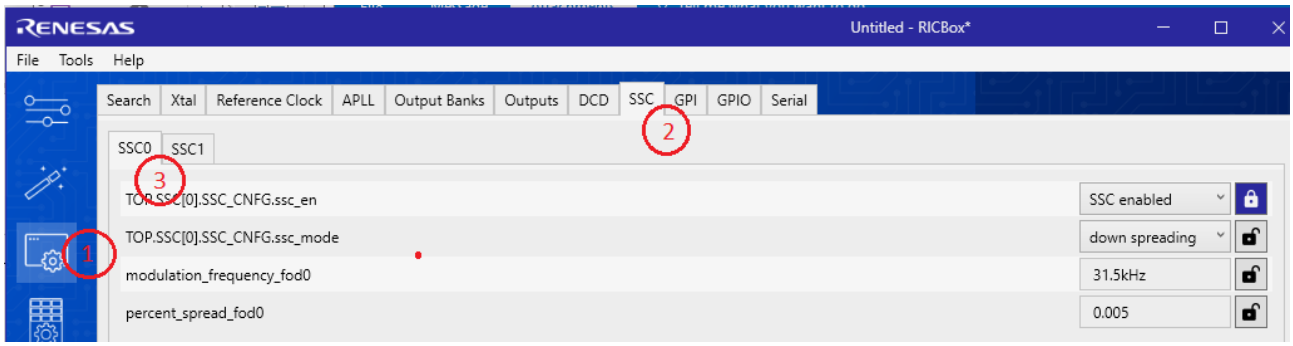


**Figure 8. Steps to Configure Spread Spectrum**

## 2.2 Buffer Mode

In other use cases, a reference clock is generated from a PCIe switch. This reference clock is expected to pass out to a PCIe RC or EP without inserting a PLL in its path. This is where VC7 buffer mode is optimal for use in PCIe Common clocking architecture.

Buffer mode means some output clocks can source from input clocks (CLKIN0 and CLKIN1) directly instead of a PLL's VCO. In the VC7 device configuration GUI, choose "CLKIN0" or "CLKIN1" from the **Frequency Source** pull-down menu.

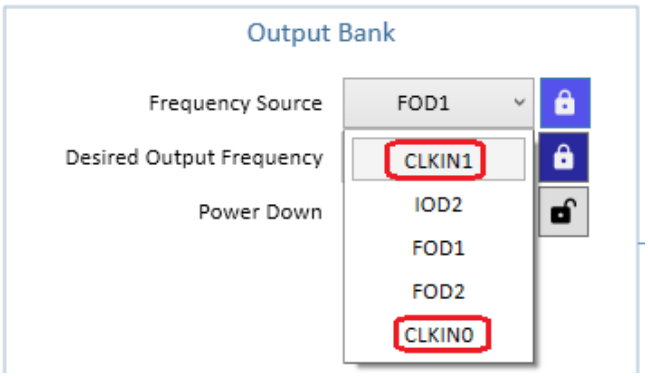


**Figure 9. Selecting CLKIN0 or CLKIN1 in Buffer Mode Configuration**

*Note*: Buffer mode is supported on Bank 4, Bank 5, and Bank 6 outputs. Higher banks (Bank 0 to 3) do not have this clock source option. In addition, when buffer mode is enabled, the APLL must operate normally because outputs are enabled only when the APLL is locked.

# 3. Flexibility of Implementing CC and IR Clocking Architectures using VersaClock 7

VC7 devices support multiple configurations. When these configurations are OTP (one-time programming) programmed into the device, each configuration in the device OTP memory can be selected by using GPIO pin strapping. For example, a four-configuration design can be made and programmed into four slots in the device's OTP memory. Table 2 shows how each of the four configurations can be selected by different GPIO logic levels.

**Table 2. Configuration Select via GPIO Pin Strapping**

| OTP Memory | GPIO1 | GPIO0 | Configuration |
|---|---|---|---|
| Slot 1 | 0 | 0 | Synthesizer Mode, No Spread Spectrum |
| Slot 2 | 0 | 1 | Synthesizer Mode, -0.5% Spread |
| Slot 3 | 1 | 0 | Buffer Mode |
| Slot 4 | 1 | 1 | Buffer Mode |

The good thing for configuration select is that VC7 devices support both static and dynamic select. *Static* select means that GPIO levels must be latched in a power-up reset to determine which configuration is intended, whereas *dynamic* select means a change of configurations can be made on-the-fly without a power-up reset or a power cycling. This feature enables a VC7 device equipped with multiple configurations to be used in multiple platforms with a single design, or in multiple PCIe links with flexibility of switching between CC or IR clocking by a flip of GPIO pins.

# 4. PCIe Compliance Performance of VersaClock 7-generated Clocks

This section describes the PCIe compliance performance of clocks generated by VC7 devices configured in different operation modes. The results show VC7 generated clocks comply with PCIe Gen1-6 requirements in each operation mode. The following list summarizes how each compliance plot is produced:

1. All clock frequency is configured 100MHz, LP-HCSL.
2. The phase noise data are recorded in raw data (CSV format) from 100Hz to 100MHz.
3. The above data are run through the Renesas PCIe Test Tool with PCIe Gen 1-6 filters built in. The final results and summary are printed out by the tool.

## 4.1 Clock Generation: Synthesizer Mode without Spread Spectrum

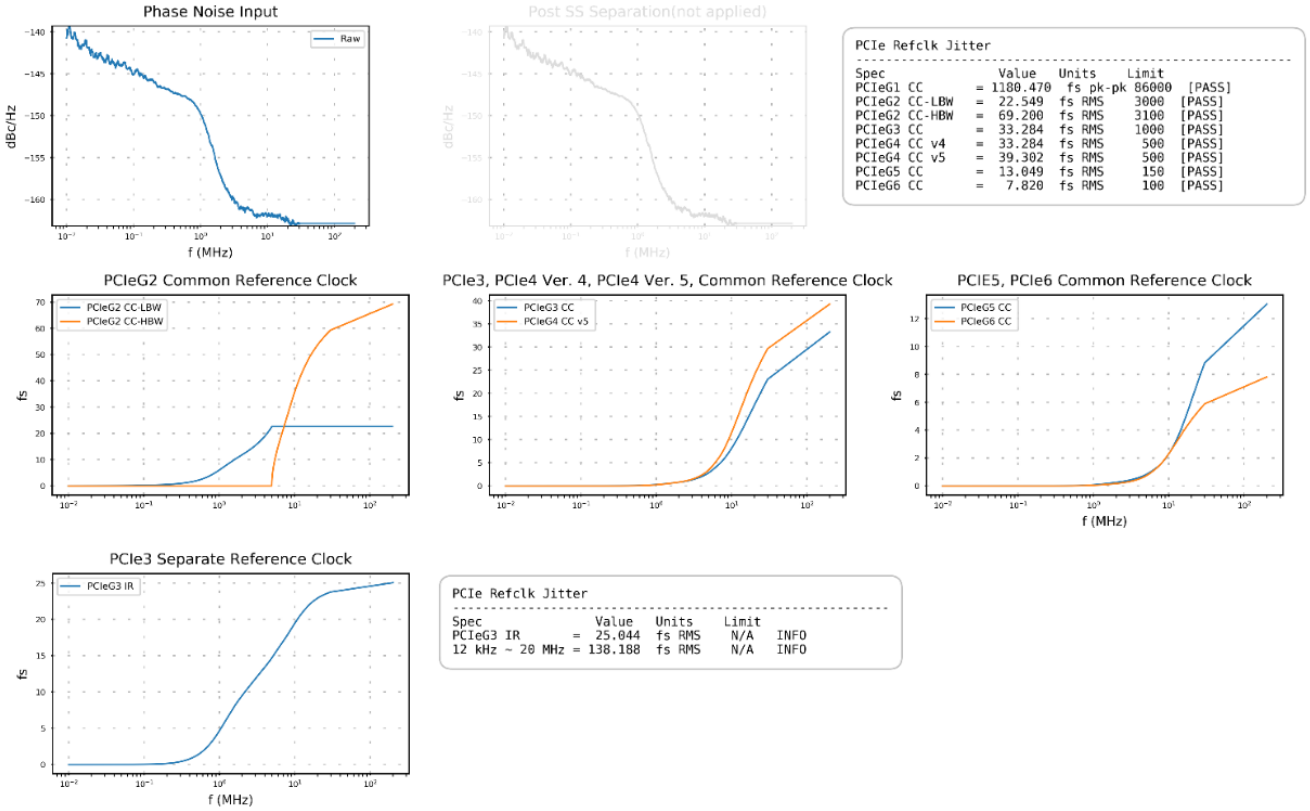


**Figure 10. Clock in Synthesizer Mode: 100MHz, HCSL, No Spread Spectrum, Pass PCIe Gen1-6**

## 4.2 Clock Generation: Synthesizer Mode with Spread Spectrum

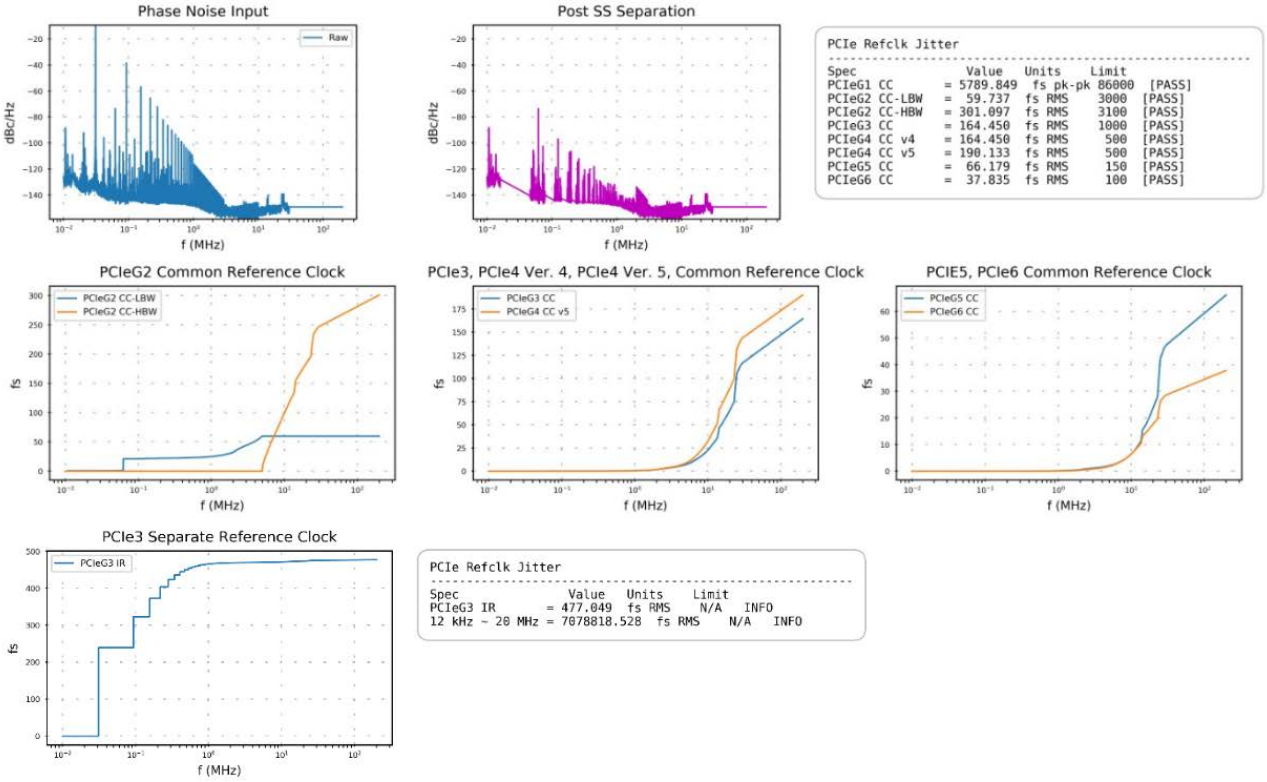


**Figure 11. Clock in Synthesizer Mode: 100MHz, HCSL, -0.5% Down Spread Pass PCIe Gen1-6**

## 4.3 Clock Buffer: Input Clock without Spread Spectrum

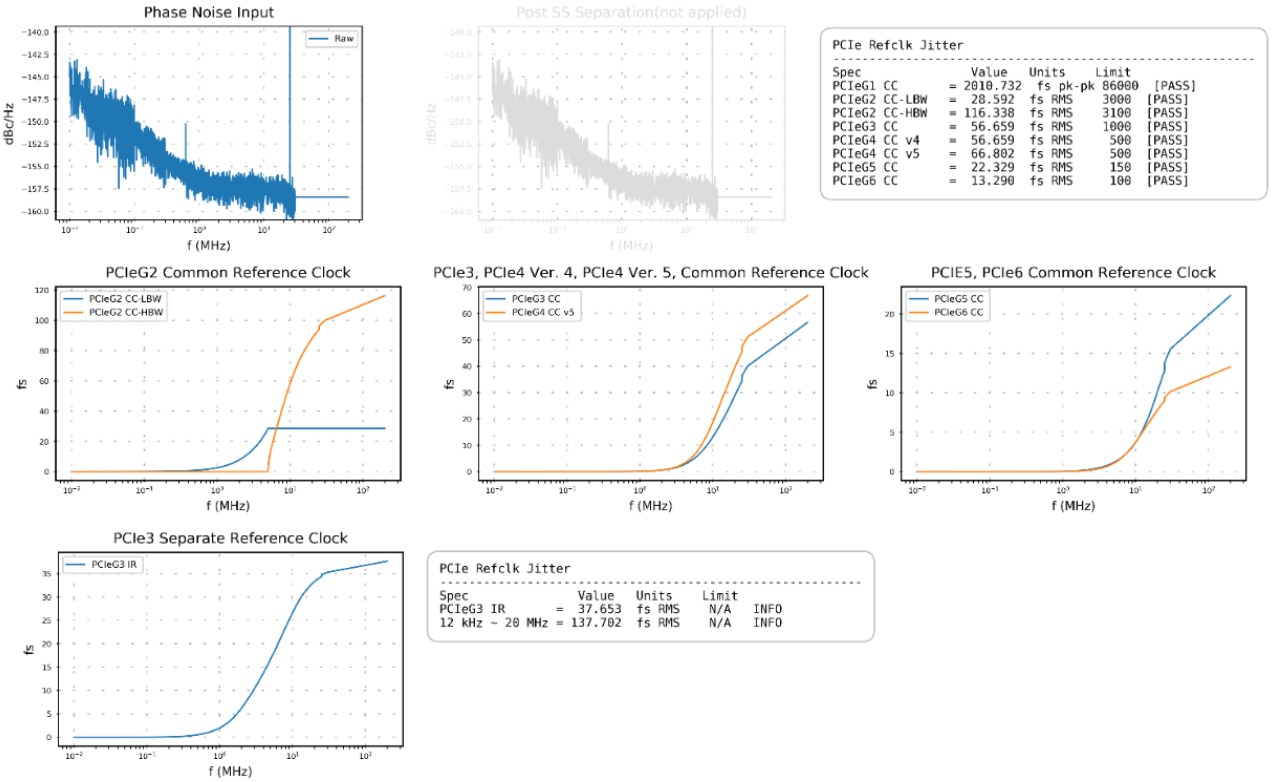


**Figure 12. Clock in Buffer Mode: Input Clock = 100MHz, HCSL, No Spread**

# 5. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Aug 29, 2022 | Initial release. |

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