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Renesas Electronics Corporation

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H8/300H Tiny Series

Outputting a Scale

Introduction

A keyboard is connected to the parallel port, and musical notes corresponding to pressed keys are output from a speaker.

Target Device

H8/36014

Contents

1. Specifications

1. Figure 1.1 shows the hardware configuration for an example of a musical note output circuit connection. As shown in figure 1.1, the keyboard is connected to the I/O port (pins P10 to P12 and P70 to P73).
2. A square wave of the frequency corresponding to the key pressed on the keyboard is output from the speaker connected to the I/O port (pin P76).

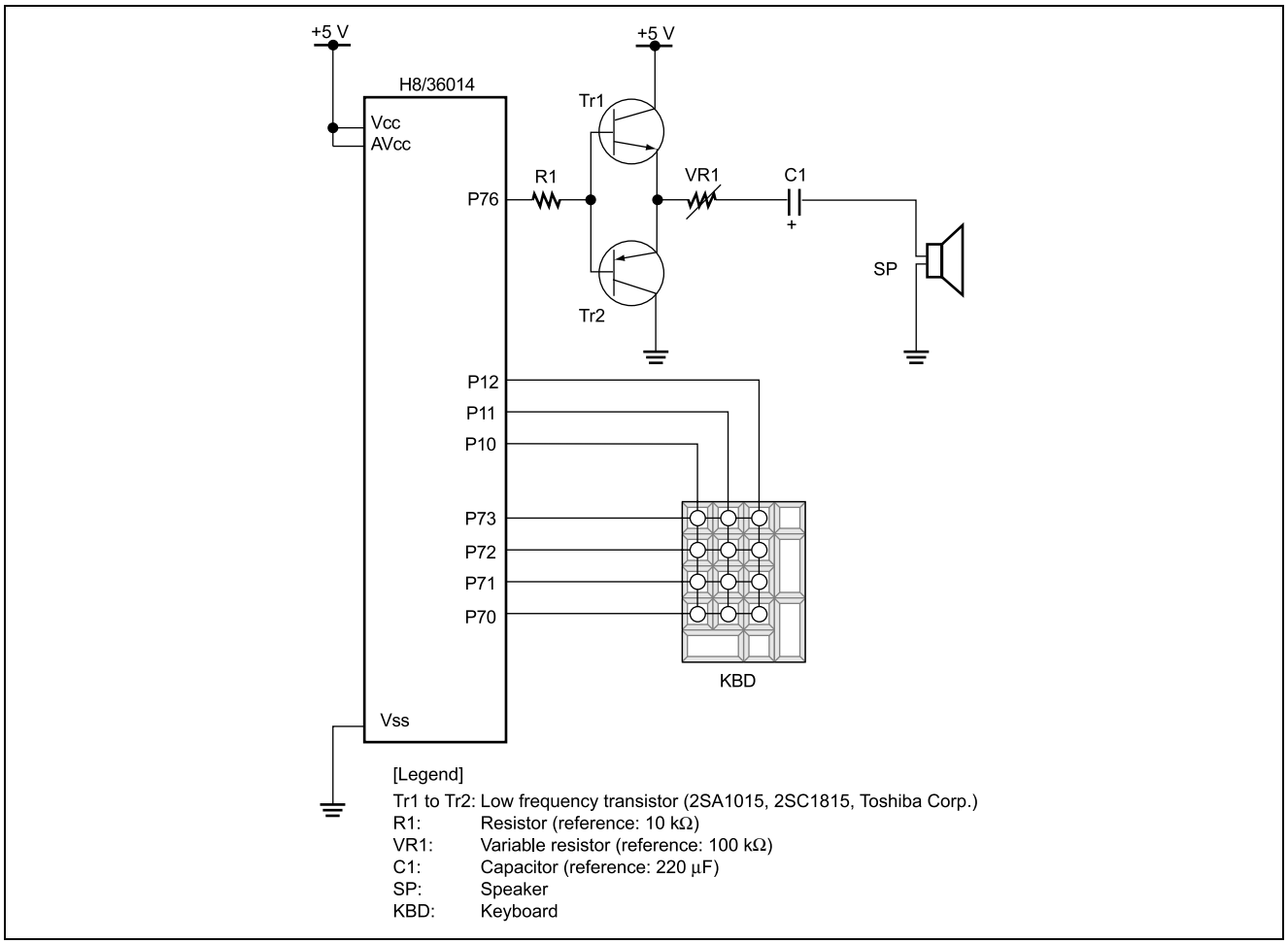


Figure 1.1 Hardware Configuration

3. In this sample task, the H8/36014 operating voltage (Vcc) and analog power supply voltage (AVcc) are 5.0 V, and the OSC clock frequency is 16 MHz.
4. The keyboard used in this sample task is a numerical keypad used for input to a personal computer. Normally a 1-bit serial signal is output, but in this example the keyboard is modified to enable parallel I/O.
5. Operation of this sample task is as follows:
   A. Of the seven ports connected to the keyboard, P70 to P73 are sequentially switched to set to H level.
   B. Then the states of the remaining three ports P10 to P12 are monitored, and a pressed key is identified through the ports at which H level is detected.
   C. The frequency corresponding to the pressed key is output to port P76. The waveform is a rectangular waveform at H level.
   D. For example, if "1" on the numerical keypad is pressed, the combination of ports P70 and P10 causes the frequency 261.63 Hz of the note "do" to be output.
   E. The volume is adjusted using the variable resistor.

2. Description of Functions

Figure 2.1 is a block diagram of the H8/36014 functions used in this sample task. Table 2.1 shows function allocations.

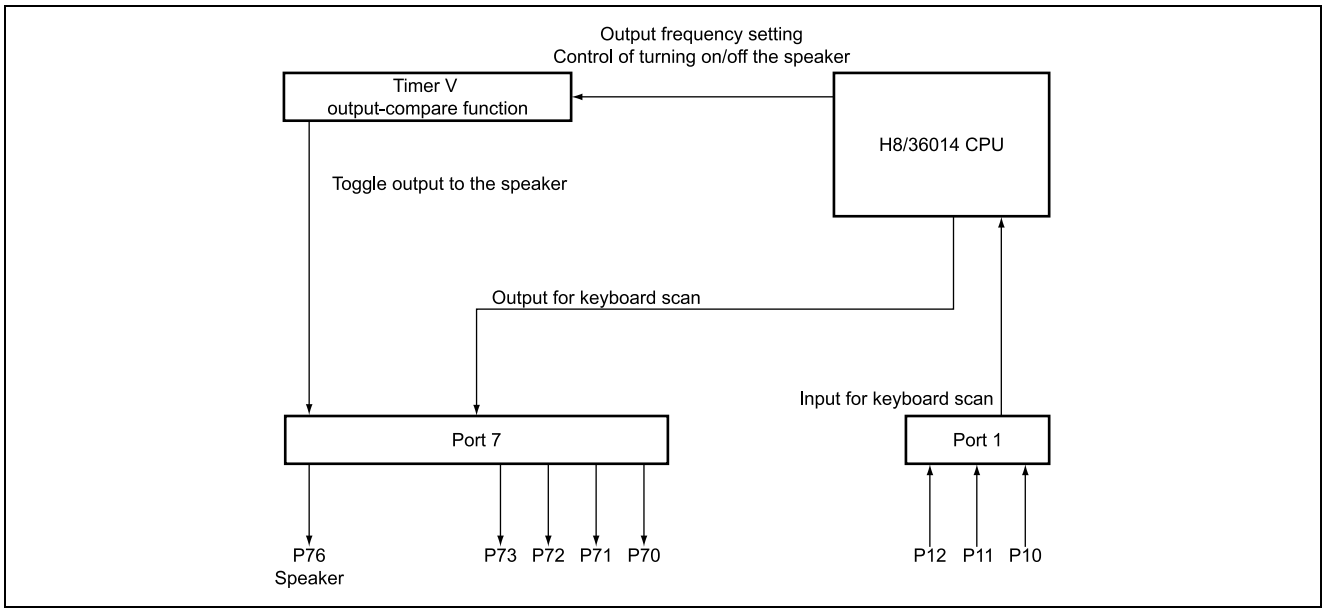


Figure 2.1 Block Diagram of Functions

Table 2.1 Function Allocation

Function Used	Function Allocation
Timer V	A compare-match function is used to toggle output. By setting the value in the time constant register A (TCORA), the output frequency is changed.
Port 1	Keyboard input is detected on input pins P10 to P12 of port 1.
Port 7	Successive switching to the H level is effected through the port 7 output pins P70 to P73. The frequency is output from P76.

3. Principle of Operation

1. The principle of operation for producing a musical note output using the timer V is shown in figure 3.1. As illustrated in this figure, TMOV output is toggled in the cycle of compare-match of timer V to output the sound of A (440 Hz).

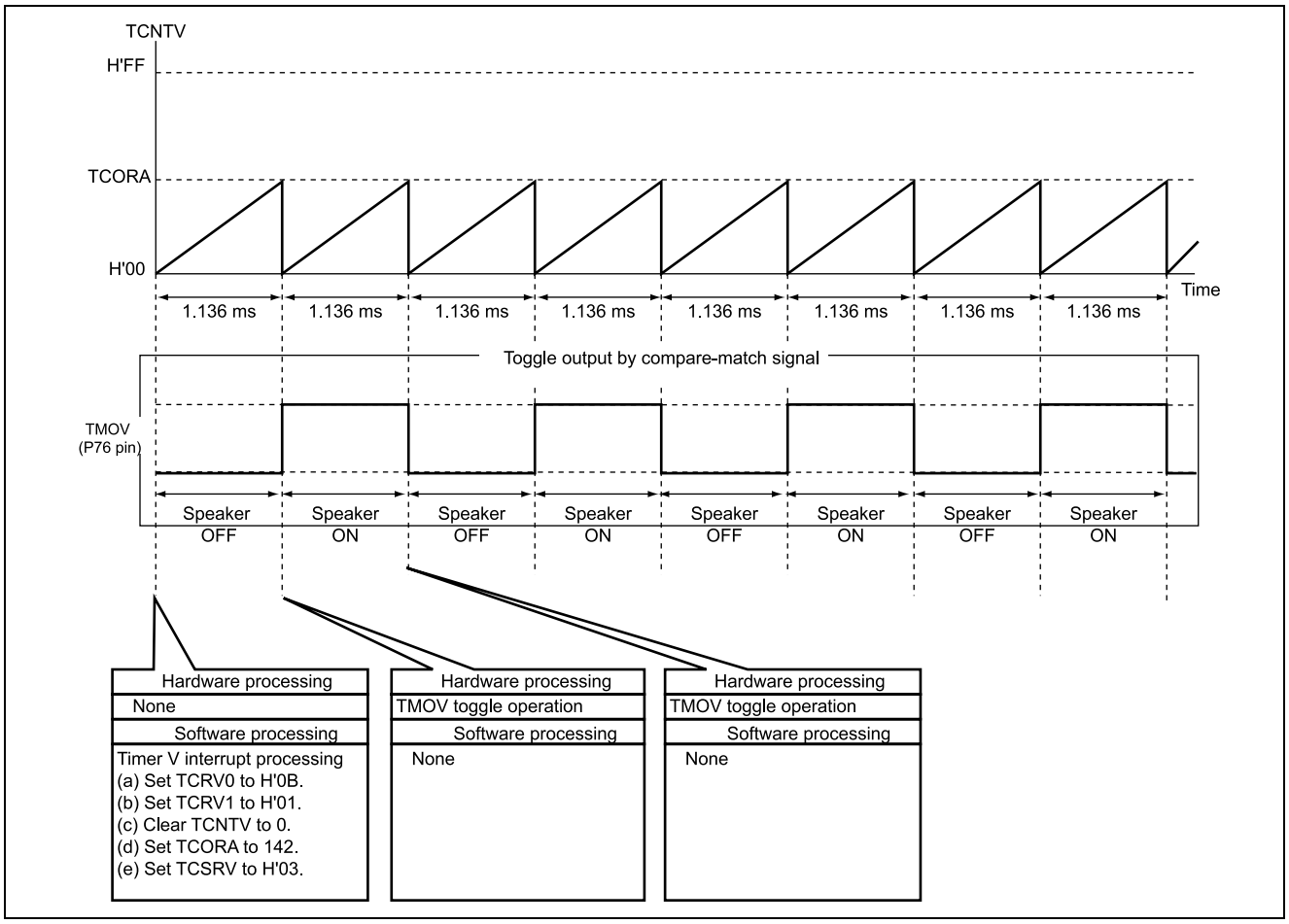


Figure 3.1 Principle of Operation for Musical Note Output Using Timer V

2. Timer V settings

- Internal clock settings
  The system clock is ϕ = 16 MHz, and the internal clock ϕ/128 is selected. ϕ/128 = 12500 Hz.
- Counter values set in TCORA

Table 3.1 Description of Counter Values

Note	Counter value	Output frequency	Calculated frequency
C	239	261.51	261.63
C#	225	277.78	277.18
D	213	293.43	293.66
D#	201	310.95	311.13
E	190	328.95	329.63
F	179	349.16	349.23
F#	169	369.82	369.99
G	159	393.08	392.00
G#	150	416.67	415.30
A	142	440.14	440.00
A#	134	466.42	466.16
B	127	492.13	493.88

[Legend]
Musical notes: C (do) to B (ti)
Counter value: (operating clock/2)/calculated frequency
Output frequency: (operating clock/2)/counter value
Calculated frequency: Calculated frequency of each musical note.

Note: The operating clock is divided by 2 because the ON/OFF action makes one cycle.

- Calculated frequency
  The frequency for each note is calculated using the following formula:
  Calculated frequency = 440 * 2^(X/12)
  Example: Calculate to two decimal places.
  For the note of A: 440 × 2^(0/12) = 440 Hz
  For the note of A#: 440 × 2^(1/12) = 466.16 Hz
  For the note of G#: 440 × 2^(-1/12) = 415.30 Hz

- Counter values
  Calculate the counter values that are to be set in TCORA.
  Counter value = (operating clock/2)/calculated frequency.
  Example: Calculate as integers.
  For the note of A: 125000 / 2 / 440 = 142
  For the note of A#: 125000 / 2 / 466.16 = 134
  For the note of G#: 125000 / 2 / 415.30 = 150

- Output frequency
  Calculate the frequency to be output from the speaker.
  Output frequency = (operating clock/2)/counter value.
  Example: Calculated to two decimal places.
  For the note of A: 125000 / 2 / 142 = 440.14
  For the note of A#: 125000 / 2 / 134 = 466.42
  For the note of G#: 125000 / 2 / 150 = 416.67

3. Keyboard input

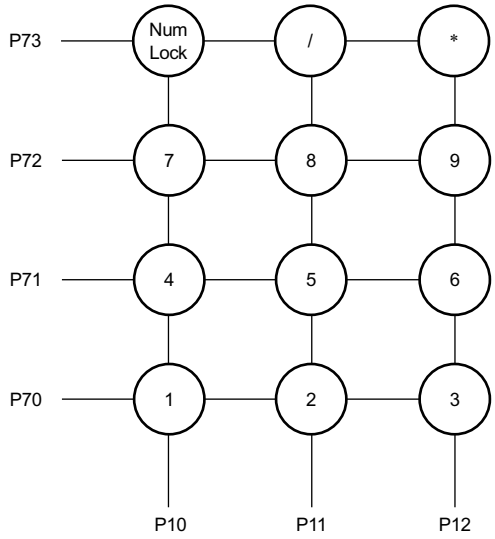


Figure 3.2 Example of Keyboard Connection

Table 3.2 Correspondence Between the Output Musical Note and the Key Pressed

Musical Note	Key
C	1
C#	2
D	3
D#	4
E	5
F	6
F#	7
G	8
G#	9
A	Num Lock
A#	/
B	*

P70 to P73 are sequentially switched to be driven to H level, and the states of P10 to P12 are monitored; the pressed key is identified from the ports at which H level is detected. The correspondence between the output musical note and the key pressed is indicated in table 3.2.

4. Description of Software

4.1 Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Makes initial settings, outputs frequencies.
Keyboard input processing routine	input_key	Scans keyboard and returns the corresponding code. If no key is pressed: –1 If a key is pressed: 0 to 11

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 4.2.

Table 4.2 Description of Internal Registers

Register Name		Function	Address	Setting
TCRV0		Timer control register V0 Selects TCNTV input clock, sets condition for clearing of TCNTV, and controls the individual timer V interrupt requests.	H'FFA0	H'0B
	CMIEB	Compare Match Interrupt Enable B: When CMIEB = 0, interrupt requests on setting of the CMFB bit in TCSRV are disabled.	Bit 7	0
	CMIEA	Compare Match Interrupt Enable A: When CMIEA = 0, interrupt requests on setting of the CMFA bit in TCSRV are disabled.	Bit 6	0
	OVIE	Timer Overflow Interrupt Enable: When OVIE = 0, interrupt requests on setting of the OVF bit in TCSRV are disabled. When OVIE = 1, interrupt requests on setting of the OVF bit in TCSRV are enabled.	Bit 5	0
	CCLR1	Counter Clear 1 and 0: Sets the conditions for clearing of TCNTV. When CCLR1 = 0 and CCLR0 = 1 are both set, TCNTV is cleared on compare-match with A.	Bit 4	0
	CCLR0		Bit 3	1
	CKS2	Clock Select 2 to 0: In combination with the ICKS0 bit of TCRV1, selects the clock signal for input to TCNTV and the condition to be counted. With CKS2 = 0, CKS1 = 1, CKS0 = 1 and ICKS0=1, counting by TCNTV is of the falling edges of the internal clock ϕ/128.	Bit 2	0
	CKS1		Bit 1	1
	CKS0		Bit 0	1

Register Name		Function	Address	Setting
TCSRV		Timer Control/Status Register V: Holds the overflow and compare-match status flags for timer V and controls output in response to a match.	H'FFA1	H'00 (initial setting)
	CMFB	Compare Match Flag B: When the values of TCNTV and TCORB match, CMFB is set to 1.	Bit 7	0
	CMFA	Compare Match Flag A: When the values of TCNTV and TCORA match, CMFA is set to 1.	Bit 6	0
	OVF	Timer Overflow Flag: When the value of TCNTV overflows, OVF is set to 1. This bit is cleared by reading it while it is set and then writing a 0 to it.	Bit 5	0
	OS3	Output Select Bits 3 and 2: Selects the output level on the TMOV pin in response to a match for compare-match B. When OS3 = 0 and OS2 = 0: No change	Bit 3	0
	OS2		Bit 2	0
	OS1	Output Select Bits 1 and 0: Selects the output level on the TMOV pin in response to a match for compare-match A. When OS = 0 and OS0 = 0: No change When OS = 1 and OS0 = 1: Toggle output	Bit 1	0/1
	OS0		Bit 0	0/1
TCORA		Time constant register A: TCORA is an 8-bit readable/writable register. In this sample task, TCNTV is always compared with TCORA and the output is toggled upon a match.	H'FFA2	H'00 (initial setting)
TCNTV		Timer counter V: An 8-bit count-up counter which takes as input the system clock- frequency divided by 128.	H'FFA4	H'00
TCRV1		Timer Control Register V1: Selects the input edge of the TRGV pin, enables TRGV input, and selects the TCNTV input clock.	H'FFA5	H'01
	TVEG1	TRGV Input Edge Selects 1 and 0: Selects the input edge of the TRGV pin. In this case TVEG1 = 0 and TVEG0 = 0, so trigger input from the TRGV pin is disabled.	Bit 4	0
	TVEG0		Bit 3	0
	TRGE	TRGV Input Enable: Enables and disables incrementing of TCNTV count on the edge input selected by TVEG1 and TVEG0. In this case TRGE = 0, so counting by TCNTV is not affected by the input to the TRGV pin.	Bit 2	0
	ICKS0	Internal Clock Select 0: Selects the clock input to TCNTV and condition counted, in combination with the CKS2 to CKS0 bits of TCRV0. In this case CKS2=0, CKS1=1, CKS0=1 and ICKS0=1, so counting by TCNTV is of the falling edges of the internal clock ϕ/128.	Bit 0	1

Register Name	Function	Address	Setting
PCR1	Port control register 1: Provides pin-by-pin control of input/output selection for the pins of port 2 that have been set as general purpose I/O pins. When PCR1 = H'00, pins P10 to P12 function as general-purpose input pins.	H'FFE4	H'00
PDR1	Port data register: General I/O port data register for port 1.	H'FFD4	H'00
PCR7	Port control register 7: Provides pin-by-pin control of input/output selection for the pins of port 7 that have been set as general purpose I/O pins. When PCR7 = H'0F, the pins P70 to P73 function as general-purpose output pins.	H'FFEA	H'0F
PDR7	Port data register 7: General I/O port data register for port 7.	H'FFDA	H'00 (initial setting)

4.4 Description of RAM

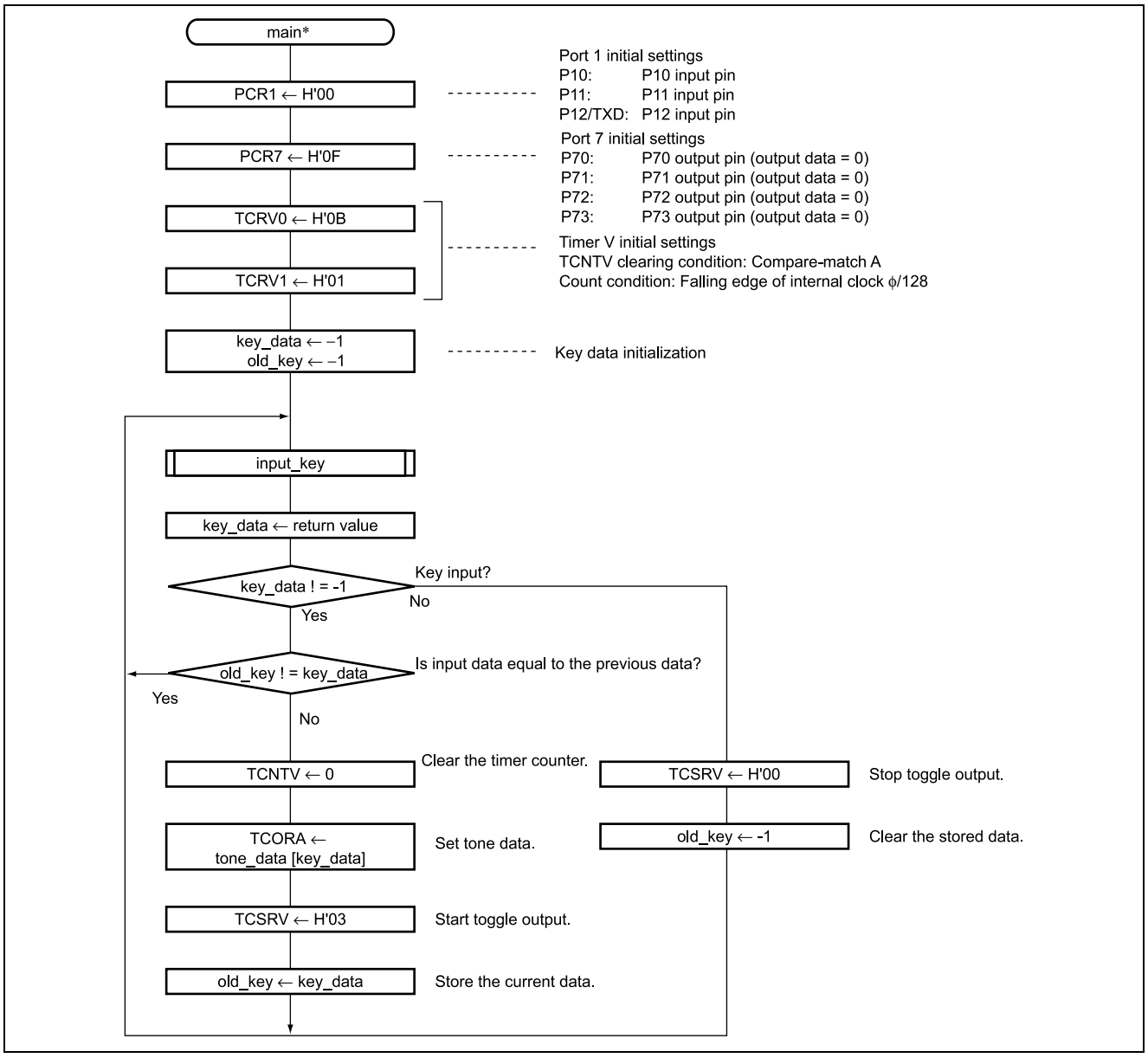
Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

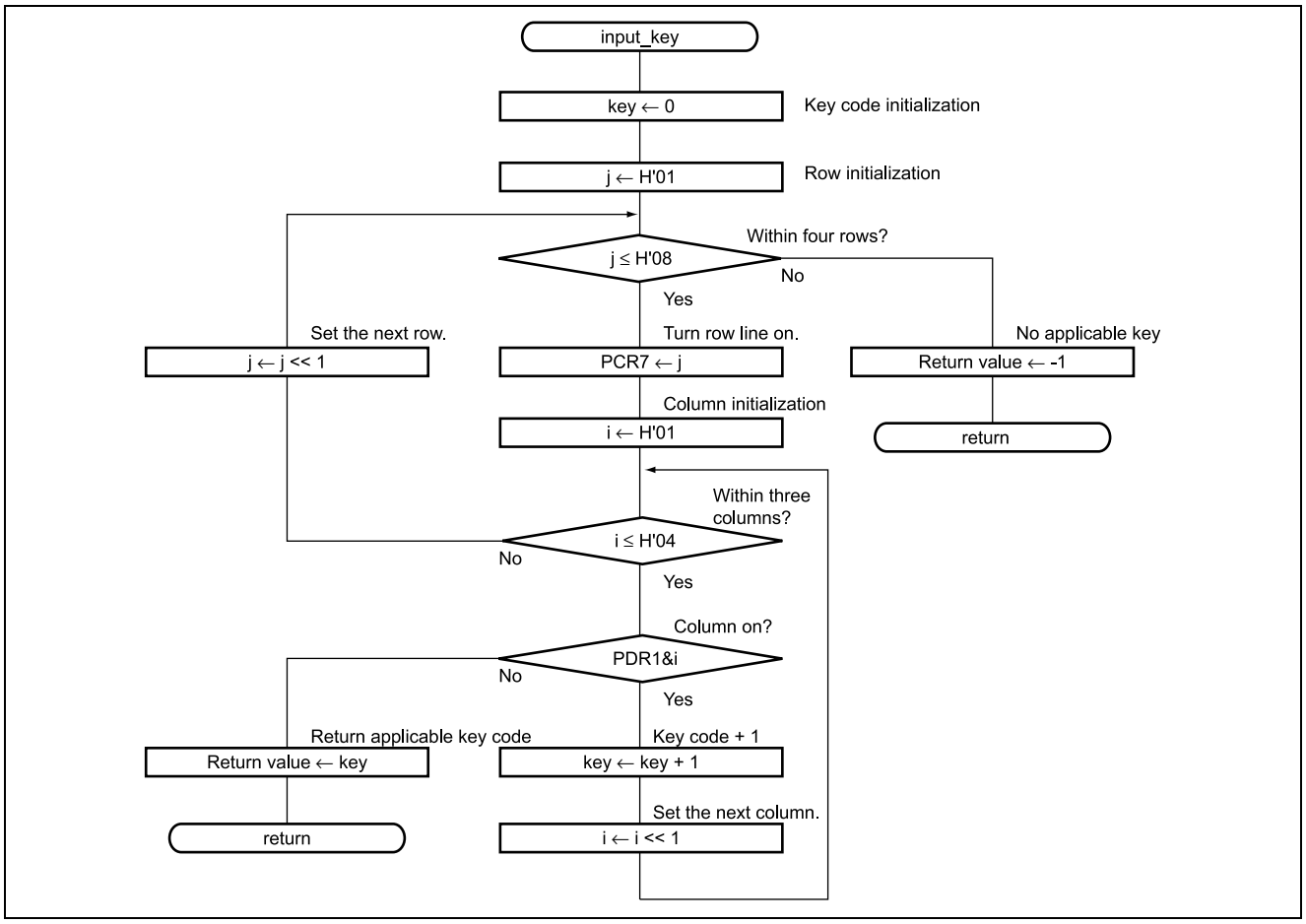
Label Name	Function	Address	Used in
key_data	Stores input key data. (2 bytes)	H'FB80	main
ole_key	Stores previous key data. (2 bytes)	H'FB82	main
i	Stores loop counter for key scans. (2 bytes)	H'FB84	input_key
j	Stores loop counter for key scans. (2 bytes)	H'FB86	input_key
key	Key data for key scans (2 bytes)	H'FB88	input_key

5. Flowchart

1. Main Routine (main)



2. Keyboard Input Processing Routine (input_key)



6. Program Listing

INIT.SRC (program list)

```
     .export   _INIT
     .import   _main
;
     .section  P,CODE
_INIT:
     mov.w     #h'ff80,r7
     ldc.b     #b'10000000,ccr
     jmp  @_main
;
     .end
```

```
/*   H8/300H tiny Series -H8/36014- Application note                                    */
/*   Application                                                                       */
/*   Outputting musical notes                                                          */

#include <machine.h>

/*   Symbol defnition                                                                  */
struct BIT {
     unsigned char b7:1;           /* bit 7 */
     unsigned char b6:1;           /* bit 6 */
     unsigned char b5:1;           /* bit 5 */
     unsigned char b4:1;           /* bit 4 */
     unsigned char b3:1;           /* bit 3 */
     unsigned char b2:1;           /* bit 2 */
     unsigned char b1:1;           /* bit 1 */
     unsigned char b0:1;           /* bit 0 */
};

#define PDR1        *(volatile unsigned char *)0xFFD4                  /* Port data register 1                 */
#define PCR1        *(volatile unsigned char *)0xFFE4                  /* Port control register 1              */

#define PDR7        *(volatile unsigned char *)0xFFDA                  /* Port data register 7                 */
#define PCR7        *(volatile unsigned char *)0xFFEA                  /* Port control register 7              */

#define TCRV0       *(volatile unsigned char *)0xFFA0                  /* Timer control register V0            */
#define TCSRV       *(volatile unsigned char *)0xFFA1                  /* Timer control/status register V      */
#define TCORA       *(volatile unsigned char *)0xFFA2                  /* Time constant register A             */
#define TCNTV       *(volatile unsigned char *)0xFFA4                  /* Timer counter V                      */
#define TCRV1       *(volatile unsigned char *)0xFFA5                  /* Timer control register V1            */

/*   Function define                                                                   */
extern void INIT(void);                                                /* Stack pointer set                    */
void main(void);                                                       /* main routine                         */
int input_key(void);                                                   /* Input key                            */
```

```
const unsigned char tone_data[12] =
{
     239,                                                    /* C (261.63Hz)                  */
     225,                                                    /* C#(277.18Hz)                  */
     213,                                                    /* D (293.66Hz)                  */
     201,                                                    /* D#(311.13Hz)                  */
     190,                                                    /* E (329.63Hz)                  */
     179,                                                    /* F (349.23Hz)                  */
     169,                                                    /* F#(369.99Hz)                  */
     159,                                                    /* G (392.00Hz)                  */
     150,                                                    /* G#(415.30Hz)                  */
     142,                                                    /* A (440.00Hz)                  */
     134,                                                    /* A#(466.16Hz)                  */
     127                                                     /* B (493.88Hz)                  */
};

/*   RAM define                                                                                */
int key_data, old_key;                                       /* Input key code New & Old      */
int i,j;                                                     /* Loop counter                  */
int key;                                                     /* Input key code                */

/*   Vector address                                                                            */
#pragma section V1                                           /* Vector section set            */
void (*const VEC_TBL1[])(void) = {
     INIT                                                    /* H'0000 Reset vector           */
};
#pragma section                                              /* P                             */

/*****************************************************************************************************************************************/
/*   Main program                                                                              */
/*****************************************************************************************************************************************/
void main(void)
{
     PCR1 = 0x00;                                            /* Port1 0-2bit input            */

     PCR7  = 0x0f;                                           /* Port7 0-3bit output           */

     TCRV0 = 0x0b;                                           /* Set clock(φ/128)              */
     TCRV1 = 0x01;                                           /* Set clock(φ/128)              */

     key_data = old_key = -1;                                /* Initialize key data           */
     while(1){
     key_data = input_key();                                 /* Input key                     */
     if ( key_data != -1) {
          if ( old_key != key_data ) {
               TCNTV = 0;                                    /* Clear Timer Counter           */
               TCORA = tone_data[key_data];                  /* Set tone data                 */
               TCSRV = 0x03;                                 /* Start toggle output           */
               old_key = key_data;                           /* Save current key data         */
          }
     } else {
          TCSRV = 0x00;                                      /* Stop toggle output            */
          old_key = -1;                                      /* Clear old input data          */
          }
     }
}
```

```
/*****************************************************************************************************************************************************/
/*   input key data                                                                                                                                  */
/*****************************************************************************************************************************************************/
int input_key(void)
{
     key = 0;                                                                    /* Set start key code                    */
     for ( j=0x01; j<=0x08; j<<=1 ) {
          PDR7 = j;                                                              /* Output level to line                  */
          for ( i=0x01; i<=0x04; i<<=1 ) {
               if ( PDR1 & i ) {                                                 /* Read level from line                  */
                    return key;
               }
               key++;
          }
     }
     return -1;
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.29.03	—	First edition issued

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