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H8SX Family

Output of Multiple $\overline{CS}$ Signals through the Same Pin

Introduction

The H8SX/1663 is capable of the output of multiple $\overline{CS}$ signals via a single pin. This application note covers an example where $\overline{CS1}$ and $\overline{CS2}$ output signals are both output via a single pin.

Target Device

H8SX/1663

Contents

1. Specification

This LSI circuit is capable of the output of multiple $\overline{CS}$ signals via a single pin. In this example, the $\overline{CS1}$ output and $\overline{CS2}$ output are both on the same pin (pin PB1) so that access to any location in the range formed by areas 1 and 2 (H'200000 – H'BFFFFF) is selected by the $\overline{CS}$ signal on PB1.

- An example of connection of this sample task is shown in figure 1.
- The PFCR is set so that both the $\overline{CS1}$ and $\overline{CS2}$ signals are output from pin PB1.
- In this example, one byte of data is written to H'200000 in area 1 and then H'400000 in area 2, and output of the common $\overline{CS}$ signal from the PB1 pin is confirmed.

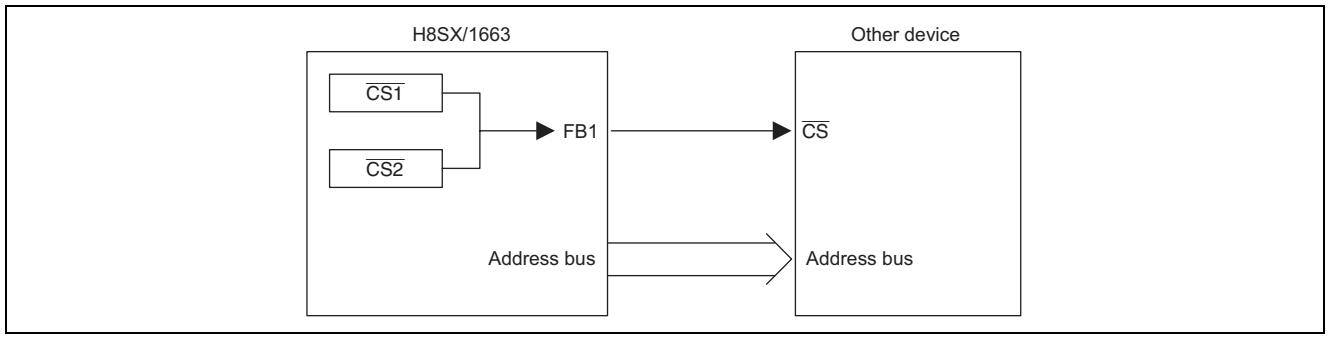


Figure 1 Example of Connection for Output of Multiple $\overline{CS}$ Signals through the Same Pin

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating frequency	Input clock	: 16 MHz
	System clock (Iϕ)	: 32MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	: 32 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 32 MHz (input clock frequency × 2)
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0)	

3. Description of Modules Used

3.1 Bus Controller

Figure 2 is a block diagram of the bus-control block.

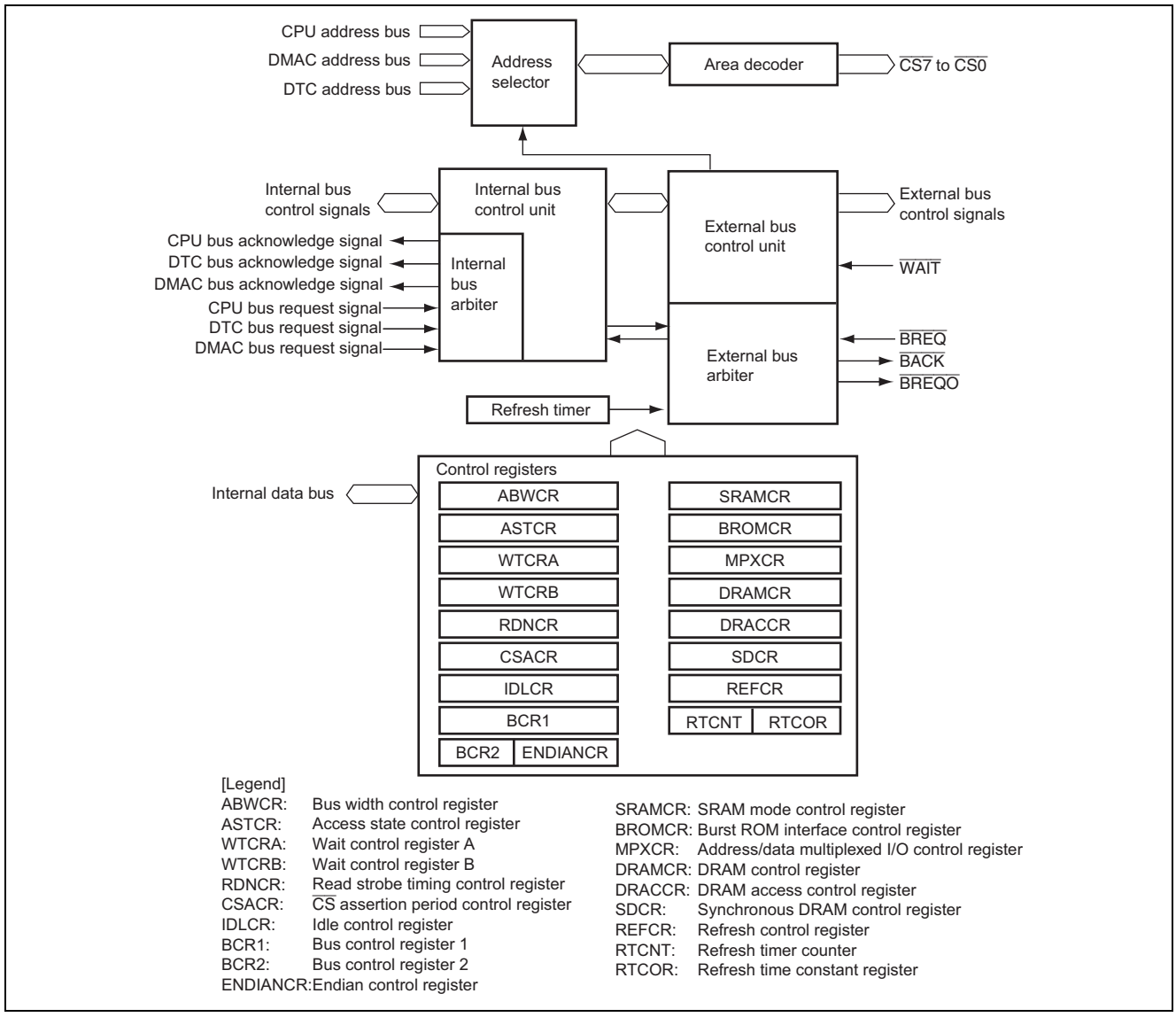


Figure 2 Block Diagram of the Bus Controller

Explanations of the functional elements shown in figure 2 are given below.

- Bus width control register (ABWCR)
  ABWCR is used to set data-bus width for all areas of external address space.
- Access state-control register (ASTCR)
  ASTCR is used to set all areas of external address space as spaces for access in two states (cycles of the bus clock) or as spaces for access in three states. Settings to enable or disable the wait states can be made at the same time.
- Wait control register B (WTCRB)
  WTCRB is used to select numbers of programmed cycles of waiting for access to all areas of external address space.
- Port function control registers 0, 2, 4, 6 (PFCR0, 2, 4, 6)
  PFCRs control the I/O ports. With the settings in this example, the $\overline{CS1}$ and $\overline{CS2}$ signals are output on pin PB1, output on the RD/$\overline{WR}$ pin and on pins A16 to A20 is enabled, and the $\overline{LHWR}$ output pin is set.
- Port D data direction register (PDDDR)
- Port E data direction register (PEDDR)
  DDRs are 8-bit write-only registers and used to specify bit-wise settings of input or output for the pins of the corresponding ports. In this example, pins A0 to A15 are set as output pins.

3.2 Chip Select

This LSI can output chip select signals ($\overline{CS0}$ to $\overline{CS7}$) for areas 0 to 7. The low level is output when the corresponding area of external address space is accessed.

Enabling or disabling of $\overline{CSn}$ signal output is set by the port function control registers (PFCR).

In on-chip ROM disabled extended mode, pin $\overline{CS0}$ is placed in the output state after a reset. Pins $\overline{CS1}$ to $\overline{CS7}$ are placed in the input state after a reset and so the corresponding PFCR bits should be set to 1 if signals $\overline{CS1}$ to $\overline{CS7}$ are to be output.

In on-chip ROM enabled extended mode, pins $\overline{CS0}$ to $\overline{CS7}$ are all placed in the input state after a reset and so the corresponding PFCR bits should be set to 1 if signals $\overline{CS0}$ to $\overline{CS7}$ are to be output.

The PFCRs can specify multiple $\overline{CS}$ outputs for most of the pins. If multiple $\overline{CSn}$ outputs are specified for a single pin by the PFCR, the $\overline{CS}$ to be output is generated by combining all of the specified $\overline{CS}$ signals. In this case, areas for which the $\overline{CSn}$ signals will be output through the same pin should have the same external bus interface settings.

Table 2 shows the system of $\overline{CS}$ output and $\overline{CS}$ signals

Table 2 The System of $\overline{CS}$ Output Pins and $\overline{CS}$ Signals

$\overline{CS}$ Output Pin	$\overline{CS}$ Signal	PFCR1	PFCR2
PB7	—	—	—
PB6	$\overline{CS6}$-D	CS6SA, CS6SB = B'11	—
PB5	$\overline{CS5}$-D	CS5SA, CS5SB = B'11	—
PB4	$\overline{CS4}$-B	CS4SA, CS4SB = B'01	—
PB3	$\overline{CS3}$-A	—	—
	$\overline{CS7}$-A	CS7SA, CS7SB = B'00	—
PB2	$\overline{CS2}$-A	—	CS2S = 0
	$\overline{CS6}$-A	CS6SA, CS6SB = B'00	—
PB1	$\overline{CS1}$	—	—
	$\overline{CS2}$-B	—	CS2S = 1
	$\overline{CS5}$-A	CS5SA, CS5SB = B'00	—
	$\overline{CS6}$-B	CS6SA, CS6SB = B'01	—
	$\overline{CS7}$-B	CS7SA, CS7SB = B'01	—
PB0	$\overline{CS0}$	—	—
	$\overline{CS4}$-A	CS4SA, CS4SB = B'00	—
	$\overline{CS5}$-B	CS5SA, CS5SB = B'01	—

3.3 Division into Areas

The external address space is divided into eight areas and the bus controller executes bus control for the external address space in area units. Chip-select signals ($\overline{CS0}$ to $\overline{CS7}$) can be output for each of the areas.

Figure 3 shows how the 16-Mbyte address space is divided into areas. In this sample task, settings are made so that access to either area 1 or area 2 produces $\overline{CS}$ signal output on the same pin (pin PB1).

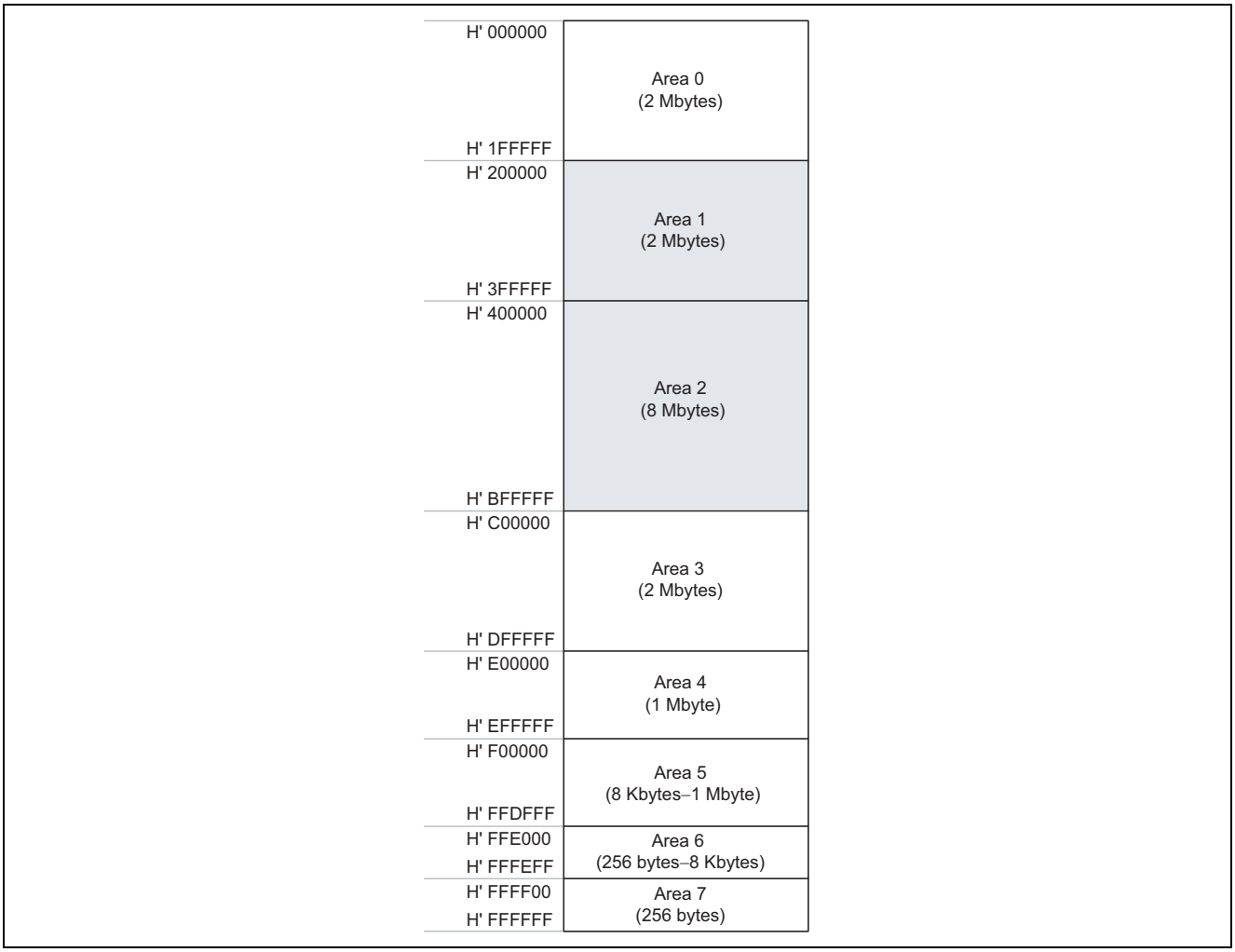


Figure 3 Division into Areas

4. Principles of Operation

Timing when the $\overline{CS}$ signals for areas 1 and 2 are output through a single pin is shown in figure 4.

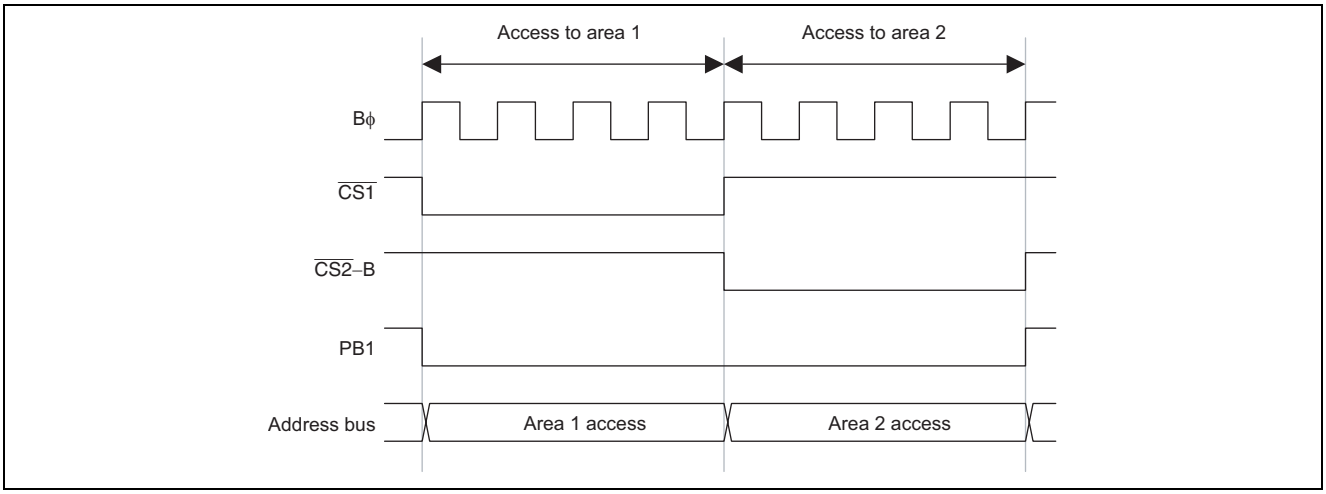


Figure 4 Timing when Multiple $\overline{CS}$ Signals are Output through a Single Pin

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler, ver. 6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'200000	BCS1	Area1
H'400000	BCS2	Area2

Table 5 Vector Table for Exception Processing

Exception Processing Source	Vector No.	Vector address	Function to interrupt destination
Reset	0	H'000000	init

5.2 List of Functions

Table 6 Functions in File main.c

Function Name	Function
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from the module stop mode, and calls the main function.
main	Main routine Calls the BscInit function; writes one byte to the first addresses of areas 1 and 2.
BscInit	Initialization of areas 1 and 2; settings for output of the $\overline{CS1}$ and $\overline{CS2}$ signals on pin PB1.

5.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	area1	First address of area 1	main
unsigned char	area2	First address of area 2	main

5.4 Description of Functions

5.4.1 init Function

1. Functional overview
   The initialization routine releases the required modules from module-stop mode, configures the clocks, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. The latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by mode pins (MD2 to MD0; see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latching is released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the setting on pins MD0 to MD3.

Table 8 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is provided to the CPU, DMAC, and DTC. 001: Input clock × 2
8	ICK0	1	R/W	
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock. 001: Input clock × 2
4	PCK0	1	R/W	
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, B and C control module stop mode. Setting a bit to 1 makes the corresponding module enter the module-stop state, while clearing the bit to 0 releases the module from module stop state.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode. 1: Enables all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

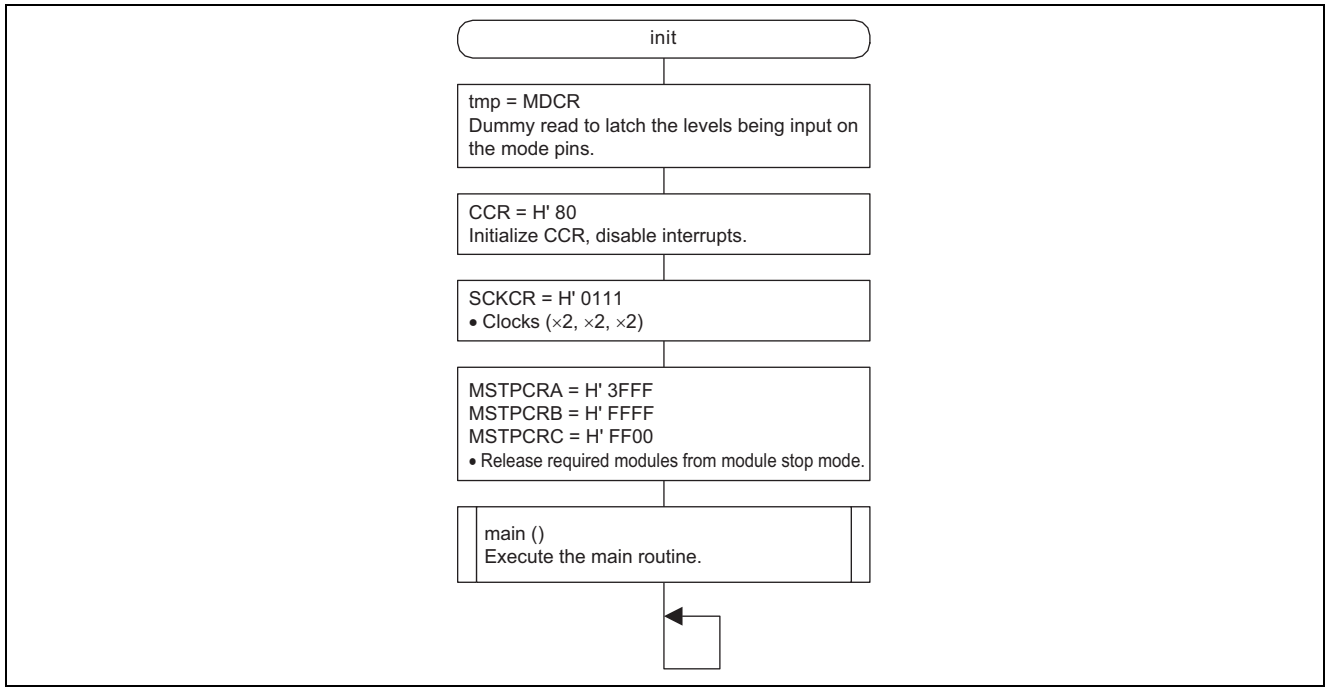
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus Interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus Interface 0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

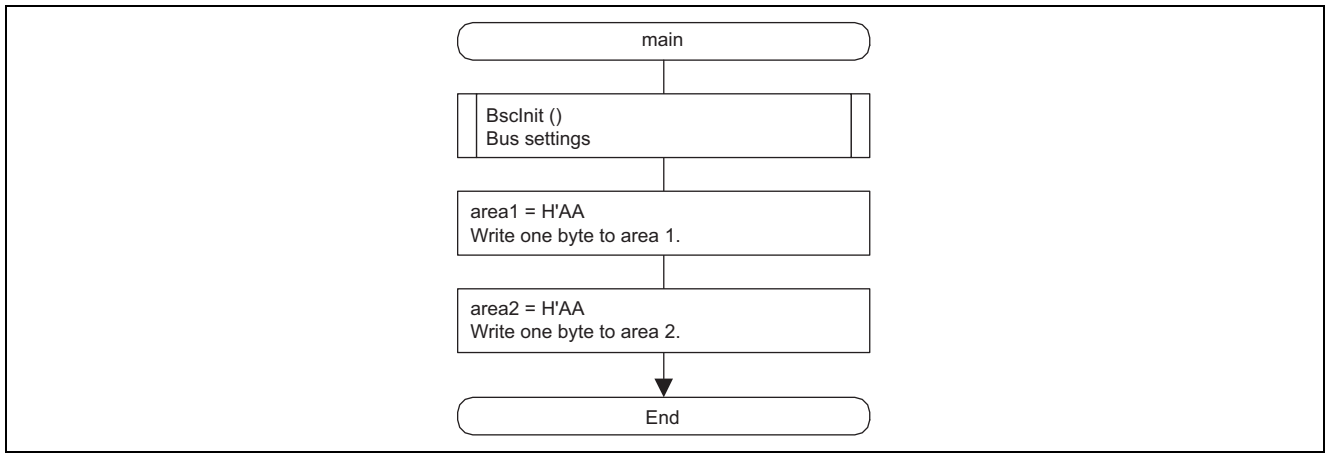
Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5 and IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6 and TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the levels being input on the mode pins.
CCR = H' 80
Initialize CCR, disable interrupts.
SCKCR = H' 0111
• Clocks (×2, ×2, ×2)
MSTPCRA = H' 3FFF
MSTPCRB = H' FFFF
MSTPCRC = H' FF00
• Release required modules from module stop mode.
main ()
Execute the main routine.

5.4.2 main Function

1. Functional overview
   Calls function BscInit and writes one byte to the first addresses of areas 1 and 2.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   None
5. Flowchart



5.4.3 Function BscInit

1. Functional outline
   Initializes areas 1 and 2; sets up output of $\overline{CS1}$ and $\overline{CS2}$ signals on pin PB1.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port D data direction register (PDDDR) Number of bits: 8 Address: H'FFFB8C
  Function: PDDDR sets pins PD7 to 0 as output pins for address output.
  Value: H'FF

- Port E data direction register (PEDDR) Number of bits: 8 Address: H'FFFB8D
  Function: PEDDR sets pins PE7 to 0 as output pins for address output.
  Value: H'FF

- Bus width control register (ABWCR) Number of bits: 16 Address: H'FFFD84
  Function: ABWCR sets areas 7 to 0 as spaces for 16-bit access.
  Value: H'00FF

- Access state-control register (ASTCR) Number of bits: 16 Address: H'FFFD86
  Function: ASTCR sets areas 7 to 0 as spaces for access in three states (cycles of the bus clock).
  Value: H'FF00

- Wait control register B (WTCRB) Number of bits: 16 Address: H'FFFD8A
  Function: WTCRB sets the number for programmed waiting. Seven states (cycles of the bus clock) are inserted for access to area 3.
  Value: H'0770

- Read strobe timing control register (RDNCR) Number of bits: 16 Address: H'FFFD8C
  Function: For read access to areas 7 to 0, RDNCR sets the timing for the negation of $\overline{RD}$ at the end of read cycles.
  Value: H'0000

- Port function control register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Setting	Description
7	CS7E	0	CS7–CS0 Enable
6	CS6E	0	These bits select enabling or disabling of the corresponding $\overline{CSn}$
5	CS5E	0	output pins.
4	CS4E	0	0: Setting for an I/O port pin
3	CS3E	0	1: Setting for a $\overline{CSn}$ output pin (n=7 – 0)
2	CS2E	1	
1	CS1E	1	
0	CS0E	0	

- Port function control register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Setting	Description
6	CS2S	1	$\overline{CS2}$ Output Pin Select Specifies the output pin for $\overline{CS2}$ when $\overline{CS2}$ output is enabled. 0: Specifies pin PB2 as the $\overline{CS2}$-A output pin. 1: Specifies pin PB1 as the $\overline{CS2}$-B output pin.
2	RDWRE	1	RD/$\overline{WR}$ Output Enable 0: Output of RD/$\overline{WR}$ is disabled. 1: Output of RD/$\overline{WR}$ is enabled.

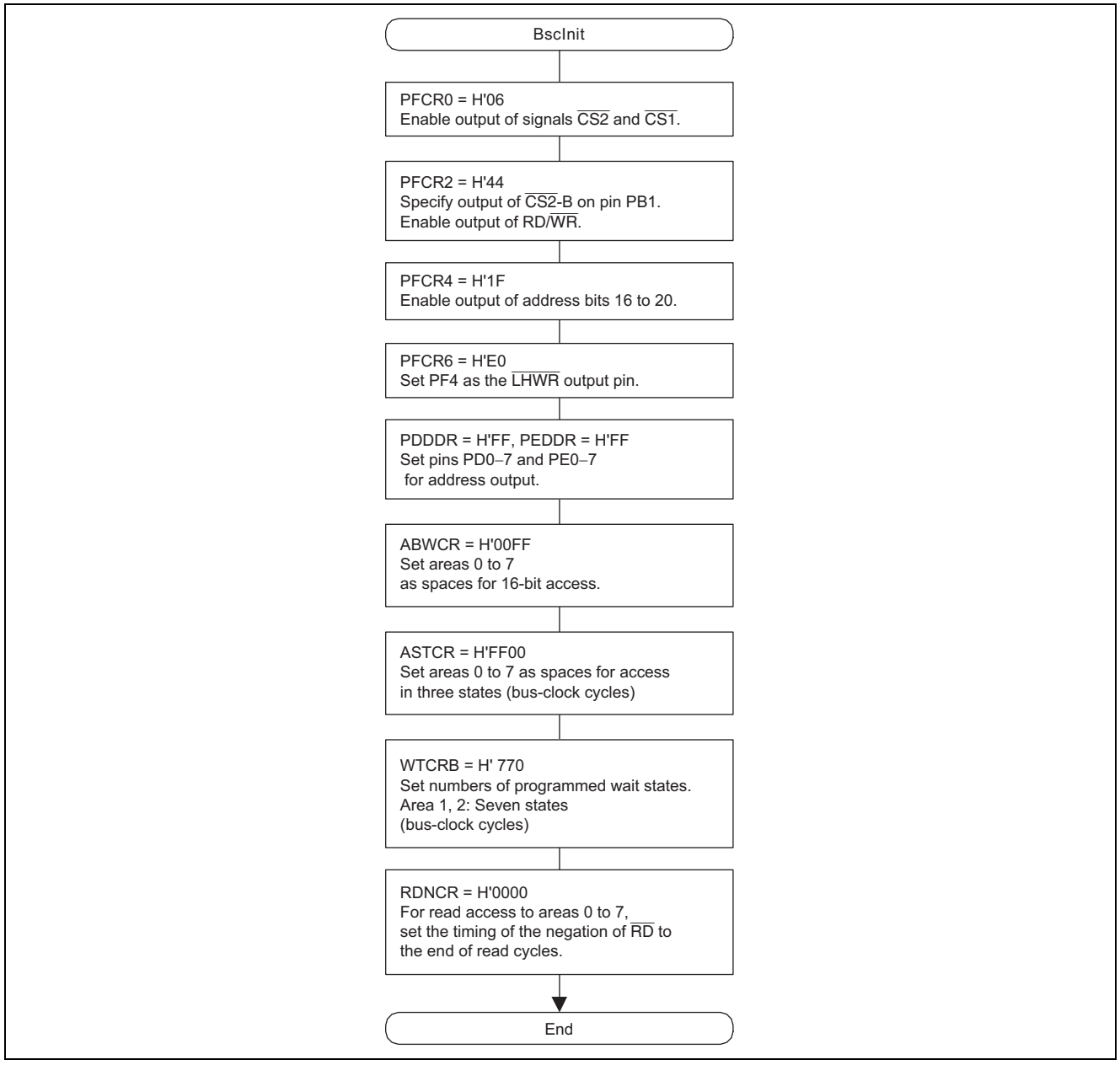
- Port function control register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Setting	Description
4	A20E	1	Address A20 Enable 0: Disables the A20 output. 1: Enables the A20 output.
3	A19E	1	Address A19 Enable 0: Disables the A19 output. 1: Enables the A19 output.
2	A18E	1	Address A18 Enable 0: Disables the A18 output. 1: Enables the A18 output.
1	A17E	1	Address A17 Enable 0: Disables the A17 output. 1: Enables the A17 output.
0	A16E	1	Address A16 Enable 0: Disables the A16 output. 1: Enables the A16 output.

- Port function control register 6 (PFCR6) Number of bits: 8 Address: H'FFFBC6

Bit	Bit Name	Setting	Description
6	LHWROE	1	$\overline{LHWR}$ Output Enable 0: Sets PA4 as an I/O port pin 1: Sets PF4 as the $\overline{LHWR}$ output pin

5. Flowchart


BscInit
PFCR0 = H'06
Enable output of signals CS2 and CS1.
PFCR2 = H'44
Specify output of CS2-B on pin PB1.
Enable output of RD/WR.
PFCR4 = H'1F
Enable output of address bits 16 to 20.
PFCR6 = H'E0
Set PF4 as the LHWR output pin.
PDDDR = H'FF, PEDDR = H'FF
Set pins PD0–7 and PE0–7
for address output.
ABWCR = H'00FF
Set areas 0 to 7
as spaces for 16-bit access.
ASTCR = H'FF00
Set areas 0 to 7 as spaces for access
in three states (bus-clock cycles)
WTCRB = H' 770
Set numbers of programmed wait states.
Area 1, 2: Seven states
(bus-clock cycles)
RDNCR = H'0000
For read access to areas 0 to 7,
set the timing of the negation of RD to
the end of read cycles.
End

6. Documents for Reference (Note)

- Hardware Manual
  H8SX/1663 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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