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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of Timer A (pulse width modulation mode, 8-bit PWM mode)

1.0 Abstract

In pulse width modulation mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up	
Count source	O	Internal count source (f_1 / f_8 / f_{32} / fc_{32})
PWM mode		16-bit PWM
	O	8-bit PWM
Count start condition	O	External trigger input (falling edge of input signal to the TAi_{IN} pin)
		External trigger input (rising edge of input signal to the TAi_{IN} pin)
		Timer overflow (TB2/TAj/TAk overflow)

Note: j = i – 1, but j = 4 when i = 0; k = i + 1, but k = 0 when i = 4.

2.0 Introduction

Operation (1) If the TAi_{IN} pin input level changes from “H” to “L” with the count start flag set to “1”, the counter performs a down count on the count source. Also, the TAi_{OUT} pin outputs an “H” level.

(2) The TAi_{OUT} pin output level changes from “H” to “L” when a set time period elapses. At this time, the timer Ai interrupt request bit goes to “1”.

(3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.

(4) Setting the count start flag to “0” causes the counter to hold its value and to stop. Also, the TAi_{OUT} pin outputs an “L” level.

Note

- The period of PWM pulses becomes (m + 1) X (2^8 – 1) / fi, and the “H” level pulse width becomes n X (m + 1) / fi. If “00_{16}” is set in the eight higher-order bits of the timer Ai register, the pulse width modulator does not work, and the TAi_{OUT} pin outputs “L” level, therefore the timer Ai interrupt request is not generated. (fi : frequency of the count source f_1, f_8, f_{32}, f_{C32}; m : values set to timer Ai register's low-order address n : values set to timer Ai register's high-order address)
- When a trigger is generated, the TAiout pin outputs “L” level of same amplitude as “H” level of the set PWM pulse, after which it starts PWM pulse output.

Figure 1 shows the operation timing

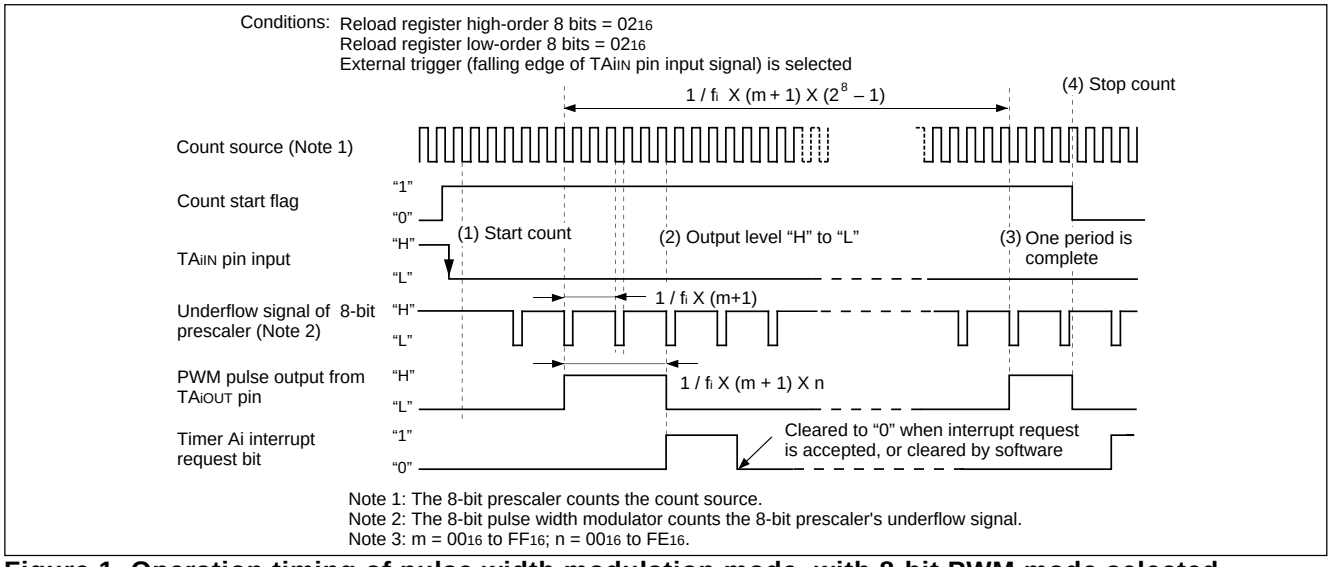
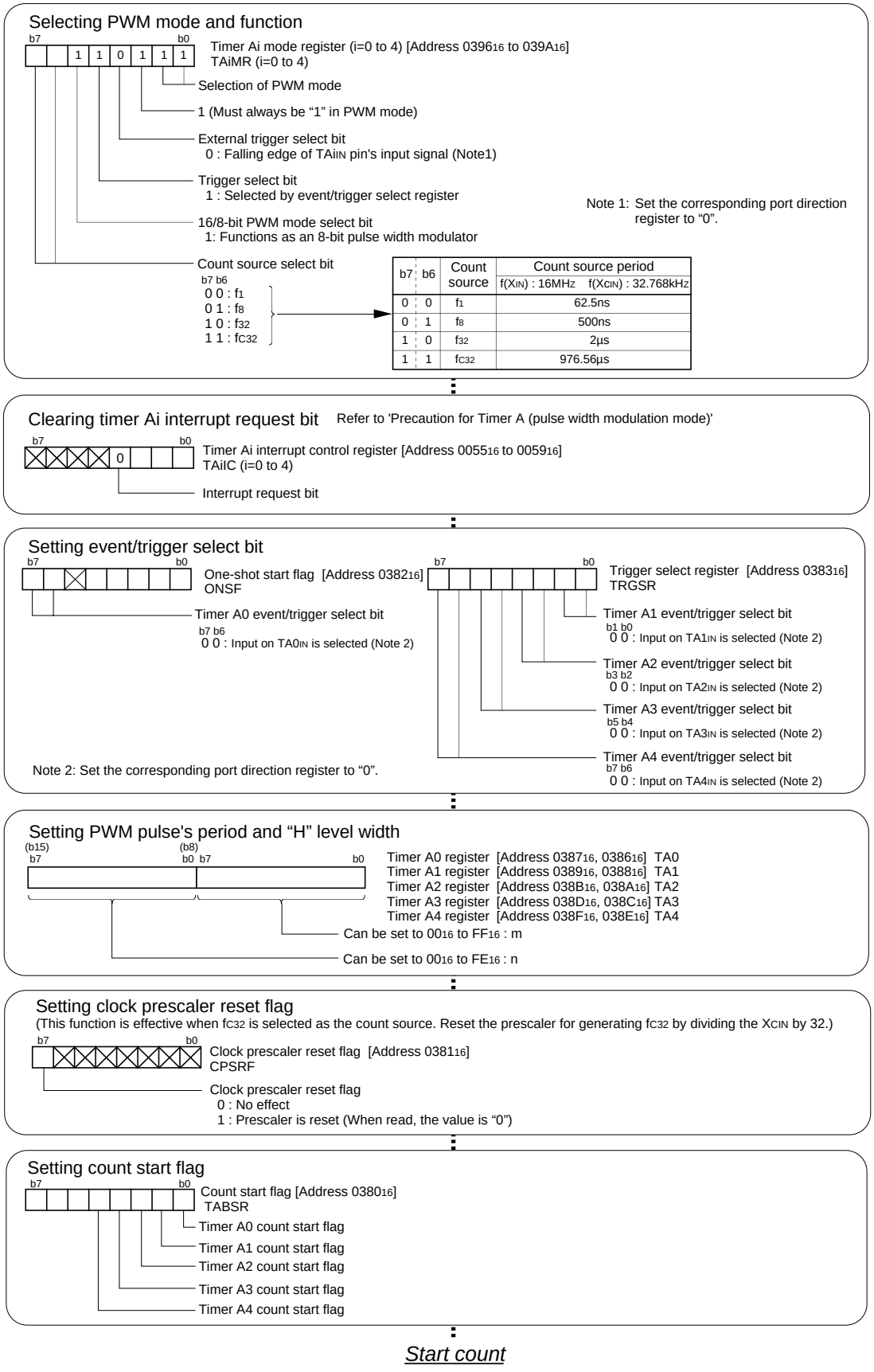


Figure 1. Operation timing of pulse width modulation mode, with 8-bit PWM mode selected

3.0 Set-up procedure



4.0 Programming Code

```
;******************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0040_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of Timer A
;               (pulse width modulation mode, 8-bit PWM mode)
;   HISTORY   : 2003.05.16  Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;******************************************************************************
;******************************************************************************
;       Include
;******************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;******************************************************************************
;       Symbol definition
;******************************************************************************
ROM_TOP         .EQU    0F8000H     ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFDCH     ;Start address of fixed vector
;
;******************************************************************************
;       Program area
;******************************************************************************
;==============================================================================
;       Start up
;==============================================================================
        .SECTION    PROGRAM, CODE   ;Declares section name and section type
        .ORG        ROM_TOP         ;Declares start address
RESET:
        MOV.B    #03H, prcr         ;Removes protect
                                    ;Set processor mode registers 0 and 1
        MOV.B    #00000000B, pm0    ; Single-chip mode
        MOV.B    #00000000B, pm1    ; No expansion, No wait
                                    ;Set system clock control registers 0 and 1
        MOV.B    #00001000B, cm0    ; Xcin-Xcout High
        MOV.B    #00100000B, cm1    ; Xin-Xout High, Main clock is No divison
        MOV.B    #00H, prcr         ;Protects all registers
;
```

```
;=============================================================================
;       TimerA (pulse width modulation mode,8-bit PWM mode selected)
;=============================================================================
        MOV.B    #01110111B, ta1mr ;Selecting PWM mode and function
;                 ||||||++---------;Selection of PWM mode
;                 |||||+-----------;Must always be "1" in PWM mode
;                 ||||+------------;Falling edge of TA1IN pin's input signal (Note)
;                 |||+-------------;Selected by event/trigger select register
;                 ||+--------------;Functions as an 8-bit pulse width modulator
;                 ++---------------;Count source (01:f8)
        MOV.B    #00000000B, ta1ic ;Clearing timerA1 interrupt request bit
;                     +------------;Interrupt request bit
        MOV.B    #00000000B, trgsr ;Setting event/trigger select bit
;                       ++---------;Input on TA1IN is selected (Note)
        BCLR     pd7_3             ;(Note) Set the corresponding port direction register to 0
        MOV.W    #6463H, ta1       ;Setting PWM pulse's period and "H" level width
;                 ||++-------------;m = timer Ai register's low-order address
;                 ++---------------;n = timer Ai register's high-order address
;                                   PWM pulse's period: 12.75(msec), @16MHz,f8
;                                   "H" level width: 5(msec), @16MHz,f8
        MOV.B    #00000000B, cpsrf ;Setting clock prescaler reset flag
;                 +----------------;Clock prescaler reset flag (0:No effect)
        MOV.B    #00000010B, tabsr ;Setting count starts flag
;                       +----------;TimerA1 count start flag
;
MAIN:
        JMP      MAIN
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*****************************************************************************
;       Setting of fixed vector
;*****************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    dummy    ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

http://www.renesas.com/

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
(Use the latest version on the Home page: http://www.renesas.com/)

User's Manual

M16C/62A group Rev. 1.0
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