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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M32C/84 Group

Operation of Timer A (event counter mode, free run type selected)

1. Abstract

In event counter mode, choose functions from those listed in Table 1. Operations of the circled items are described below. Figure 1 shows the operation timing, and Figure 2 shows the set-up procedure.

A reference program is an example when using the Timer A0 interrupt based on the setting procedure of Figure 2.

2. Introduction

This application note is applied to the M32C/84 group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M32C/84 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation

3. Chosed functions

Table 1. Chosed functions

Item	Set-up	Item	Set-up
Count source	○ Input signal to TAIIN (counting falling edges)	Pulse output function	○ No pulses output
	○ Input signal to TAIIN (counting rising edges)	○ Pulses output	
	○ Timer overflow (TB2/TAj overflow)	Count operation type	○ Reload type
		○ Free-run type	
		○ Content of up/down flag	
		○ Input signal to TAIOUT	

Note: j=i-1, but j=4 when i=0

4. Operation

- (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.
- (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer Ai interrupt request bit goes to "1".
- (3) If switching from an up count to a down count or vice versa while a count is in progress, the switch takes effect from the next effective edge of the count source.
- (4) Even if an overflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the timer Ai interrupt request bit goes to "1".

Note

- When not using pulse output, do not select TAIOUT output function with the function select register A and B.

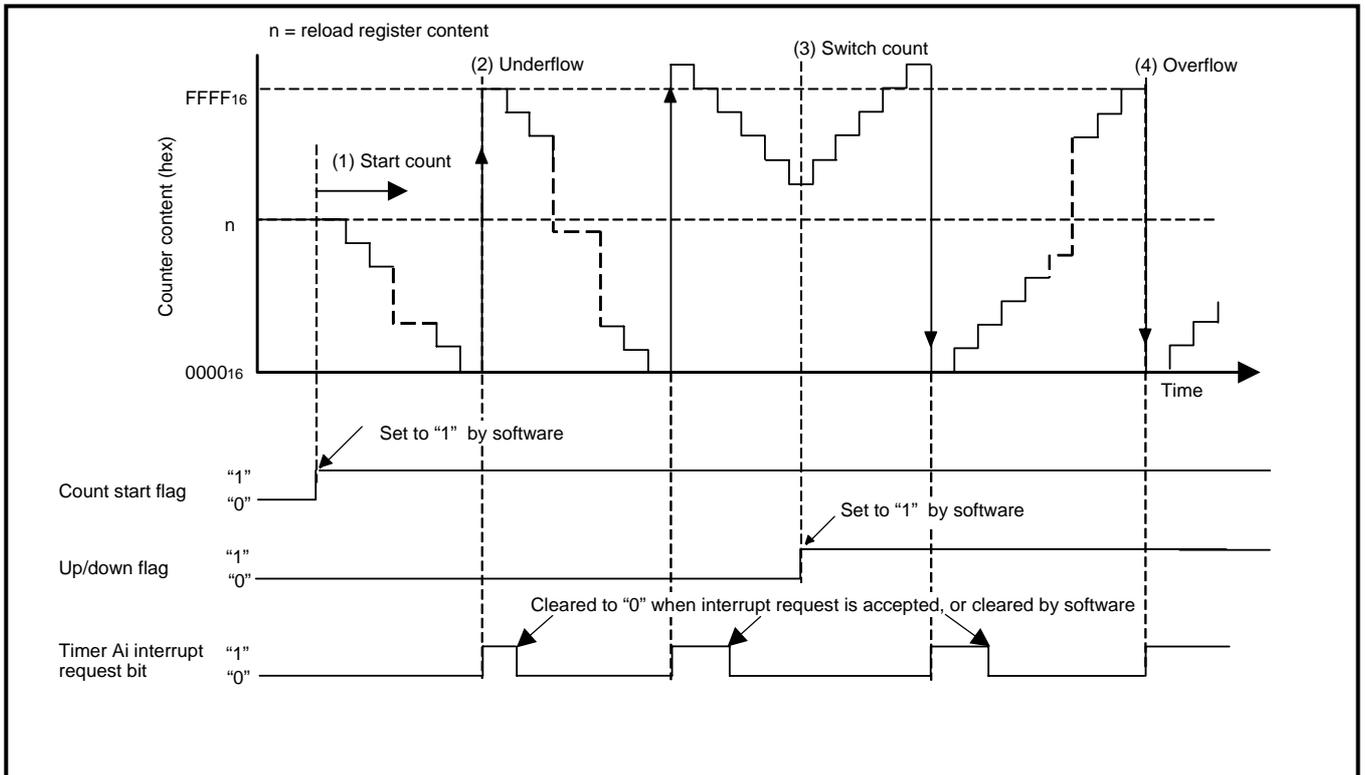


Figure 1. Operation timing of event counter mode, free run type selected

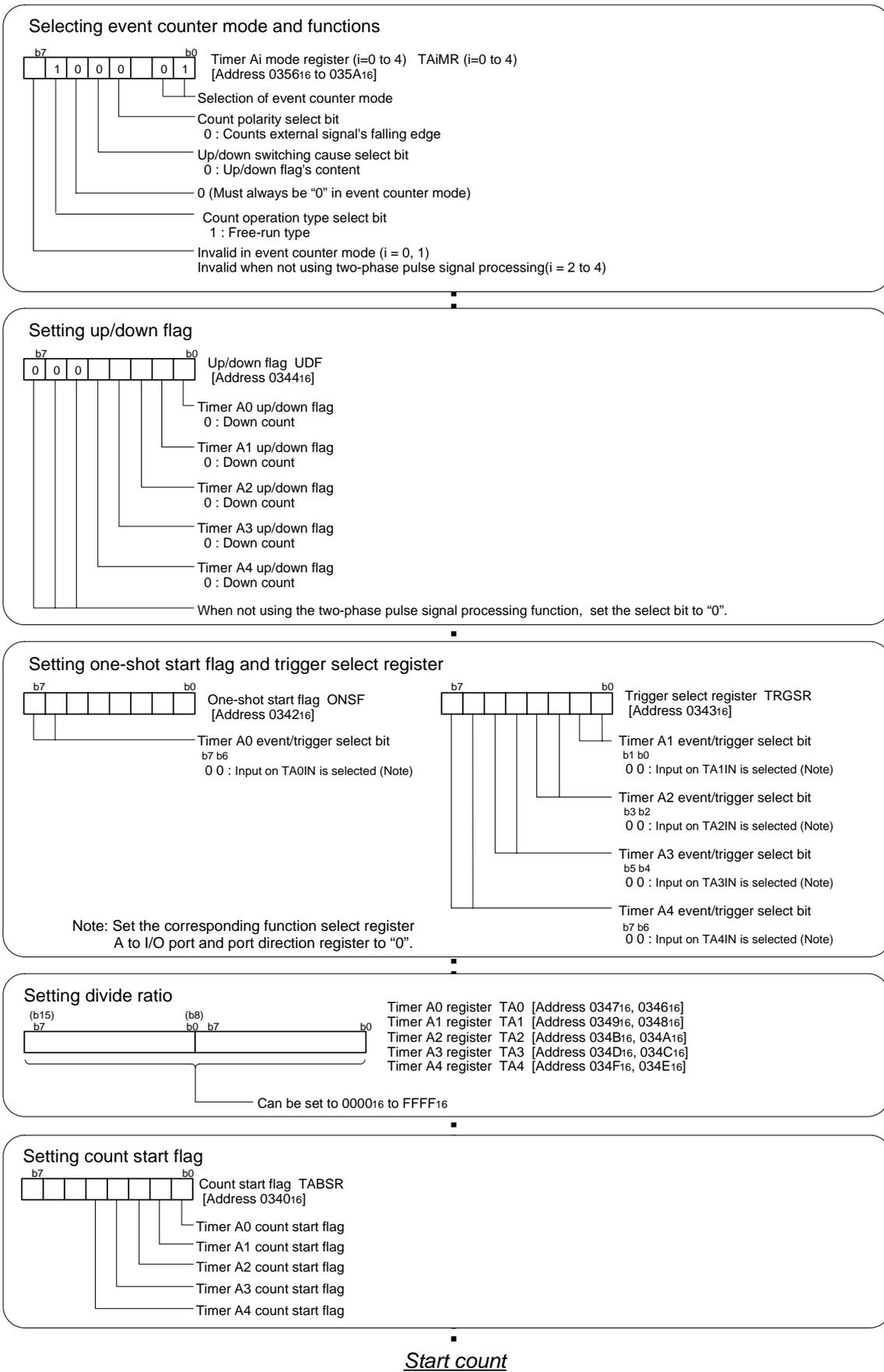


Figure 2. Set-up procedure of event counter mode, free run type selected

5. The example of reference program

```

*****
;
;
; M32C/84 Program Collection
;
; FILE NAME : rjj05b0711_src.a30
; CPU      : M32C/84 Group
; FUNCTION : Operation of Timer A (event counter mode, free run type selected)
; HISTORY  : 2005.1.31 Ver 1.00
;
; Copyright(C)2005, Renesas Technology Corp.
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; All rights reserved.
;
*****
;
; Include
*****
;
; .LIST      off          ;Stops outputting lines to the assembler list file
; .INCLUDE   sfr32c84.inc ;Reads the file that defined SFR
; .LIST      on          ;Starts outputting lines to the assembler list file
;
;
*****
;
; Symbol definition
*****
;
;
RAM_TOP      .equ    000400h    ;Start address of RAM
RAM_END      .equ    002affh    ;End address of RAM
ROM_TOP      .equ    0fe0000h   ;Start address of ROM
VECT_TOP     .equ    0ffe00h    ;Start address of vect_top
FIXED_VECT_TOP .equ    0fffdch   ;Start address of fixed_vect_top
;
;
*****
;
; Program area
*****
;
;=====  

; Start up  

;=====  

; .SECTION   PROGRAM, CODE    ;Declares section name and section type
; .ORG      ROM_TOP          ;Declares start address
START:
ldc         #RAM_END+1,isp    ;Sets interrupt stack pointer
mov.b      #03h, prcr        ;Removes protect
mov.b      #00000000b, pm0    ;Single-chip mode
mov.b      #00000000b, pm1    ;

```

Operation of Timer A (event counter mode, free run type selected)

```

mov.b      #00001000b, cm0      ;Xcin-Xcout High
mov.b      #00100000b, cm1      ;
mov.b      #00010010b, mcd      ;No division mode
mov.b      #00h, prcr           ;Protects all registers
ldc        #VECT_TOP,intb       ;Sets interrupt table register
;
;=====
;      Main program
;=====
;
mov.b      #01000001b, ta0mr     ;Timer A0 mode register
;      |||||  ++-----;Selection of event counter mode
;      |||||
;      ||||| +-----;Count polarity select bit
;      |||||           ;(0:counts external signal's falling edge)
;      ||| +-----;Up/down switching cause select bit (0:up/down flag's
;      |||             ;content)
;      || +-----;Must always be "0" in event counter mode
;      | +-----;Count operation type select bit (1:free-run type)
;      +-----;When not using the 2-phase pulse signal processing
;              ;function, set the select bit to "0"
mov.b      #00000000b, udf      ;
;      |||  +-----;Timer a0 up/down flag (0:down count)
;      +++-----;When not using the 2-phase pulse signal processing
;              ;function, set the select bit to "0"
mov.b      #00000000b, onsf     ;
;      ++-----;Timer a0 event/trigger select bit
;              ;(00:input on ta0in is selected) (note)
bclr       pd7_1                ;(Note)Set the corresponding port direction
;              ;register to "0"(TA0IN)
bclr       ps1_1                ;Port p7_1 is i/o port
mov.w      #5, ta0              ;Timer A0 register
mov.b      #00000011b,ta0ic     ;Interrupt control register
;      |+++-----;Interrupt priority level select bit
;      |           ;(011:Level 3, interrupt disabled)
;      +-----;Interrupt request bit (0:interrupt not requested)
mov.b      #00000001b, tabsr    ;
;              +-----;Timer a0 count start flag
fset       i                    ;Set interrupt enable flag
;
MAIN:
      jmp      MAIN
;
;=====
;      Interrupt program
;=====
TA0_INT:

```

```

;           ;/ TA0 interrupt routine /
;           reit
;
;=====
;           Dummy interrupt processing program
;=====
DUMMY:
           reit
;
;*****
;           Setting of variable vector table
;*****
;
;           .SECTION      VECT,ROMDATA
;           .ORG          VECT_TOP + (8*4)
;
;           .lword        DUMMY          ;DMA0 interrupt vector
;           .lword        DUMMY          ;DMA1 interrupt vector
;           .lword        DUMMY          ;DMA2 interrupt vector
;           .lword        DUMMY          ;DMA3 interrupt vector
;           .lword        TA0_INT        ;TA0 interrupt vector
;           .lword        DUMMY          ;TA1 interrupt vector
;           .lword        DUMMY          ;TA2 interrupt vector
;           .lword        DUMMY          ;TA3 interrupt vector
;           .lword        DUMMY          ;TA4 interrupt vector
;           .lword        DUMMY          ;UART0 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART0 receive/ACK interrupt vector
;           .lword        DUMMY          ;UART1 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART1 receive/ACK interrupt vector
;           .lword        DUMMY          ;TB0 interrupt vector
;           .lword        DUMMY          ;TB1 interrupt vector
;           .lword        DUMMY          ;TB2 interrupt vector
;           .lword        DUMMY          ;TB3 interrupt vector
;           .lword        DUMMY          ;TB4 interrupt vector
;           .lword        DUMMY          ;INT5 interrupt vector
;           .lword        DUMMY          ;INT4 interrupt vector
;           .lword        DUMMY          ;INT3 interrupt vector
;           .lword        DUMMY          ;INT2 interrupt vector
;           .lword        DUMMY          ;INT1 interrupt vector
;           .lword        DUMMY          ;INT0 interrupt vector
;           .lword        DUMMY          ;TB5 interrupt vector
;           .lword        DUMMY          ;UART2 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART2 receive/ACK interrupt vector
;           .lword        DUMMY          ;UART3 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART3 receive/ACK interrupt vector
;           .lword        DUMMY          ;UART4 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART4 receive/ACK interrupt vector

```


6. Referense

Hardware manual

M32C/84 group (Tentative version) Hardware Manual Rev.0.50

(Use the latest version on the web-site: <http://www.renesas.com>)

7. Web-site and contact for support

Renesas web-site

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Revision

Rev.	Issue data	Revised	
		Page	Point
1.00	2005.1.31	-	First edition issued

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