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M16C/62P Group

Operation of Timer B (pulse period measurement mode)

1. Abstract

In pulse period/pulse width measurement mode, choose functions from those listed in Table 1. Operations of the circled items are described below. Figure 1 shows the operation timing, and Figure 2 shows the set-up procedure. A reference program is an example when using the Timer B0 interrupt based on the setting procedure of Figure 2.

2. Introduction

This application note is applied to the M16C/62P group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M16C/62P Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation



Choosed functions

Table 1. Choosed functions

Item		Set-up	
Count source	ce O Internal count source (f1 / f8 / f32 / fc32)		
Measurement			
mode		Pulse period measurement (interval between measurement pulse rising edge to rising edge)	
		Pulse width measurement (interval between measurement pulse falling edge to rising edge, and between rising edge to falling edge)	

4. Operation

- (1) Setting the count start flag to "1" causes the counter to start counting the count source.
- (2) If a measurement pulse changes from "H" to "L", the value of the counter goes to "0000h", and measurement is started. In this instance, an indeterminate value is transferred to the reload register. The timer Bi interrupt request does not generate.
- (3) If a measurement pulse changes from "H" to "L" again, the value of the counter is transferred to the reload register, and the timer Bi interrupt request bit goes to "1". Then the value of the counter becomes "0000h", and the measurement is started again.

Note

- The timer Bi interrupt request bit goes to "1" when an effective edge of a measurement pulse is input or timer Bi is overflowed. The factor of interrupt request can be determined by use of the timer Bi overflow flag within the interrupt routine.
- The value of the counter at the beginning of a count is indeterminate. Therefore, the timer Bi overflow flag may go to "1" and timer Bi interrupt request may be generated during the interval between a count start and an effective edge input.
- The timer Bi overflow flag is indeterminate after reset. The timer Bi overflow flag goes to "0" if timer Bi mode register is written to when the count start flag is "1". This flag cannot be set to "1" by software.

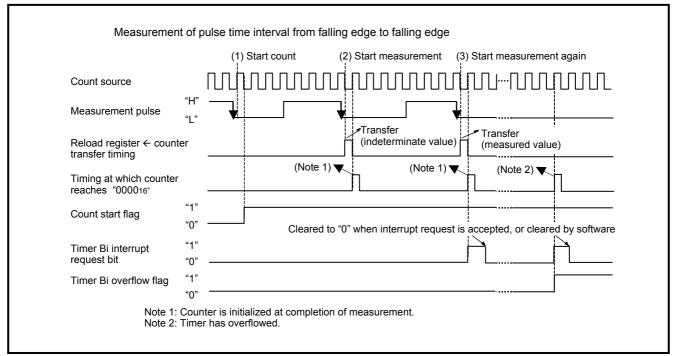


Figure 1. Operation timing of pulse period measurement mode



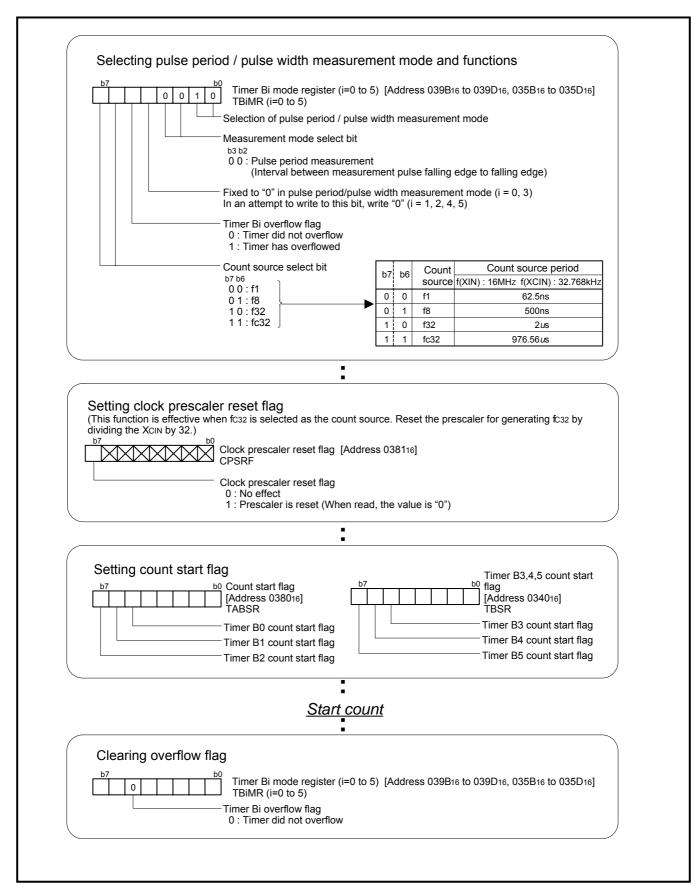


Figure 2. set-up procedure of pulse period measurement mode



5. The example of reference program

```
M16C/62P Program Collection
  FILE NAME: rjj05b0704_src.a30
  CPU
         : M16C/62P Group
  FUNCTION: Operation of Timer B (pulse period measurement mode)
  HISTORY : 2004.12.24 Ver 1.00
          : 2006.1.25 Ver 1.10
  Copyright(C)2006, Renesas Technology Corp.
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  All rights reserved.
  *******************************
     Include
  .LIST
             off
                             ;Stops outputting lines to the assembler list file
     .INCLUDE sfr62p.inc
                             ;Reads the file that defined SFR
     .LIST
                             ;Starts outputting lines to the assembler list file
             on
 *********************
     Symbol definition
RAM_TOP
                     00400h
                                 ;Start address of RAM
                .equ
RAM_END
                                 ;End address of RAM
                .equ
                     013ffh
ROM TOP
                     0f4000h
                                 ;Start address of ROM
                .equ
VECT_TOP
                     0ffe00h
                                 ;Start address of vect_top
                .equ
FIXED_VECT_TOP
                .equ
                     0fffdch
                                 ;Start address of fixed_vect_top
SB BASE
                      00380h
                                 ;Base address of sb
                .equ
     Program area
  Start up
;Declares section name and section type
          .section program,code
                     ROM_TOP
                                 ;Declares start address
          .org
                     SB_BASE
          .sb
```



START:			
	ldc	#RAM_END+1,is _l	p ;Sets interrupt stack pointer
	ldc	#SB_BASE,sb	;Sets sb register
,	mov.b	#03h,prcr	;Removes protect
		·	;Set processor mode registers 0 and 1
	mov.w	#0800h,pm0	;Single-chip mode
			;No expansion, No wait
	mov.w	#2008h,cm0	;Xcin-Xcout High
			;Xin-Xout High, Main clock is No divison
	mov.b	#0,prcr	;Protects all registers
,	ldintb	#VECT_TOP	;Sets interrupt table register
	mov.w	#0,r0	;Clears WORKRAM area
	mov.w	#((RAM_END+1)-	-RAM_TOP)/2,r3
	mov.w	#RAM_TOP,a1	
	sstr.w		
;=======	========	==========	=======================================
	in program		=======================================
,	mov.b		rr ;Timer B0 mode register
;		++	;Pulse period/pulsewidgh measurement mode
;		++	;Pulse period measurement (measurement between
;		Ш	;a falling adge ;and the next falling adge of measured
;			;pulse)
;			;Set to "0" in pulse period and pulse widge measurement
			;mode ;Timer has not overflowed
,		1.1	;Count source(f8)
,	mov.b		; ;Interrupt control register
;			;Interrupt priority level select bit
•		i	;(011:Level 3, interrupt disabled)
;		+	;Interrupt request bit (0:interrupt not requested)
	mov.b	#00100000b,tabs	sr ;Count start flag
;		+	;Starts counting
	nop		;To set the MR3 bit to "0" (no overflow), set TBiMR
	nop		register with setting the TBiS bit to "1" and counting the
	nop		;next count source after setting the MR3 bit to "1"
	nop		;(overflow). Newly added in the Ver 1.10
	nop		;



	fset	i	;Set interrupt enable flag		
	mov.b	#01000010b,	tb0mr ;Timer B0 mode register		
;		+	;Timer did not overflowed		
MAIN:					
	imn	MAINI			
·====	jmp ========	MAIN ========	=======================================		
;	Interrupt program				
;====	===========	=========			
TB0_IN	IT:				
;	./ TD0 into	at accition of			
	;/ TB0 interru	pt routine /			
,	reit				
;=====					
;	Dummy interrupt prod	cessing program			
,		========			
DUMM'	Y: reit				
	reit				
, .*****	*******	********	******		
;	Setting of variable ve	tting of variable vector table			
.****** ,	*******	*******	************		
;					
	.section vec				
	.org	VECT_TOP +	(4 ^ 4)		
,	.lword	DUMMY	;INT3 interrupt vector		
	.lword	DUMMY	;TB5 interrupt vector		
	.lword	DUMMY	;TB4 interrupt vector		
			;UART1 bus collision detection interrupt vector		
	.lword	DUMMY	;TB3 interrupt vector		
			;UART0 bus collision detection interrupt vector		
	.lword	DUMMY	;SI/04/INT5 interrupt vector		
	.lword	DUMMY	;SI/03/INT4 interrupt vector		
	.lword	DUMMY	;UART2 bus collision detection interrupt vector		
	.lword	DUMMY	;DMA0 interrupt vector		
	.lword	DUMMY	;DMA1 interrupt vector		
	.lword	DUMMY	;KEY interrupt vector		
	.lword	DUMMY	;A-D interrupt vector		
	.lword	DUMMY	;UART2 transmit/NACK interrupt vector		
	.lword	DUMMY	;UART2 receive/ACK interrupt vector		
	.lword	DUMMY	;UART0 transmit/NACK interrupt vector		
	.lword	DUMMY	;UART0 receive/ACK interrupt vector		
	.lword	DUMMY	;UART1 transmit/NACK interrupt vector		



	.lword	DUMMY	;UART1 receive/ACK interrupt vector
	.lword	DUMMY	;TA0 interrupt vector
	.lword	DUMMY	;TA1 interrupt vector
	.lword	DUMMY	;TA2 interrupt vector
	.lword	DUMMY	;TA3 interrupt vector
	.lword	DUMMY	;TA4 interrupt vector
	.lword	TB0_INT	;TB0 interrupt vector
	.lword	DUMMY	;TB1 interrupt vector
	.lword	DUMMY	;TB2 interrupt vector
	.lword	DUMMY	;INT0 interrupt vector
	.lword	DUMMY	;INT1 interrupt vector
	.lword	DUMMY	;INT2 interrupt vector
•			
.*************************************	*******	*******	**********
; Setting	of fixed vector		
.*************************************	******	*******	*************
;			
	.section f_vect,ro		
	.org	FIXED_VECT_TC	OP
;			
;	.lword	DUMMY	;Undefined instruction interrupt vector
;	.lword	DUMMY	;Overflow (INTO instruction) interrupt vector
;	.lword	DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector
;	.lword .lword .lword	DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector
;	.lword .lword .lword	DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector
;	.lword .lword .lword	DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector
;	.lword .lword .lword	DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt
;	.lword .lword .lword	DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt ;vector
;	.lword .lword .lword .lword	DUMMY DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt ;vector ;Voltage down detection interrupt vector
;	.lword .lword .lword .lword	DUMMY DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt ;vector ;Voltage down detection interrupt vector ;DBC interrupt vector
;	.lword .lword .lword .lword .lword	DUMMY DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt ;vector ;Voltage down detection interrupt vector ;DBC interrupt vector ;NMI interrupt vector
;	.lword .lword .lword .lword	DUMMY DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt ;vector ;Voltage down detection interrupt vector ;DBC interrupt vector
;	.lword .lword .lword .lword .lword	DUMMY DUMMY DUMMY DUMMY DUMMY	;Overflow (INTO instruction) interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;Single-step interrupt vector ;Watchdog timer interrupt vector ;Oscillation stop and Re-oscillation detection interrupt ;vector ;Voltage down detection interrupt vector ;DBC interrupt vector ;NMI interrupt vector



6. Referense

Hardware manual
M16C/62P Group Hardware Manual
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