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April 1st, 2010 Renesas Electronics Corporation

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M16C/62A Group

Operation of Timer B (event counter mode)

1.0 Abstract

In event counter mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item		Set-up
Count source	0	Input signal to the TBin pin (counting falling edges)
		Input signal to the TBiเท pin (counting rising edges)
		Input signal to the TBiin pin (counting rising edges and falling edges)
		Timer overflow(TBj overflow)

Note: j = i - 1, but j = 2 when i = 0, j = 5 when i = 3

2.0 Introduction

Operation (1) Setting the count start flag to "1" causes the counter to count the falling edges of the count source.

- (2) If an underflow occurs, the content of the reload register is reloaded, and the count continues. At this time, the timer Bi interrupt request bit goes to "1".
- (3) Setting the count start flag to "0" causes the counter to hold its value and to stop.

Figure 1 shows the operation timing

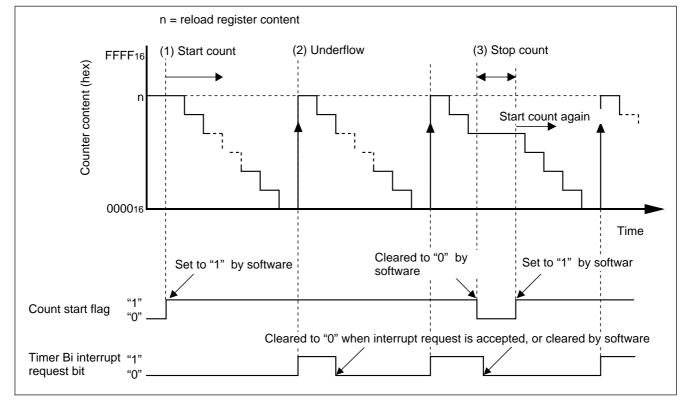
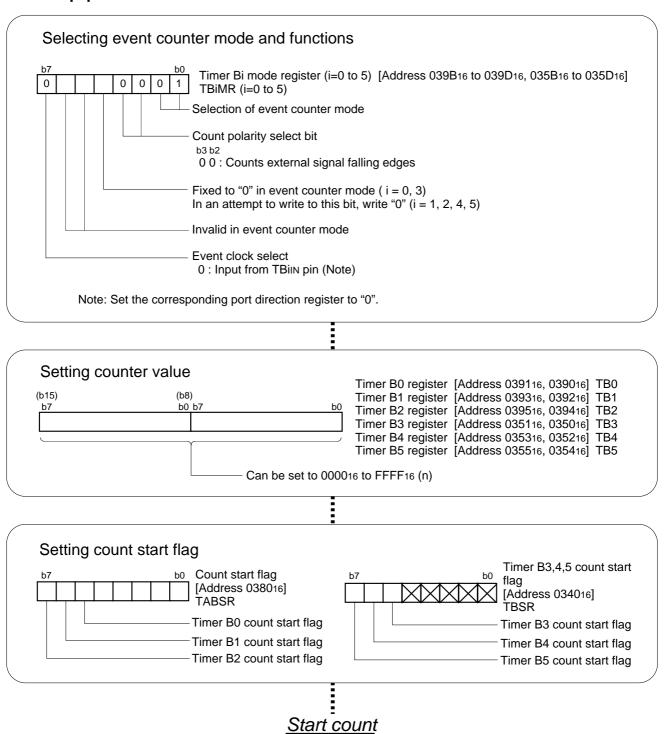


Figure 1. Operation timing of event counter mode



M16C/62A Group Operation of Timer B (event counter mode)

3.0 Set-up procedure





M16C/62A Group Operation of Timer B (event counter mode)

4.0 Programming Code

```
M16C/62A Program Collection
 FILE NAME : rjj05b0042_src.a30
 CPU : M16C/62A Group
 FUNCTION : Operation of Timer B
       (event counter mode)
 HISTORY : 2003.05.16 Ver 1.00
 Copyright(C)2003, Renesas Technology Corp.
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Include
.LIST OFF ;Stops outputting lines to the assembler list file
   .INCLUDE sfr62a.inc ;Reads the file that defined SFR
   .LIST
         ON
                 ;Starts outputting lines to the assembler list file
Symbol definition
ROM_TOP .EQU 0F8000H ;Start address of ROM
FIXED_VECT_TOP .EQU OFFFDCH ;Start address of fixed vector
C_CNT_TB_EV .EQU (08000H-1H); Counter value on event counter mode
Program area
.SECTION PROGRAM, CODE ; Declares section name and section type
         ROM_TOP
                ;Declares start address
RESET:
                  Removes protect
    MOV.B #03H, prcr
                  ;Set processor mode registers 0 and 1
    MOV.B #00000000B, pm0 ; Single-chip mode
    MOV.B #0000000B, pml; No expansion, No wait
                  ;Set system clock control registers 0 and 1
    MOV.B #00001000B, cm0; Xcin-Xcout High
    MOV.B #00100000B, cml ; Xin-Xout High, Main clock is No divison
    MOV.B
       #00H, prcr ;Protects all registers
```



M16C/62A Group Operation of Timer B (event counter mode)

```
TimerB (event counter mode)
#00000001B, tb0mr ; Selecting event counter mode and functions
             |||||++----;Selection of event counter mode
             ||||++----;Counts external signal falling edges
;
             |||+----;Fixed to "0" in event counter mode
;
             | ++----; Invalid in event counter mode
             +----; Event clock select (0:Input from TB0IN pin) (Note)
            #00000100B, prcr ;Clearing the protect (set to write-enabled state)
     MOV.B
                +----:Enables writing to port P9 direction register
                    ;(Note) Set the corresponding port direction register to \ensuremath{\text{0}}
           pd9_0
     BCLR
     MOV.W
            #C_CNT_TB_EV, tb0 ;Setting counter value
     MOV.B
            #00100000B, tabsr ;Setting count start flag
              +----;TimerB0 count start flag
MAIN:
            MAIN
     JMP
Dummy interrupt processing program
dummy:
Setting of fixed vector
.SECTION F_VECT, ROMDATA
            FIXED_VECT_TOP
     .LWORD
            dummy
                   ;Undefined instruction interrupt vector
     .LWORD
            dummy
                   ;Overflow (INTO instruction) interrupt vector
     .LWORD
            dummy
                   ;BRK instruction interrupt vector
     .LWORD
            dummy
                   ;Address match interrupt vector
     .LWORD
            dummy
                   ;Single-step interrupt vector
     .LWORD
            dummy
                   ;Watchdog timer interrupt vector
                   ;DBC interrupt vector
     .LWORD
            dummy
     .LWORD
            dummy
                   ;NMI interrupt vector
     .LWORD
            RESET
                   ;Sets reset vector
     .END
```



M16C/62A Group Operation of Timer B (event counter mode)

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

http://www.renesas.com/

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1 (Use the latest version on the Home page: http://www.renesas.com/)

User's Manual

M16C/62A group Rev. 1.0 (Use the latest version on the Home page: http://www.renesas.com/)

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