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M16C/62P Group

Operation of timer A (2-phase pulse single process in event counter mode, multiply-by-4 mode selected)

1. Abstract

In processing 2-phase pulse signals in event counter mode, choose functions from those listed in Table 1. Operations of the circled items are described below. Figure 1 shows the operation timing, and Figure 2 shows the set-up procedure. A reference program is an example when using the Timer A4 interrupt based on the setting procedure of Figure 2.

2. Introduction

This application note is applied to the M16C/62P group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M16C/62P Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation

3. Chooosed functions

Table 1. Chooosed functions

Item	Set-up		Item	Set-up	
Count operation type		Reload type	Processing 2 phase pulses (Note)		Normal processing
	0	Free run type		0	4-multiplication processing

Note: Timer A3 alone can be selected. Timer A2 is solely used for normal processes, and timer A4 is solely used for 4-multiplication processes.

4. Operation

- (1) Setting the count start flag to "1" causes the counter to count effective edges of the count source.
- (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the interrupt request bit goes to "1".
- (3) Even if an overflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the interrupt request bit goes to "1".

Note

- The conditions and effective edges of up count or down count are as follows:

Table 2. The conditions and effective edges of up count or down count

	Input signal to the TAIOUT pin	Input signal to the TAIiN pin		Input signal to the TAIOUT pin	Input signal to the TAIiN pin
Up count	"H" level	Rising	Down count	"H" level	Falling
	"L" level	Falling		"L" level	Rising
	Rising	"L" level		Rising	"H" level
	Falling	"H" level		Falling	"L" level

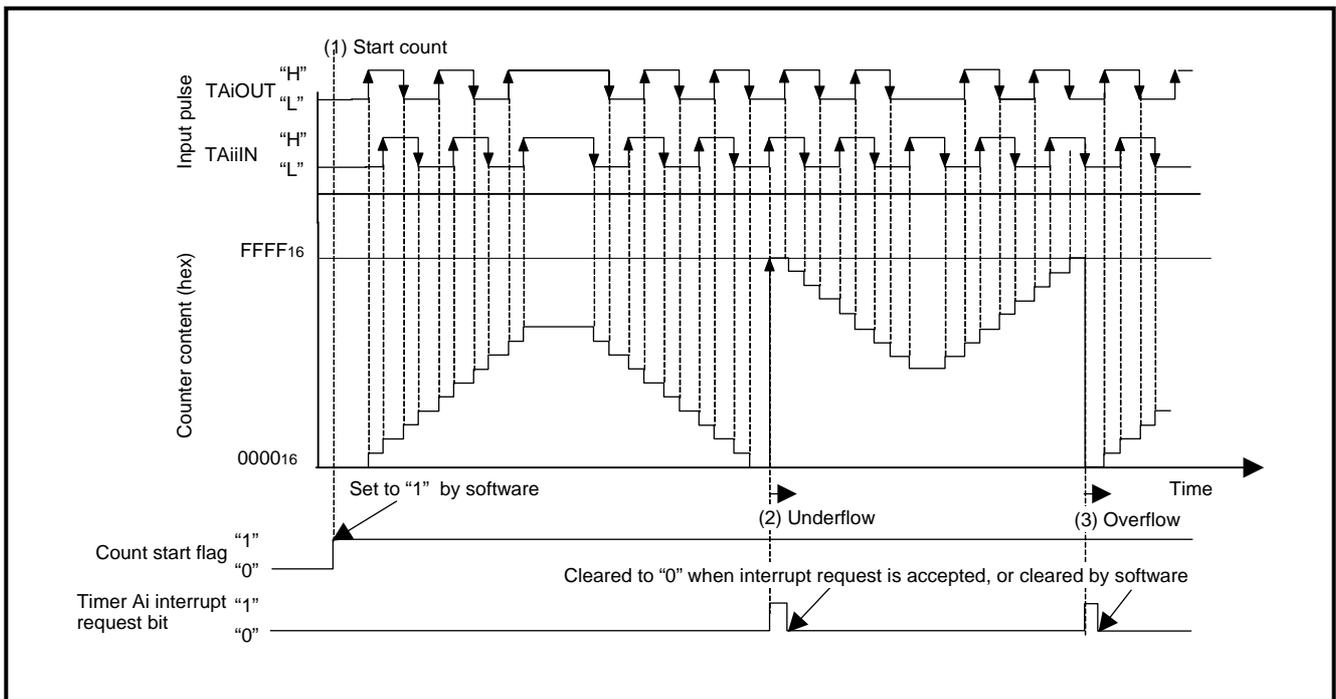
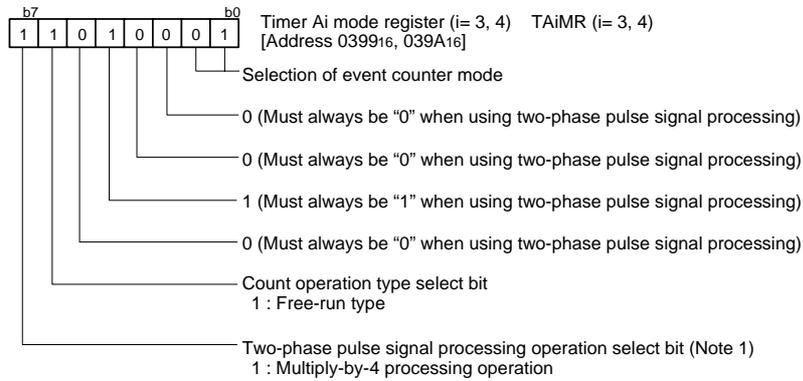


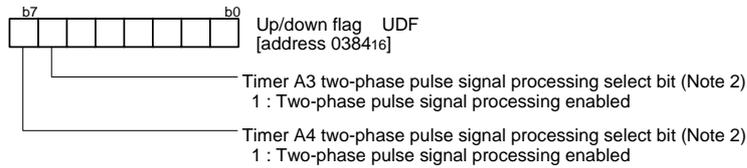
Figure 1. Operation timing of 2-phase pulse single process in event counter mode, multiply-by-4 mode selected

Selecting event counter mode and functions



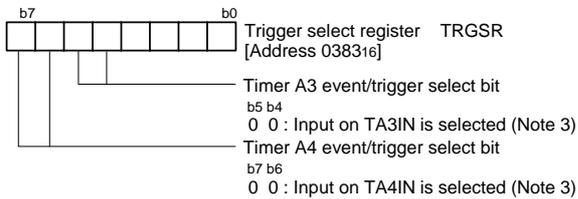
Note 1: This bit is valid for timer A3 mode register. For timer A4 mode register, this bit can be "0" or "1".

Setting two-phase pulse signal processing select bit



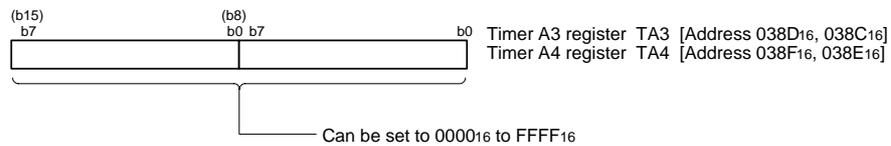
Note 2: Set the TAiIN, TAiOUT corresponding port direction register to "0".

Setting trigger select register

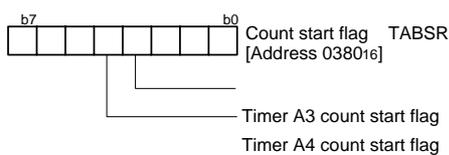


Note 3: Set the corresponding port direction register to "0".

Setting counter value



Setting count start flag



Start count

Figure 2. Set-up procedure of 2-phase pulse single process in event counter mode, multiply-by-4 mode selected

5. The example of reference program

```

*****
;
;
; M16C/62P Program Collection
;
; FILE NAME : rjj05b0694_src.a30
; CPU       : M16C/62P Group
; FUNCTION  : Operation of timer A (2-phase pulse single process in event
;            counter mode, multiply-by-4 mode selected)
; HISTORY   : 2004.12.24 Ver 1.00
;
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;
*****
;
*****
;
; Include
;
*****
;
; .LIST      off           ;Stops outputting lines to the assembler list file
; .INCLUDE   sfr62p.inc   ;Reads the file that defined SFR
; .LIST      on           ;Starts outputting lines to the assembler list file
;
;
*****
;
; Symbol definition
;
*****
;
RAM_TOP      .equ    00400h    ;Start address of RAM
RAM_END      .equ    013ffh    ;End address of RAM
ROM_TOP      .equ    0f4000h   ;Start address of ROM
VECT_TOP     .equ    0ffe00h   ;Start address of vect_top
FIXED_VECT_TOP .equ    0ffdch   ;Start address of fixed_vect_top
SB_BASE      .equ    00380h    ;Base address of sb
;
;
*****
;
; Program area
;
*****
;
=====
;
; Start up
;
=====
;
;
; .section program,code      ;Declares section name and section type
; .org      ROM_TOP         ;Declares start address
; .sb      SB_BASE          ;
;
;

```

START:

```

ldc          #RAM_END+1,isp ;Sets interrupt stack pointer
ldc          #SB_BASE,sb   ;Sets sb register
;
mov.b        #03h,prcr     ;Removes protect
;                               ;Set processor mode registers 0 and 1
mov.w        #0800h,pm0    ;Single-chip mode
;                               ;No expansion, No wait
mov.w        #2008h,cm0    ;Xcin-Xcout High
;                               ;Xin-Xout High, Main clock is No divison
mov.b        #0,prcr      ;Protects all registers
;
ldintb       #VECT_TOP    ;Sets interrupt table register

mov.w        #0,r0        ;Clears WORKRAM area
mov.w        #((RAM_END+1)-RAM_TOP)/2,r3
mov.w        #RAM_TOP,a1
sstr.w
;
;=====
; Main program
;=====
mov.b        #11010001b,ta4mr;Timer A4 mode register
;                               ||||| ++-----;Event counter mode
;                               ||||| +-----;To use two-phase pulse signal processing,
;                               |||||           ;set this bit to "0"
;                               ||||| +-----;To use two-phase pulse signal processing,
;                               |||||           ;set this bit to "0"
;                               ||| +-----;To use two-phase pulse signal processing,
;                               |||           ;set this bit to "1"
;                               || +-----;To use two-phase pulse signal processing,
;                               ||           ;set this bit to "0"
;                               | +-----;Free-run type
;                               +-----;Multiply-by-4 processing operation
mov.b        #10000000b,udf ;Up/down flag
;                               +-----;Two-phase pulse signal processing enabled
bclr         pd8_0         ;(Note)Set the corresponding port direction register to "0"
;                               ;(TA4OUT)
bclr         pd8_1         ;(Note)Set the corresponding port direction register to "0"
;                               ;(TA4IN)
mov.b        #00000000b,trgsr ;Trigger select register
;                               ++-----;Input on ta4in is selected
mov.w        #0,ta4        ;Timer A4 register
mov.b        #00000011b,ta4ic ;Interrupt control register
;                               |+++-----;Interrupt priority level select bit
;                               |           ;(011:Level 3, interrupt disabled)
;                               +-----;Interrupt request bit (0:interrupt not requested)

```

```

mov.b      #00010000b,tabsr;Count start flag
;
;          +-----;Starts counting
fset      i          ;Set interrupt enable flag
MAIN:
jmp       MAIN

;=====
;      Interrupt program
;=====
TA4_INT:

;          ;/ TA4 interrupt routine /
;
;          reit
;
;=====
;      Dummy interrupt processing program
;=====
DUMMY:
;          reit
;
;*****
;          Setting of variable vector table
;*****
;
;          .section vect,romdata
;          .org          VECT_TOP + (4 * 4)
;
;          .lword      DUMMY          ;INT3 interrupt vector
;          .lword      DUMMY          ;TB5 interrupt vector
;          .lword      DUMMY          ;TB4 interrupt vector
;          .lword      DUMMY          ;UART1 bus collision detection interrupt vector
;          .lword      DUMMY          ;TB3 interrupt vector
;          .lword      DUMMY          ;UART0 bus collision detection interrupt vector
;          .lword      DUMMY          ;SI/04/INT5 interrupt vector
;          .lword      DUMMY          ;SI/03/INT4 interrupt vector
;          .lword      DUMMY          ;UART2 bus collision detection interrupt vector
;          .lword      DUMMY          ;DMA0 interrupt vector
;          .lword      DUMMY          ;DMA1 interrupt vector
;          .lword      DUMMY          ;KEY interrupt vector
;          .lword      DUMMY          ;A-D interrupt vector
;          .lword      DUMMY          ;UART2 transmit/NACK interrupt vector
;          .lword      DUMMY          ;UART2 receive/ACK interrupt vector
;          .lword      DUMMY          ;UART0 transmit/NACK interrupt vector
;          .lword      DUMMY          ;UART0 receive/ACK interrupt vector
;          .lword      DUMMY          ;UART1 transmit/NACK interrupt vector
;          .lword      DUMMY          ;UART1 receive/ACK interrupt vector
;          .lword      DUMMY          ;TA0 interrupt vector

```

```

.word          DUMMY          ;TA1 interrupt vector
.word          DUMMY          ;TA2 interrupt vector
.word          DUMMY          ;TA3 interrupt vector
.word          TA4_INT        ;TA4 interrupt vector
.word          DUMMY          ;TB0 interrupt vector
.word          DUMMY          ;TB1 interrupt vector
.word          DUMMY          ;TB2 interrupt vector
.word          DUMMY          ;INT0 interrupt vector
.word          DUMMY          ;INT1 interrupt vector
.word          DUMMY          ;INT2 interrupt vector
;
;*****
;
;   Setting of fixed vector
;*****
;
;
;   .section f_vect,romdata
;   .org          FIXED_VECT_TOP
;
;   .word          DUMMY          ;Undefined instruction interrupt vector
;   .word          DUMMY          ;Overflow (INTO instruction) interrupt vector
;   .word          DUMMY          ;BRK instruction interrupt vector
;   .word          DUMMY          ;Address match interrupt vector
;   .word          DUMMY          ;Single-step interrupt vector
;   .word          DUMMY          ;Watchdog timer interrupt vector
;   .word          DUMMY          ;Oscillation stop and Re-oscillation detection interrupt
;   .word          DUMMY          ;vector
;   .word          DUMMY          ;Voltage down detection interrupt vector
;   .word          DUMMY          ;DBC interrupt vector
;   .word          DUMMY          ;NMI interrupt vector
;   .word          START        ;Sets start vector
;
;   .end

```

6. Referense

Hardware manual

M16C/62P group (M16C/62P,M16C/62PT) Hardware Manual Rev.2.30

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Revision

Rev.	Issue data	Revised	
		Page	Point
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