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M16C/65 Group

Operation of Timer A (2-phase pulse signal process in event counter mode, multiply-by-4 processing operation)

1. Abstract

In processing 2-phase pulse signals in event counter mode, choose functions from those listed in Table 1. Operations of the circled items are described below. Figure 1 shows the operation timing. A reference program is an example when using the Timer A4 interrupt based on the setting procedure in this application note.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up	
Count operation type		Reload type
	O	Free-run type
2-phase pulses process (Note)		Normal processing
	O	4-multiplication processing

Note: Timer A3 alone can be selected. Timer A2 is solely used for normal processing, and timer A4 is solely used for multiply-by-4 processing.

4. Operation

(1) Setting the count start flag to "1" causes the counter to count the effective edges of the count source.

(2) Even if an underflow occurs, the content of the reload register is not reloaded to the counter, but the count continues. At this time, the timer Ai interrupt request bit goes to "1".

(3) Even if an overflow occurs, the content of the reload register is not reloaded to the counter, but the count continues. At this time, the timer Ai interrupt request bit goes to "1".

Note:

● The conditions and effective edges of up count or down count are as follows:

Table 2. The conditions and effective edged of up count or down count

	Input signal to the TAiOUT pin	Input signal to the TAiIN pin		Input signal to the TAiOUT pin	Input signal to the TAiIN pin
Up count	"H" level	Rising	Down count	"H" level	Falling
	"L" level	Falling		"L" level	Rising
	Rising	"L" level		Rising	"H" level
	Falling	"H" level		Falling	"L" level

Figure 1 shows the operation timing.

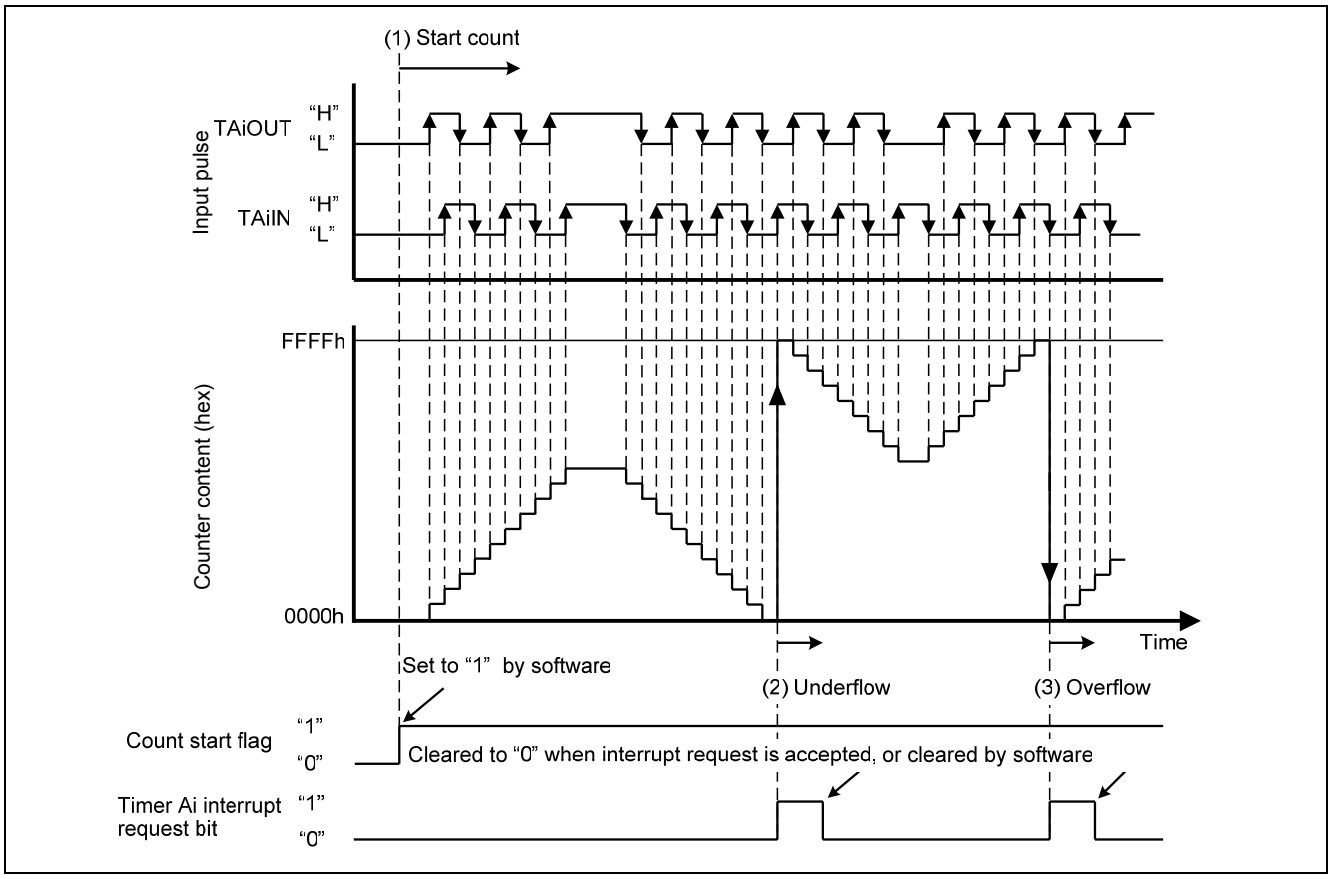
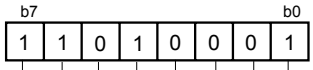


Figure 1. Operation timing of 2-phase pulse signal process in event counter mode, multiply-by-4 processing operation

5. Set-up procedure

Selecting event counter mode and functions



Timer Ai mode register (i=3, 4) [Address 0339h to 033Ah]
TAiMR (i=3, 4)

Selection of event counter mode

0 (Must always be “0” when using two-phase pulse signal processing)

0 (Must always be “0” when using two-phase pulse signal processing)

1 (Must always be “1” when using two-phase pulse signal processing)

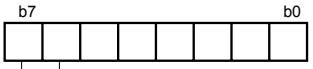
0 (Must always be “0” when using two-phase pulse signal processing)

Count operation type select bit
1 : Free-run type

Two-phase pulse signal processing operation select bit (Note 1)
1 : Multiply-by-4 processing operation

Note 1: This bit is valid for timer A3 mode register. For timer A4 mode register, this bit can be “0” or “1”.

Setting two-phase pulse signal processing select bit



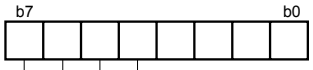
Up/down flag UDF [Address 0324h]

Timer A3 two-phase pulse signal processing select bit (Note 2)
1 : Two-phase pulse signal processing enabled

Timer A4 two-phase pulse signal processing select bit (Note 2)
1 : Two-phase pulse signal processing enabled

Note 2: Set the TAiIN,TAiOUT corresponding port direction register to “0”.

Setting trigger select register



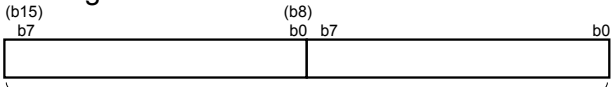
Trigger select register TRGSR [Address 0323h]

Timer A3 event/trigger select bit
b5 b4
0 0 : Input on TA3IN is selected(Note 3)

Timer A4 event/trigger select bit
b7 b6
0 0 : Input on TA4IN is selected(Note 3)

Note 3: Set the corresponding port direction register to “0”.

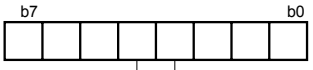
Setting counter value



Timer A3 register [Address 032Dh, 032Ch] TA3
Timer A4 register [Address 032Fh, 032Eh] TA4

Can be set to 0000h to FFFFh

Setting count start flag



Count start flag [Address 0320h]
TABSR

Timer A3 count start flag

Timer A4 count start flag

Start count

6. Reference

Hardware manual

M16C/65 Group Hardware Manual

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