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2010年4月1日  
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## M16C/65 群

### 当定时器 A 不足的情况下定时器脉冲输出的应用实例

#### 1. 要点

本篇应用说明描述了当定时器 A 不够执行定时器输出时，使用定时器 B 和 DMAC 执行定时器输出的步骤和应用实例。

#### 2. 说明

本篇资料，适用于 M16C/65 群单片机。

本篇应用说明也适用于 M16C 族中与上面所述的群具有相同 SFR（特殊功能寄存器）定义的产品。关于产品功能的改进，请参看手册中的相关信息。在使用本篇应用说明的程序前，需进行详细的评价。

### 3. 规格

在 M16C/65 群中，如何使用定时器 B 和 DMAC 执行定时器脉冲输出的例子进行说明。

- 系统：  
XIN = 20MHz、VCC1 = VCC2 = 5V
- DMAC：  
DMA 请求源 = TB0 中断请求、传送模式 = 重复传送、传送单位 = 8 位、原地址方向 = 正向（脉冲输出数据）、目标地址方向（端口 P0）
- TB0：  
定时器模式、时钟源 = f<sub>TIMAB</sub>、定时器周期 = 1ms（定时器的值 = 20000-1）

### 4. 操作

定时器 B0 每 1ms 下溢一次，此时，作为 DMA 传送输出端口的 P0\_0 的输出电平发生改变。工作时序图如下所示：

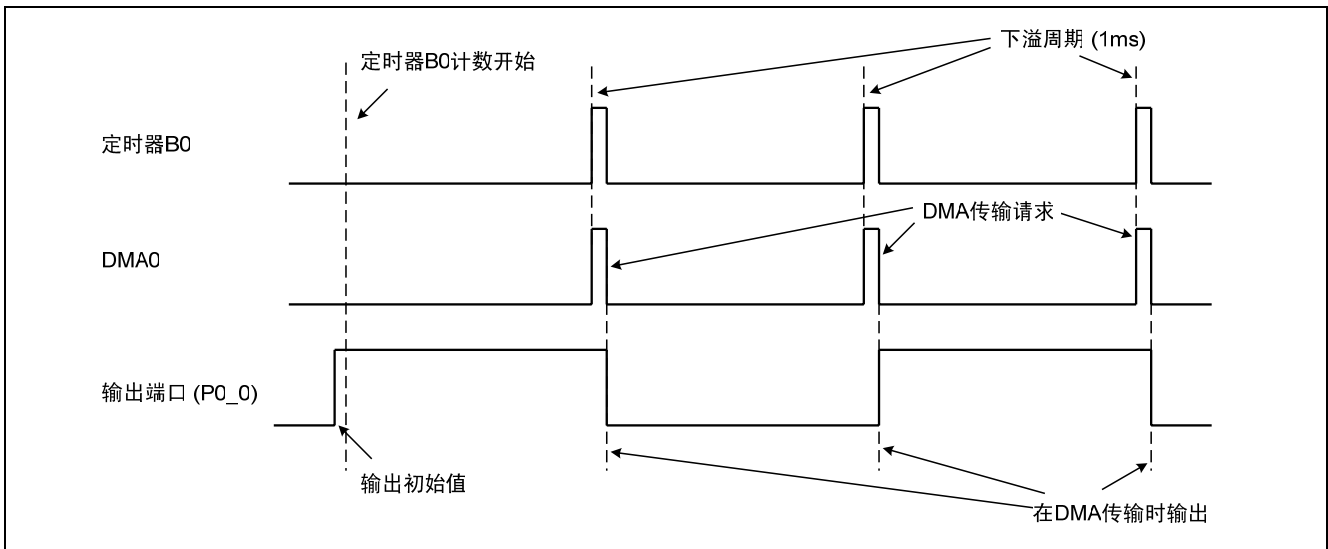


图 1. 脉冲输出的工作时序图

另外，在本参考例程中，由于 SFR 配置的原因，有些功能并未使用的位也可能被操作。所以，在用户系统中，请确认这些位的设定值符合其工作条件。

## 5. 寄存器设置

在定时器模式中，定时器 B 可以选择如表 1 中所列的各种计数源，定时器 B 计数源的结构框图如图 2 所示。

表 1. 定时器 B 计数源的选择

TCKDIVC0 寄存器 (注 1)	TBCSi 寄存器 (注 2)				TBiMR 寄存器		计数源	计数源周期
	TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		
TCDIV00								f(XIN):20MHz f(XcIN):32.768kHz f(oco-F):约 20MHz f(oco-s):约 125kHz
0	0	-	-	-	0	0	f1TIMAB/f2TIMAB (注 3)	50ns/100ns
0	0	-	-	-	0	1	f8TIMAB	400ns
0	0	-	-	-	1	0	f32TIMAB	1600ns
0	0	-	-	-	1	1	fc32	976.56μs
0	1	0	0	0	-	-	f1TIMAB/f2TIMAB (注 3)	50ns/100ns
0	1	0	0	1	-	-	f8TIMAB	400ns
0	1	0	1	0	-	-	f32TIMAB	1600ns
0	1	0	1	1	-	-	f64TIMAB	3200ns
0	1	1	0	0	-	-	foco-F	约 50ns
0	1	1	0	1	-	-	foco-s	约 8μs
0	1	1	1	0	-	-	fc32	976.56μs
1	1	0	0	0	-	-	f1TIMAB/f2TIMAB (注 3)	约 50ns/100ns
1	1	0	0	1	-	-	f8TIMAB	约 400ns
1	1	0	1	0	-	-	f32TIMAB	约 1600ns
1	1	0	1	1	-	-	f64TIMAB	约 3200ns

注 1: TCDIV00 位是定时器 AB 分频前时钟选择位。请在设定和定时器 A 相关的其它寄存器之前设定 TCDIV00 位。在改变 TCDIV00 位后，请再次设定和定时器 A 相关的其它寄存器。

注 2: TBCS0 寄存器的 TCS3~TCS0 位和定时器 B0 计数源的选择相对应，TBCS0 寄存器的 TCS7~TCS4 位和定时器 B1 计数源的选择相对应，TBCS1 寄存器的 TCS3~TCS0 位和定时器 B2 计数源的选择相对应，TBCS2 寄存器的 TCS3~TCS0 位和定时器 B3 计数源的选择相对应，TBCS2 寄存器的 TCS7~TCS4 位和定时器 B4 计数源的选择相对应，TBCS3 寄存器的 TCS3~TCS0 位和定时器 B5 计数源的选择相对应。

注 3: 如果 PCLKR 寄存器中的 PCLK0 位为“0”选择 f2TIMAB 作为计数源，PCLK0 位为“1”选择 f1TIMAB 作为计数源（复位设定值）。

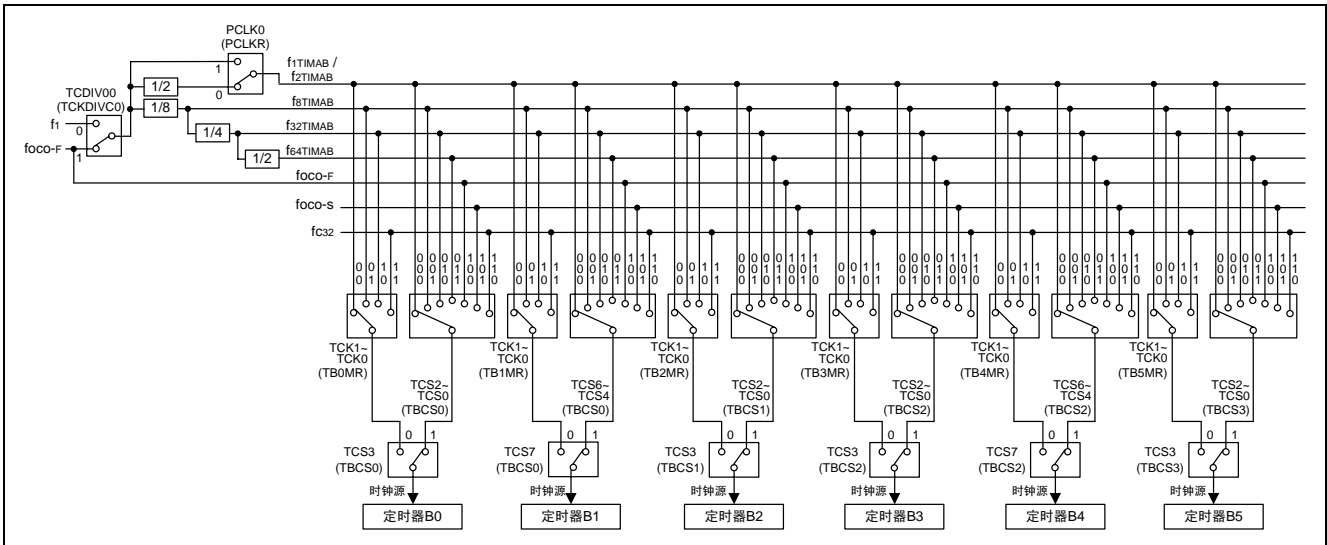


图 2. 定时器 B 的计数源

为了能够实现定义在“4.操作”的功能，下列寄存器必须按步骤顺序进行设置。对于每个寄存器的具体结构，请参考 M16C/65 群的硬件手册。

(1) 设定定时器B0

选择定时器AB分频前时钟

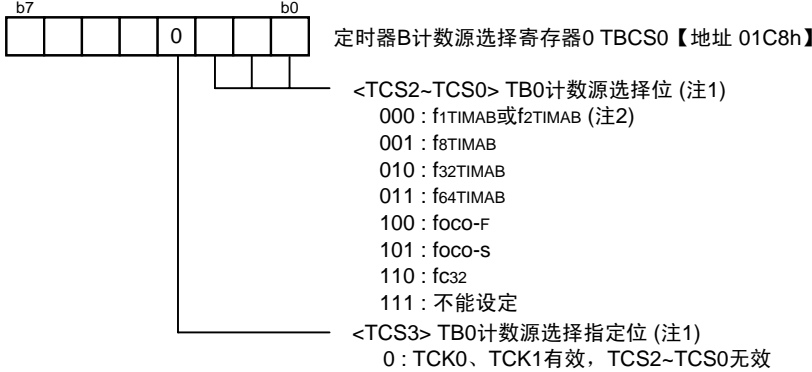
(请在设定和定时器A相关的其它寄存器之前设定TCDIV00位。在改变TCDIV00位后，请再次设定和定时器A相关的其它寄存器。)



- 定时器AB分频前时钟选择位
- 0 : f1
- 保留位
- 设定为“0”
- 什么也不指定。只能写“0”，读时值不定
- 保留位
- 设定为“0”

⋮

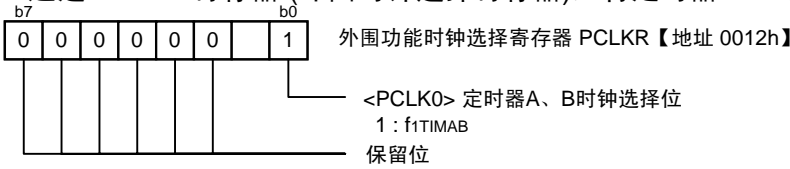
选择定时器计数源



注1: 关于各种设定情况下的计数源周期, 请参考表1。

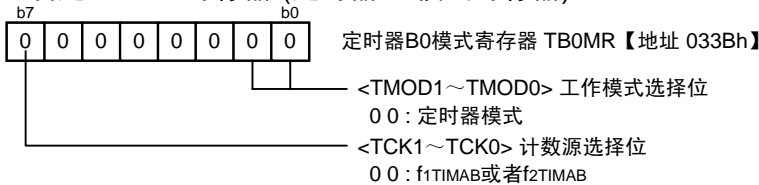
注2: 如果PCLKR寄存器中的PCLK0位为“0”选择f2TIMAB作为计数源, PCLK0位为“1”选择f1TIMAB作为计数源(复位设定值)。

通过PCLKR 寄存器 (外围时钟选择寄存器), 将定时器A、B的时钟源设定为f1TIMAB (注1)

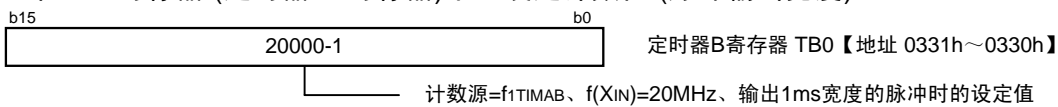


注1: 此寄存器必须在PRCR寄存器的PRC0位为“1” (允许写入) 时进行改写。

设定TB0MR寄存器 (定时器B0模式寄存器)

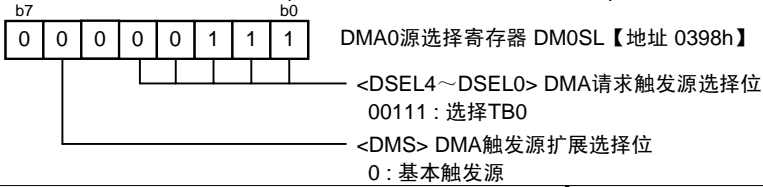


在TB0寄存器 (定时器B0寄存器)中, 设定计数值 (脉冲输出宽度)

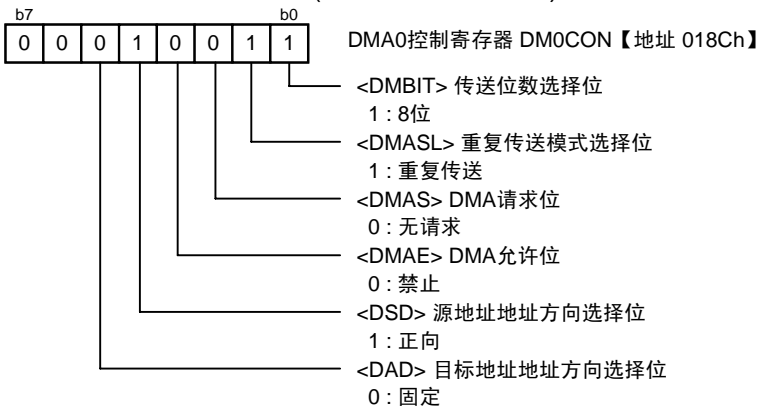


(2) 设定DMAC

设定DM0SL寄存器 (DMA0触发源选择寄存器)

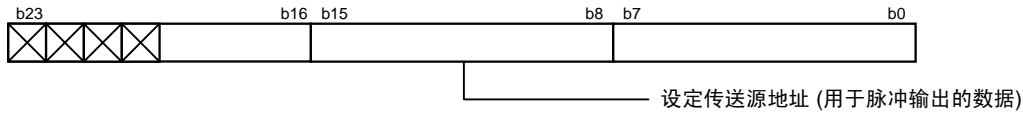


设定DM0CON寄存器 (DMA0控制寄存器)



设定SAR0寄存器 (DMA0源指针)

DMA0源指针 SAR0【地址 0182h~0180h】

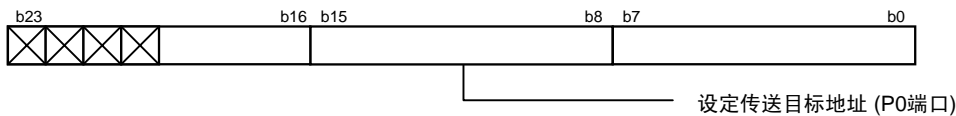


请按照以下方法设定用于脉冲输出的数据。

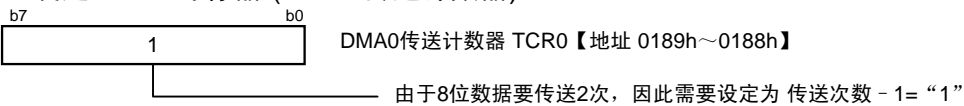
- 初始输出 = “低” 时  
char pulse\_data[2] = {0x00, 0x01};
- 初始输出 = “高” 时  
char pulse\_data[2] = {0x01, 0x00};

设定DAR0寄存器 (DMA0目标指针)

DMA0目标指针 DAR0【地址 0186h~0184h】



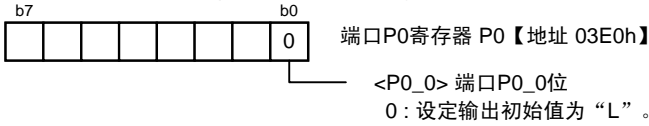
设定TCR0寄存器 (DMA0传送计数器)



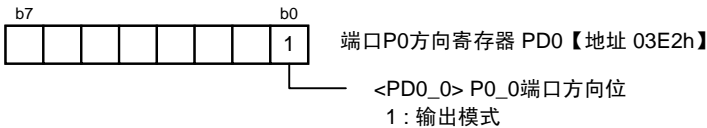


(3) 将P0\_0端口设定为用于脉冲输出的输出端口

设定P0寄存器(P0端口寄存器)

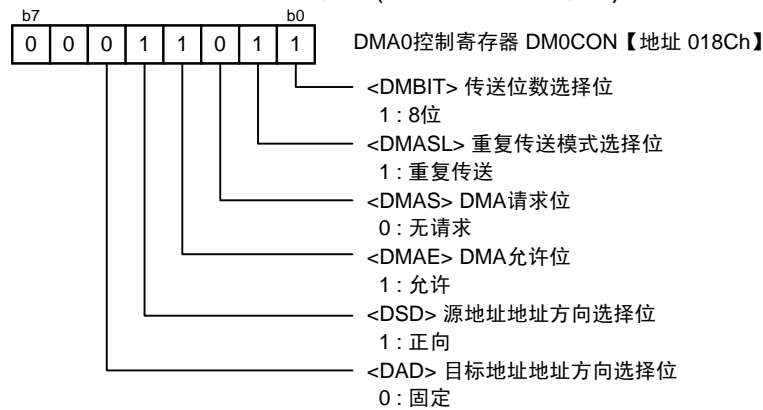


设定PD0寄存器(P0端口方向寄存器)



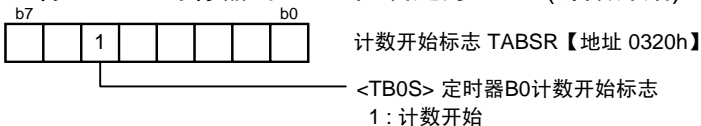
(4) 允许DMA

再次设定DM0CON寄存器(DMA0控制寄存器), 允许DMA传送



(5) 定时器B0计数开始

将TABS R寄存器的TB0S位设定为“1”(计数开始)



开始计数

6. 注意事项

当组合使用定时器 B 和 DMAC 进行定时器输出时，请注意以下事项。

(1) 由 DMAC 的规格所产生的限制

由于 DMAC，有以下限制：

- 如果 DMA 请求发生在其他中断顺序处理过程中，DMA 传送将继续等待。
- 当 DMA0 和 DMA1 同时产生 DMA 请求时，DMA0 由于优先级较高将首先被处理，DMA1 继续等待。因此，这里的操作不能用作短周期、高精度的应用，对于这种应用优先推荐使用定时器 A。

(2) 脉冲输出延迟

- 定时器 B 开始时的延迟时间

最初，定时器 B 开始时的脉冲输出，从端口方向寄存器被设置为输出时到定时器 B 开始时的执行时间为延迟时间。

- 由 DMA 传送产生的延迟时间

定时器 B 发生中断请求后，在 DMA 建立时间+DMA 传送周期数（参见“6. 注意事项”中的“(3) DMA 传送周期”）之后才输出实际的脉冲输出，这段延迟时间可以通过调整定时器的值来进行调整。

定时器 A 和定时器 B 在设定相同的定时器值的情况下脉冲输出延迟的实例如图 3 所示。

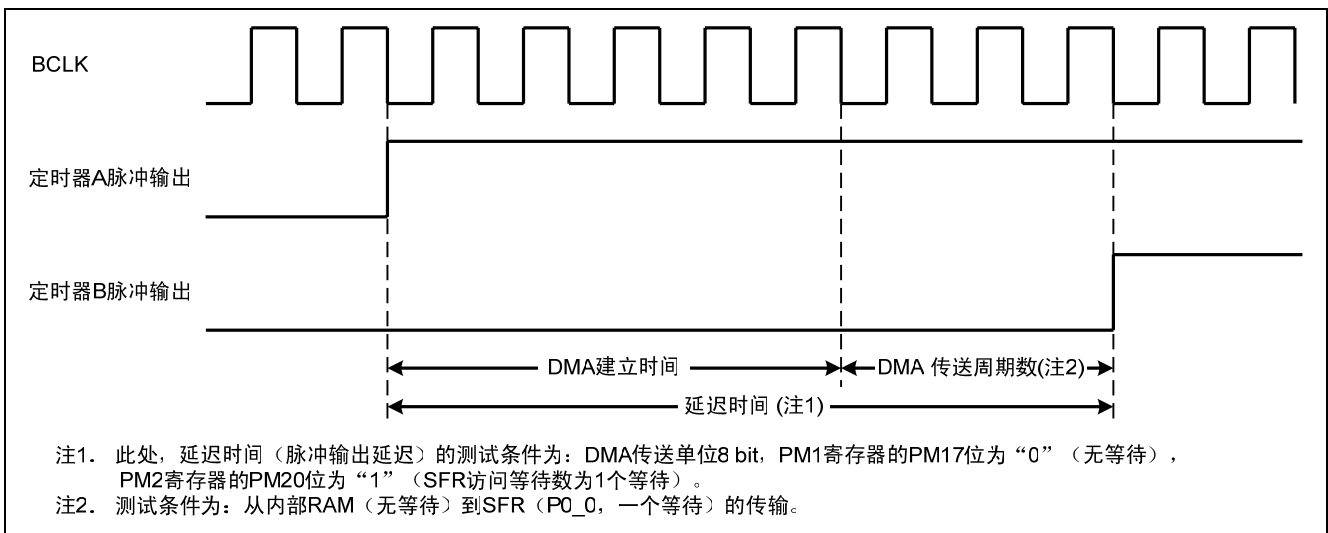


图 3. 脉冲输出延迟实例

(3) DMA 传送周期

DMAC 传送周期数可以由以下计算得出。

DMA 传送周期数如表 2 所示，系数 j、k 如表 3 所示。

$$\text{每个传送单元的传送周期数} = \text{读周期数} \times j + \text{写周期数} \times k$$

表 2. DMA 传送周期

传送单元	总线宽度	读取地址	单芯片模式		存储器扩展模式 微处理器模式	
			读周期数	写周期数	读周期数	写周期数
8 位传送	16 位	偶数	1	1	1	1
		奇数	1	1	1	1
	8 位	偶数	-	-	1	1
		奇数	-	-	1	1
16 位传送	16 位	偶数	1	1	1	1
		奇数	2	2	2	2
	8 位	偶数	-	-	2	2
		奇数	-	-	2	2

表 3. 系数 j、k

	内部区域				外部区域						
	内部 ROM、RAM		SFR		分离总线			复合总线			
	无等待	有等待	1 等待 (注 1)	2 等待 (注 2)	无等待	有等待 (注 1)			有等待 (注 1)		
						1 等待	2 等待	3 等待	1 等待	2 等待	3 等待
j	1	2	2	3	1	2	3	4	3	3	4
k	1	2	2	3	2	2	3	4	3	3	4

注 1: 取决于 CSE 寄存器的设定值。

注 2: 取决于 PM2 寄存器的 PM20 位的设定值。

#### (4) 输出端口的限制

由于 DMA 以 8 位为单位进行传送，所以除了 P0\_0 用作定时器脉冲输出外，其他的引脚（P0\_1~P0\_7）可用作输出端口。

## 7. 参考文献

数据手册

M16C/65 群硬件手册

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