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## M32C/84 Group

### Operation of timer A (2-phase process in event counter , multiply-by-4 and Z-phase)

#### 1. Abstract

In this mode, timer A3 counter can be set to "0" by selecting Z-phase input. Choose functions from those listed in Table 1. Operations of the circled items are described below. Figure 1 shows the operation timing, and Figure 2 shows the set-up procedure. A reference program is an example when using the INT2 interrupt based on the setting procedure of Figure 2.

#### 2. Introduction

This application note is applied to the M32C/84 group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M32C/84 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation

## 3. Choosed functions

**Table 1. Choosed functions**

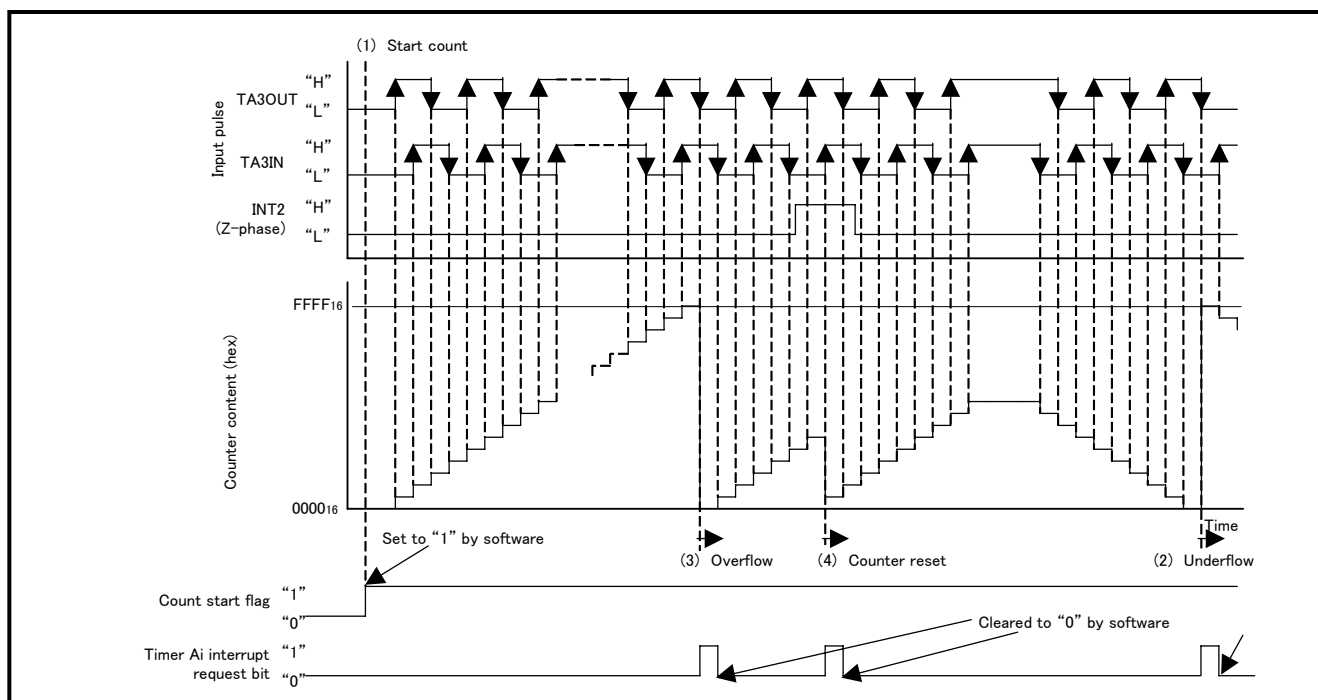
Item	Set-up	Item	Set-up
Count operation type	Reload type	Processing two-phase pulses (Note)	Normal processing
	<input type="radio"/> Free run type		<input type="radio"/> 4-multiplication processing
INT2 polarity	Falling edge		
	<input type="radio"/> Rising edge		

## 4. Operation

- (1) Setting the count start flag to "1" causes the counter to count effective edges of the count source.
- (2) Even if an underflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the interrupt request bit goes to "1".
- (3) Even if an overflow occurs, the content of the reload register is not reloaded, but the count continues. At this time, the interrupt request bit goes to "1".
- (4) When a rising edge is input to Z-phase (INT2 input), timer count value goes to "1". At this time, the interrupt request bit goes to "1".

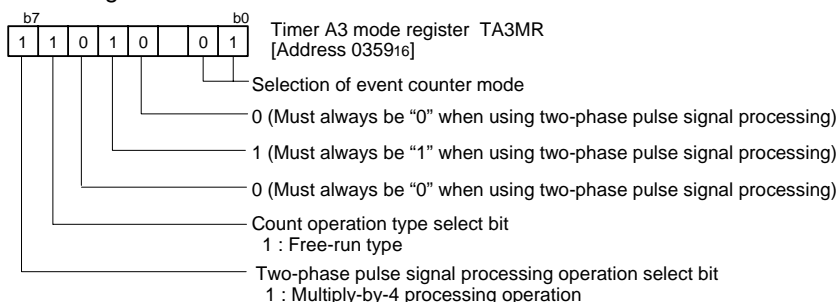
### Note

- The Z-phase is input when the INT2 input edge is detected. The edge polarity is selected by the INT2 polarity switch bit.
- The Z-phase must have a pulse width greater than 1 cycle of the timer A3 count source.
- Set TA3IN pin and TA3OUT pin's function select register A to I/O port and port direction register to "0".
- Note that timer A3 interrupt requests occur successively two times when timer A3 underflow and INT2 input reload are happened at the same timing.
- Do not use timer A3 interrupt request when this function is used.

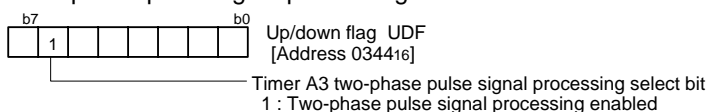


**Figure 1. Operation timing of 2-phase pulse single process in event counter mode, multiply-by-4 mode and Z-phase input selected**

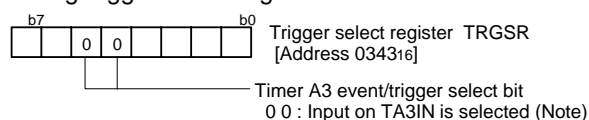
### Selecting event counter mode and functions



### Two-phase pulse signal processing select bit

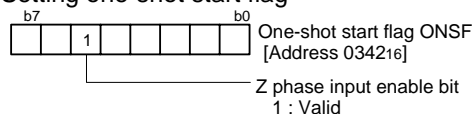


### Setting trigger select register

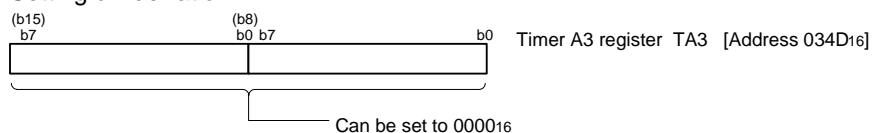


Note: Set the corresponding function select register A to I/O port, and port direction register to "0".

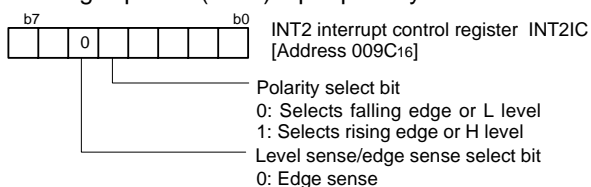
### Setting one-shot start flag



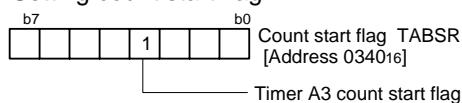
### Setting divide ratio



### Setting Z-phase (INT2) input polarity



### Setting count start flag



Start count

Figure 2. Set-up procedure of 2-phase pulse single process in event counter mode,multiply-by-4 mode and Z-phase input selected

## 5. The example of reference program

```

*****
;
;
;
;   M32C/84 Program Collection
;
;
;   FILE NAME : rjj05b0714_src.a30
;   CPU       : M32C/84 Group
;   FUNCTION  : Operation of timer A (2-phase pulse single process in event
;               : counter mode, multiply-by-4 mode Z-phase input selected)
;   HISTORY   : 2005.1.31   Ver 1.00
;
;
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;   All rights reserved.
;
*****
;
;
;   Include
;
*****
;
;
;   .LIST      off           ;Stops outputting lines to the assembler list file
;   .INCLUDE   sfr32c84.inc  ;Reads the file that defined SFR
;   .LIST      on           ;Starts outputting lines to the assembler list file
;
;
*****
;
;   Symbol definition
;
*****
;
;
RAM_TOP      .equ    000400h    ;Start address of RAM
RAM_END      .equ    002affh    ;End address of RAM
ROM_TOP      .equ    0fe0000h   ;Start address of ROM
VECT_TOP     .equ    0fffe00h   ;Start address of vect_top
FIXED_VECT_TOP .equ    0ffffdch ;Start address of fixed_vect_top
;
;
*****
;
;   Program area
;
*****
;
;=====
;
;   Start up
;
;=====
;
;   .SECTION   PROGRAM, CODE    ;Declares section name and section type
;   .ORG      ROM_TOP          ;Declares start address
;
START:
;
;   ldc        #RAM_END+1,isp   ;Sets interrupt stack pointer
;   mov.b      #03h, prcr       ;Removes protect
;   mov.b      #00000000b, pm0  ;Single-chip mode
;   mov.b      #00000000b, pm1  ;
;   mov.b      #00001000b, cm0  ;Xcin-Xcout High
;   mov.b      #00100000b, cm1  ;

```

```

mov.b      #00010010b, mcd      ;No division mode
mov.b      #00h, prcr           ;Protects all registers
ldc        #VECT_TOP,intb      ;Sets interrupt table register
;
;=====
;      Main program
;=====
;
mov.b      #11010001b,ta3mr     ;Timer A3 mode register
;      ||||| ++-----;Event counter mode
;      ||||| +-----;To use two-phase pulse signal processing,
;      |||||           ;set this bit to "0"
;      ||||| +-----;To use two-phase pulse signal processing,
;      |||||           ;set this bit to "0"
;      ||| +-----;To use two-phase pulse signal processing,
;      |||           ;set this bit to "1"
;      || +-----;To use two-phase pulse signal processing,
;      ||           ;set this bit to "0"
;      | +-----;Free-run type
;      +-----;Multiply-by-4 processing operation
mov.b      #01000000b,udf       ;Up/down flag
;      +-----;Two-phase pulse signal processing enabled
bclr       pd7_6                ;(Note)Set the corresponding port direction register to "0"
;                                ;(TA3OUT)
bclr       pd7_7                ;(Note)Set the corresponding port direction register to "0"
;                                ;(TA3IN)
bclr       ps1_6                ;Port P7_6 is I/O port
bclr       ps1_7                ;Port P7_7 is I/O port
mov.b      #00000000b,trgsr     ;Trigger select register
;      ++-----;Input on TA3IN is selected
mov.b      #00100000b,onsf     ;One-shot start flag
;      +-----;Z phase input enable bit
mov.w      #0000h,ta3          ;Timer A3 register
mov.b      #00010011b,int2ic    ;Interrupt control register
;      |+++-----;Interrupt priority level select bit
;      ||           ;(011:Level 3, interrupt disabled)
;      | +-----;Interrupt request bit (0:interrupt not requested)
;      +-----;Selects rising edge or H level
mov.b      #00000000b,ta3ic    ;Interrupt control register
;      |+++-----;Interrupt priority level select bit
;      |           ;(000:Level , interrupt disabled)
;      +-----;Interrupt request bit (0:interrupt not requested)
mov.b      #00001000b,tabsr     ;Count start flag
;      +-----;Starts counting
fset       i                   ;Set interrupt enable flag
;
MAIN:
      jmp      MAIN
;=====

```

```

; Interrupt program
;=====
INT2_INT:
;
;           ;/ INT2_INT interrupt routine /
;
;           reit
;
;=====
; Dummy interrupt processing program
;=====
DUMMY:
;           reit
;
;*****
;           Setting of variable vector table
;*****
;
;           .SECTION      VECT,ROMDATA
;           .ORG          VECT_TOP + (8*4)
;
;           .lword        DUMMY          ;DMA0 interrupt vector
;           .lword        DUMMY          ;DMA1 interrupt vector
;           .lword        DUMMY          ;DMA2 interrupt vector
;           .lword        DUMMY          ;DMA3 interrupt vector
;           .lword        DUMMY          ;TA0 interrupt vector
;           .lword        DUMMY          ;TA1 interrupt vector
;           .lword        DUMMY          ;TA2 interrupt vector
;           .lword        DUMMY          ;TA3 interrupt vector
;           .lword        DUMMY          ;TA4 interrupt vector
;           .lword        DUMMY          ;UART0 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART0 receive/ACK interrupt vector
;           .lword        DUMMY          ;UART1 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART1 receive/ACK interrupt vector
;           .lword        DUMMY          ;TB0 interrupt vector
;           .lword        DUMMY          ;TB1 interrupt vector
;           .lword        DUMMY          ;TB2 interrupt vector
;           .lword        DUMMY          ;TB3 interrupt vector
;           .lword        DUMMY          ;TB4 interrupt vector
;           .lword        DUMMY          ;INT5 interrupt vector
;           .lword        DUMMY          ;INT4 interrupt vector
;           .lword        DUMMY          ;INT3 interrupt vector
;           .lword        INT2_INT       ;INT2 interrupt vector
;           .lword        DUMMY          ;INT1 interrupt vector
;           .lword        DUMMY          ;INT0 interrupt vector
;           .lword        DUMMY          ;TB5 interrupt vector
;           .lword        DUMMY          ;UART2 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART2 receive/ACK interrupt vector
;           .lword        DUMMY          ;UART3 transmit/NACK interrupt vector
;           .lword        DUMMY          ;UART3 receive/ACK interrupt vector

```



```

.lword      DUMMY      ;UART4 transmit/NACK interrupt vector
.lword      DUMMY      ;UART4 receive/ACK interrupt vector
.lword      DUMMY      ;Bus collision detection,start/stop
                        ;condition detection (UART2) interrupt vector
.lword      DUMMY      ;Bus collision detection,start/stop
                        ;condition detection (UART3) interrupt vector
.lword      DUMMY      ;Bus collision detection,start/stop
                        ;condition detection (UART4) interrupt vector

.lword      DUMMY      ;A-D interrupt vector
.lword      DUMMY      ;KEY interrupt vector
.lword      DUMMY      ;IntelligentI/O interrupt vector0
.lword      DUMMY      ;IntelligentI/O interrupt vector1
.lword      DUMMY      ;IntelligentI/O interrupt vector2
.lword      DUMMY      ;IntelligentI/O interrupt vector3
.lword      DUMMY      ;IntelligentI/O interrupt vector4
.lword      DUMMY      ;IntelligentI/O interrupt vector8
.lword      DUMMY      ;IntelligentI/O interrupt vector9,CAN0
.lword      DUMMY      ;IntelligentI/O interrupt vector10,CAN1
.lword      DUMMY      ;CAN2

;
;
;*****
;
;      Setting of fixed vector
;*****
;
;
SECTION      F_VECT,ROMDATA
ORG          FIXED_VECT_TOP

;

.lword      DUMMY      ;Undefined instruction interrupt vector
.lword      DUMMY      ;Overflow interrupt vector
.lword      DUMMY      ;BRK instruction interrupt vector
.lword      DUMMY      ;Address match interrupt vector
.lword      DUMMY      ;
.lword      DUMMY      ;Watchdog timer interrupt vector
.lword      DUMMY      ;
.lword      DUMMY      ;NMI interrupt vector
.lword      START      ;Sets start vector

;

.end

```

## 6. Referense

### Hardware manual

M32C/84 group (Tentative version) Hardware Manual Rev.0.50

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		Page	Point
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