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Renesas Electronics Corporation

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M16C/Tiny Series

Operation of Serial I/O (Transmission in Clock-Synchronous Serial I/O Mode, Transfer Clock Output from Multiple Pins Function)

1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table1. Operations of the checked items are described below.

Table 1. Choosed Functions

Item	Set-up		Item	Set-up	
Transfer clock source	Yes	Internal clock (f_1/f_2/f_8/f_{32})	Transmission interrupt factor		Transmission buffer empty
		External clock (CLKi pin)		Yes	Transmission complete
$\overline{CTS}$ function		$\overline{CTS}$ function enabled	Output transfer clock to multiple pins (Note 1)		Not selected
	Yes	$\overline{CTS}$ function disabled		Yes	Selected
CLK polarity	Yes	Output transmission data at the falling edge of the transfer clock	Data logic select (Note 2)	Yes	No reverse
					Reverse
		Output transmission data at the rising edge of the transfer clock	TxD, RxD I/O polarity reverse function (Note 2)	Yes	No reverse
					Reverse
Transfer format	Yes	LSB first			
		MSB first			

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{CTS}$/$\overline{RTS}$ function can not be utilized. Set the UART1 $\overline{CTS}$/$\overline{RTS}$ disable bit to “1”.

Note 2: UART2 only

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

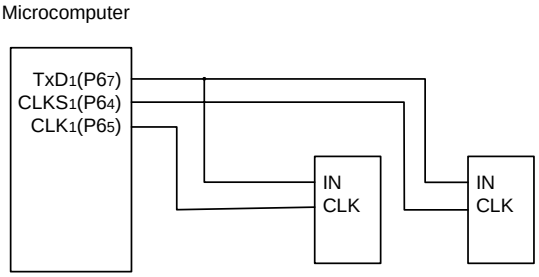
This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/26, M16C/26A, M16C/28, M16C/29 microcomputers. However, some functions may have been modified.
Refer to the User’s Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Operation of Serial I/O

(1) Setting the transmit enable bit to “1” makes data transmissible status ready.
(2) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.
(3) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that the transmission is completed. The transfer clock stops at “H” level. At this time, the UART1 transmit interrupt request bit goes to “1”.
(4) Setting CLK/CLKS select bit 1 to “1” and setting CLK/CLKS select bit 0 to “1” causes the CLKS1 pin to go to the transfer clock output pin. Change the transfer clock output pin when transmission is halted.
(5) When transmission data is written to the UART1 transmit buffer register, transmission data held in the UART1 transmit buffer register is transmitted to the UART1 transmit register in synchronization with the first falling edge of the transfer clock. At this time, the first bit of the transmission data is transmitted from the TxD1 pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges of the transfer clock.

Figure 1 shows the operation timing.

Example of wiring



Note: This applies when performing only transmission with an internal clock selected in the clock synchronous serial I/O mode.

Example of operation

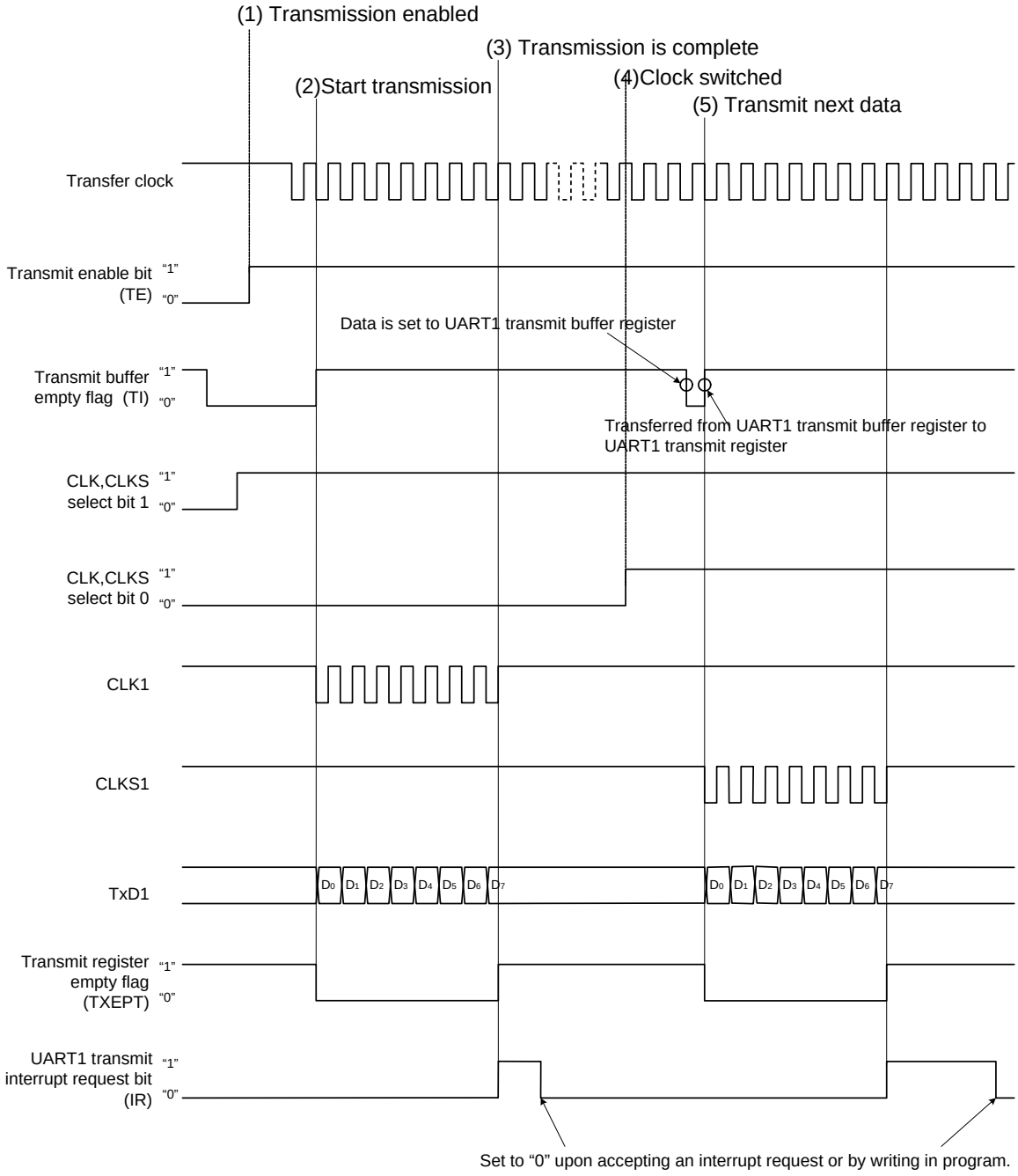
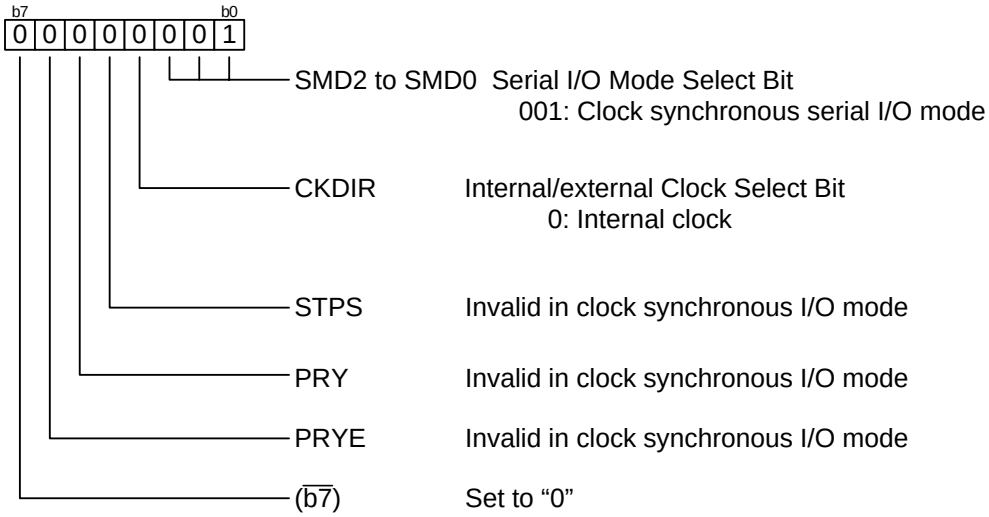


Figure 1. Operation Timing of Transmission in Clock-Synchronous Serial I/O Mode , Transfer Clock Output from Multiple Pins Function Selected

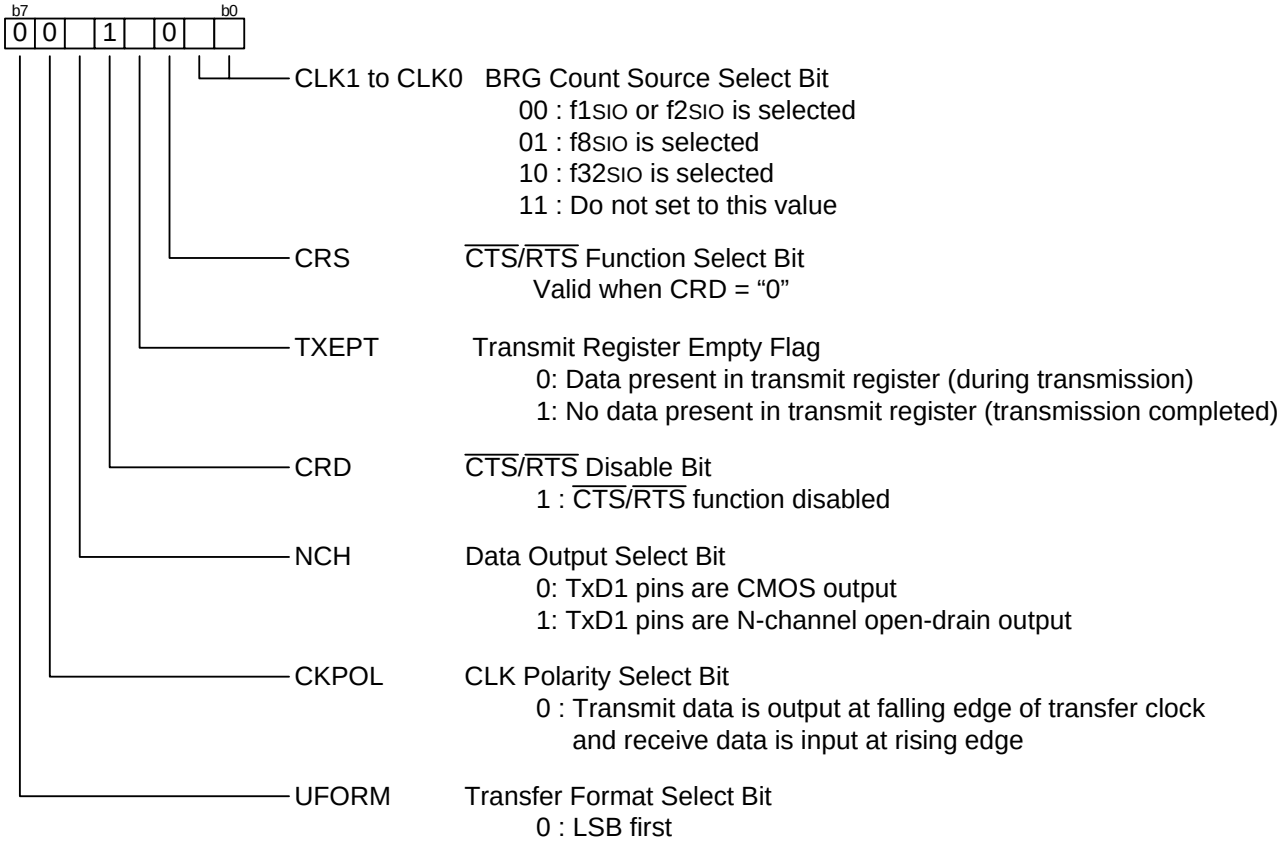
3.1 Register Setting

To enable the operation defined in “Section 3. Operation of timer A”, the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/26 Group hardware manual, M16C/26A Group hardware manual, M16C/28 Group hardware manual, M16C/29 Group hardware manual.

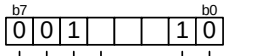
(1) Setting UART1 transmit/receive mode register



(2) Setting UART1 transmit/receive control register 0



(3) Setting UART transmit/receive control register 2



U0IRS — UART0 Transmit Interrupt Cause Select Bit
0 : Transmit buffer empty (TI = 1)

U1IRS — UART1 Transmit Interrupt Cause Select Bit
1 : Transmission completed (TXEPT = 1)

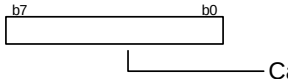
CLKMD0 — UART1 CLK/CLKS select bit 0
0 : Clock output to CLK1
1 : Clock output to CLKS1

CLKMD1 — UART1 CLK/CLKS select bit 1
1 : Transfer clock output from multiple pins function selected

RCSP — Separate UART0 $\overline{CTS}/\overline{RTS}$ Bit
0 : $\overline{CTS}/\overline{RTS}$ shared pin
1 : $\overline{CTS}/\overline{RTS}$ separated ($\overline{CTS}_0$ supplied from the $P6_4$ pin)

($\overline{b7}$) — Set to "0"

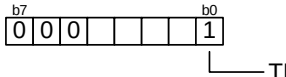
(4) Setting UART1 baud rate generation register



Can be set to 00_{16} to FF_{16} (Note)

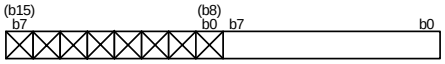
Note: Write to UART1 baud rate generation register when transmission/reception is halted.

(5) Transmission enabled (UART1 transmit/receive control register 1)



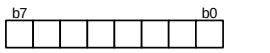
TE — Transmit Enable Bit
1 : Transmission enabled

(6) Writing transmit data (UART1 transmit buffer register



Setting transmission data

(7) Checking the status of UART1 transmit buffer register



TXEPT — Transmit Buffer Empty Flag
0 : Data present in UiTB register
1 : No data present in UiTB register

It returns to (6) when continuously transmitting.

4. Sample Program

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART1                         *
 *             (Clock synchronous serial I/O transfer mode. *
 *              transfer clock output multiple pins function ) *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/***************************
 *   include file          *
 ***************************/
#include "sfr28.h"

/***************************
 *   Function Definition   *
 ***************************/

/***************************
 *   main                  *
 ***************************/
void main(void) {

    unsigned short   trans_data = 0;
    unsigned short   i;

    u1mr = 0x01; /* UART1 transmint/receive mode register setting
                 Clock synchronous serial I/O mode
                 Internal clock select
            */

    u1c0 = 0x10; /* UART1 transmint/receive control register 0 setting
                 ~CTS/~RTS function disabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    ucon = 0x22; /* UART transmint/receive control register 2 setting
             UART1 tansmit interrupt cause is selected to "Transmission completed(TXEPT=1)"
             transfer clock output from multiple pins function selected
             */

    u1brg = 10-1;    /* Setting UART1 bit rate generator (1MHz @20MHz f1) */

    u1c1 = 0x01; /* UART transmint/receive control register 1 setting
                 Transmit enabled
            */

    while (1) {

        u1tb = trans_data;       /* Writing transmit data */

        for ( i=0;i<=20;i++) {   /* Delay loop */
        }            /* wait until txept="0" */

        while (!txept_u1c0) {    /* Check & wait the status of UART1 transmit buffer empty flag */
        }

        clkmd0 = !clkmd0;        /* Clock output pin is exchanged */

        trans_data++;
        trans_data = 0xFF & trans_data;

    }
}
```

5. Reference

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Hardware Manual

M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual
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REVISION HISTORY

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