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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M16C/80 Group

Operation of Serial I/O (reception in UART mode)

1.0 Abstract

In receiving data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosed functions

Item	Set-up	Item	Set-up
Transfer clock source (Note 2)	<input type="radio"/> Internal clock (f1 / f8 / f32)	Data logic select function (Note 3)	<input type="radio"/> No reverse
	<input type="radio"/> External clock (CLKi pin)		<input type="radio"/> Reverse
RTS function	<input type="radio"/> $\overline{\text{RTS}}$ function enabled	Tx/D, Rx/D I/O polarity reverse bit (Note 3)	<input type="radio"/> No reverse
	<input type="radio"/> $\overline{\text{RTS}}$ function disabled		<input type="radio"/> Reverse
CTS / $\overline{\text{RTS}}$ separation function (Note 1)	<input type="radio"/> Pin shared by CTS and $\overline{\text{RTS}}$	Bus collision detection function (Note 3)	<input type="radio"/> Not selected
	<input type="radio"/> CTS and $\overline{\text{RTS}}$ separate		<input type="radio"/> Selected
Sleep mode (Note 2)	<input type="radio"/> Sleep mode off		
	<input type="radio"/> Sleep mode selected		

Note 1: UART0 only. (UART1 CTS/ $\overline{\text{RTS}}$ function cannot be used when this function is selected.)

Note 2: UART0, UART1 only.

Note 3: UART2 to UART4 only.

2.0 Introduction

Operation (1) Setting the receive enable bit to “1” readies data-receivable status. At this time, output from the $\overline{\text{RTSi}}$ pin goes to “L” level to inform the transmission side that the receivable status is ready.

(2) When the first bit (the start bit) of reception data is received from the RxDi pin, output from the $\overline{\text{RTS}}$ goes to “H” level. Then, data is received, bit by bit, in sequence: LSB, ..., MSB, and stop bit(s).

(3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register.

At this time, the receive complete flag goes to “1” to indicate that the reception is completed, the UARTi receive interrupt request bit goes to “1”, and output from the $\overline{\text{RTS}}$ pin goes to “L” level.

(4) The receive complete flag goes to “0” when the lower-order byte of the UARTi buffer register is read.

- Note
- Select $\overline{\text{RTSi}}$ outputs with the function select register A and B.
 - Set RxDi pin's function select register A to I/O port and port direction register to “0”.
 - When setting the function select registers A, B, and C, sets the function select registers B and/or C first, and then sets the function select register A.

Figure 1 shows the operation timing

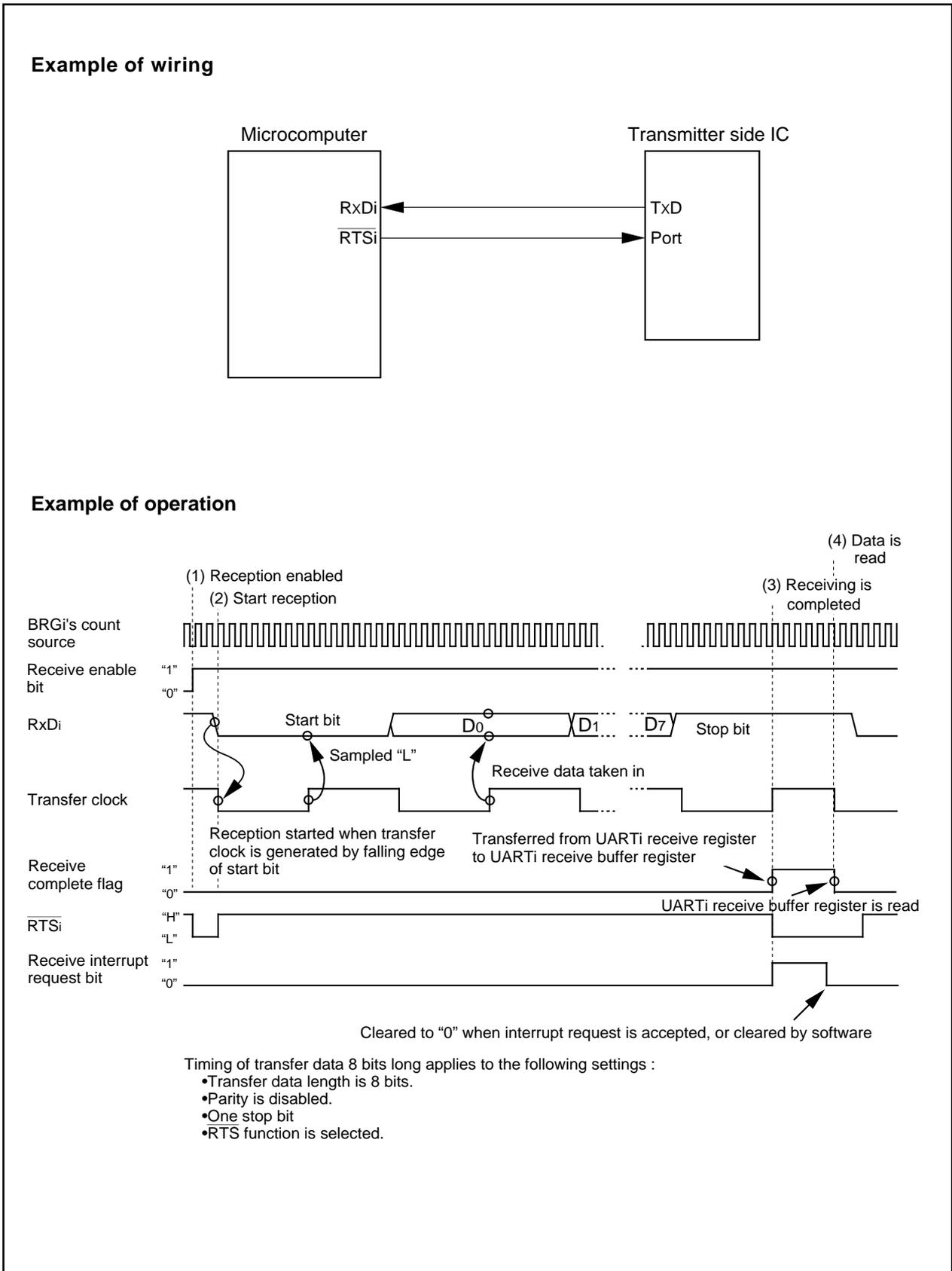


Figure 1. Operation timing of reception in UART mode

3.0 Set-up procedure

Setting UART_i transmit/receive mode register (i=0 to 4)

UART0 transmit/receive mode register
U0MR [Address 0360₁₆]
UART1 transmit/receive mode register
U1MR [Address 0368₁₆]

Serial I/O mode select bit
b₂ b₁ b₀
1 0 1 : Transfer data 8 bits long

Internal/external clock select bit
0 : Internal clock

Stop bit length select bit
0 : One stop bit

Valid when bit 6 = "1"

Parity enable bit
0 : Parity disabled

Sleep select bit
0 : Sleep mode deselected

UART2 transmit/receive mode register
U2MR [Address 0338₁₆]
UART3 transmit/receive mode register
U3MR [Address 0328₁₆]
UART4 transmit/receive mode register
U4MR [Address 02F8₁₆]

Serial I/O mode select bit
b₂ b₁ b₀
1 0 1 : Transfer data 8 bits long

Internal/external clock select bit
0 : Internal clock

Stop bit length select bit
0 : One stop bit

Valid when bit 6 = "1"

Parity enable bit
0 : Parity disabled

TXD, RXD I/O polarity reverse bit
Usually set to "0"

Setting UART_i transmit/receive control register (i=0 to 4)

UART0 transmit/receive control register 0
U0C0 [Address 0364₁₆]
UART1 transmit/receive control register 0
U1C0 [Address 036C₁₆]

BRG count source select bit
b₁ b₀
0 0 : f₁ is selected
0 1 : f₈ is selected
1 0 : f₃₂ is selected
1 1 : Inhibited

CTS/RTS function select bit
(Valid when bit 4 = "0")
1 : RTS function is selected (Note)

Transmit register empty flag
0 : Data present in transmit register
(during transmission)
1 : No data present in transmit register
(transmission completed)

CTS/RTS disable bit
0 : CTS/RTS function enabled

Data output select bit
0 : TxDi pin is CMOS output
1 : TxDi pin is N-channel open-drain output

Must be fixed to "0" in UART mode
Must be fixed to "0" in UART mode

UART2 transmit/receive control register 0
U2C0 [Address 033C₁₆]

BRG count source select bit
b₁ b₀
0 0 : f₁ is selected
0 1 : f₈ is selected
1 0 : f₃₂ is selected
1 1 : Inhibited

CTS/RTS function select bit
(Valid when bit 4 = "0")
1 : RTS function is selected (Note)

Transmit register empty flag
0 : Data present in transmit register
(during transmission)
1 : No data present in transmit register
(transmission completed)

CTS/RTS disable bit
0 : CTS/RTS function enabled

Transfer format select bit
0 : LSB first

Note: Select $\overline{\text{RTS}}$ output with the corresponding function select registers A and B.

Setting UART transmit/receive control register 2 and UART_i transmit/receive control register 1 (i=2 to 4)

UART transmit/receive control register 2
UCON [Address 0370₁₆]

Invalid in UART mode

Invalid in UART mode

Separate $\overline{\text{CTS/RTS}}$ bit
0 : CTS/RTS shared pin

UART2 transmit/receive control register 1
U2C1 [Address 033D₁₆]
UART3 transmit/receive control register 1
U3C1 [Address 032D₁₆]
UART4 transmit/receive control register 1
U4C1 [Address 02FD₁₆]

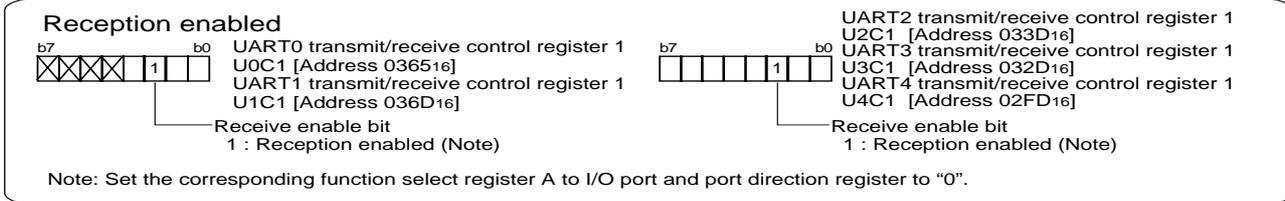
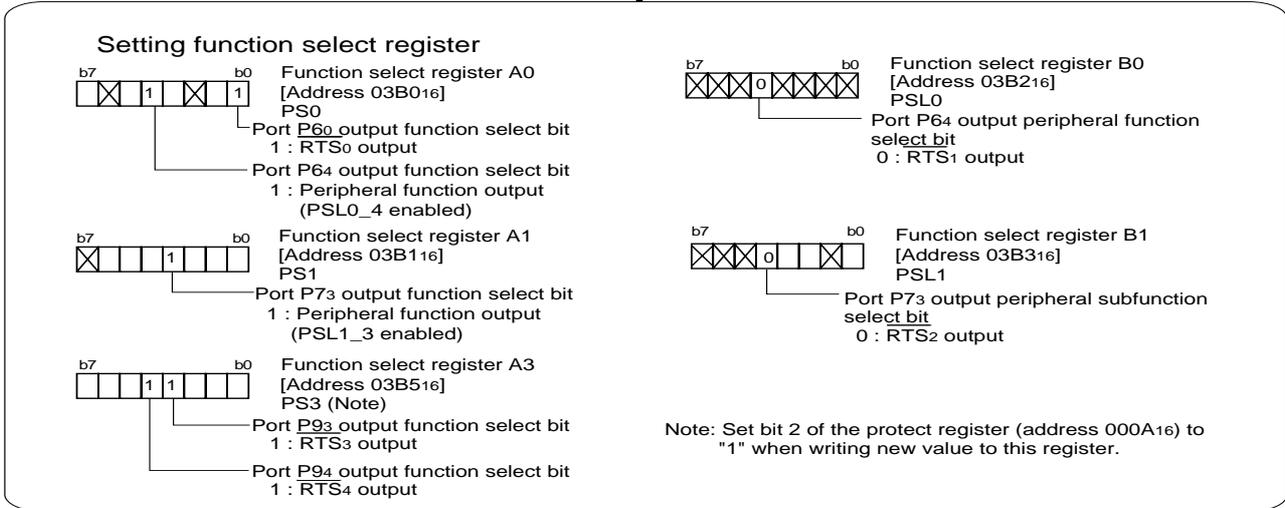
Invalid in UART mode

Data logic select bit
0 : No reverse

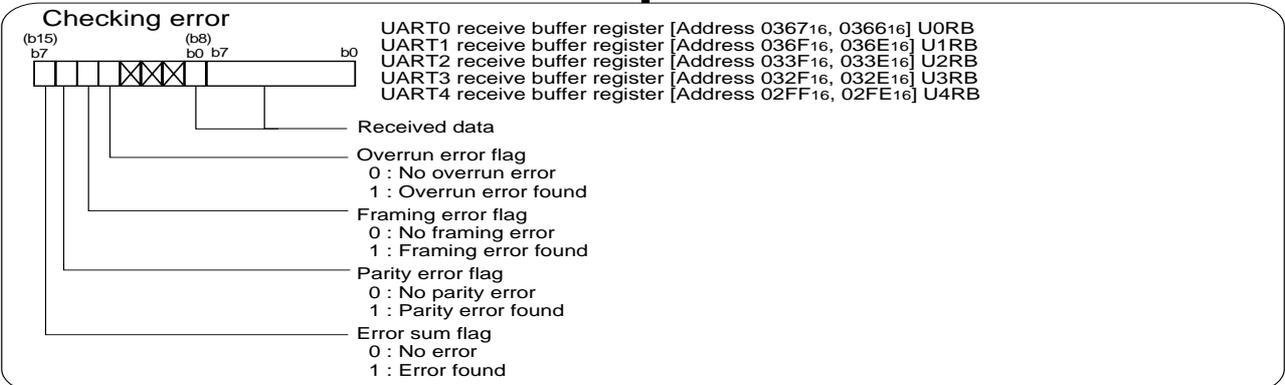
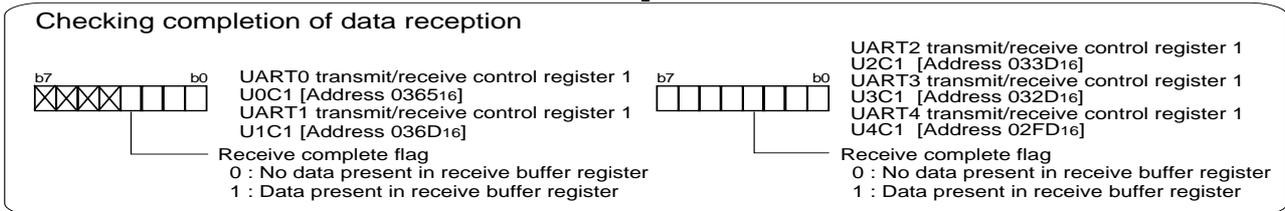
Error signal output enable bit
0 : Output disabled

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Start reception



Processing after reading out received data


```

=====
;      Serial I/O (reception in UART mode)
=====
;      Setting UART0 transmit/receive mode register
MOV.B   #00000101B, u0mr
;      ||| | | | ++-----;Serial I/O mode select bit (101:Transfer data 8 bits long)
;      ||| | | | +-----;Internal/external clock select bit (0:Internal clock)
;      ||| | | | +-----;Stop bit length select bit (0:One stop bit)
;      || +-----;Valid when bit 6="1"
;      |+-----;Parity enable bit (0:Parity disabled)
;      +-----;Sleep select bit (0:Sleep mode deselected)
;      Setting UART0 transmit/receive control register 0
MOV.B   #00001100B, u0c0
;      ||| | | | ++-----;BRG count source select bit (00:f1 is selected)
;      ||| | | | +-----;RTS function is selected (Valid when bit 4="0") (Note)
;      ||| | | | +-----;Transmit register empty flag (Written value is invalid)
;      ||| +-----;CTS/RTS disable bit (0:CTS/RTS function enabled)
;      || +-----;Data output select bit (0:TxDi pin is CMOS output)
;      ++-----;Must be fixed to "0" in UART mode
;      Setting UART transmit/receive control register 2
MOV.B   #00000000B, ucon
;      ||| | | | ++-----;Invalid in UART mode
;      || +-----;Nothing is assigned
;      |+-----;Separate CTS/RTS bit (0:CTS/RTS shared pin)
;      +-----;Nothing is assigned
;      Setting function select register
;      (Note) Select RTS output with the corresponding function select register A and B
BSET    ps0_0          ;RTS0[P60] output
;      (Note) Set the corresponding function select register A to I/O port
;      and port direction register to "0"
BCLR    pd6_2          ; RxD0[P62] is input direction
;      Setting UART0 bit rate generator
MOV.B   #129, u0brg    ;(Approx. 9600bps : fi/16(129+1) @20MHz,f1)
;      ;(Note) Write to UARTi bit rate generator when
;      ;      transmission/reception is halted

;      Reception enabled
MOV.B   #00000100B, u0c1
;      +-----;Receive enable bit (1:Reception enabled) (Note)
;
=====
;      Main program
=====
WAIT_RECEIVE:
;      Checking completion of data reception
BTST    ri_u0c1
JNC     WAIT_RECEIVE
;
CHK_ERR:
;      Reading out error information and received data to R0 register
;      (ex)
MOV.W   u0rb, R0
;      Check error (ex. Check error sum flag)
BTST    7, R0H
JC      ERR_REC
;
;      No error
;      Processing after reading out reception data
JMP     WAIT_RECEIVE

=====
;      Error found
=====
ERR_REC:
NOP
JMP     ERR_REC
;

```

```

;=====
;      Dummy interrupt processing program
;=====
dummy:
    REIT
;
;*****
;      Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD     dummy    ;Undefined instruction
    .LWORD     dummy    ;Overflow
    .LWORD     dummy    ;BRK instruction execution
    .LWORD     dummy    ;Address match
    .LWORD     dummy    ;
    .LWORD     dummy    ;Watchdog timer
    .LWORD     dummy    ;
    .LWORD     dummy    ;NMI
    .LWORD     RESET    ;Reset
;
    .END

```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

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Data Sheet

M16C/80 group Rev. E3

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