

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## M16C/62A Group

### Operation of Serial I/O (reception in UART mode)

#### 1.0 Abstract

In receiving data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

**Table 1. Chosed functions**

Item	Set-up		Item	Set-up	
Transfer clock source (Note 1)	<input type="radio"/>	Internal clock (f1 / f8 / f32)	Data logic select function (Note 2)	<input type="radio"/>	No reverse
		External clock (CLKi pin)			Reverse
RTS function	<input type="radio"/>	RTS function enabled	Tx/D, Rx/D I/O polarity reverse bit (Note 2)	<input type="radio"/>	No reverse
		RTS function disabled			Reverse
Sleep mode (Note 1)	<input type="radio"/>	Sleep mode off	Bus collision detection function (Note 2)	<input type="radio"/>	Not selected
		Sleep mode selected			Selected

**Note 1: UART0, UART1 only.**

**Note 2: UART2 only.**

#### 2.0 Introduction

Operation (1) Setting the receive enable bit to "1" readies data-receivable status. At this time, output from the  $\overline{\text{RTSi}}$  pin goes to "L" level to inform the transmission side that the receivable status is ready.

(2) When the first bit (the start bit) of reception data is received from the RxDi pin, output from the  $\overline{\text{RTS}}$  goes to "H" level. Then, data is received, bit by bit, in sequence: LSB, ..., MSB, and stop bit(s).

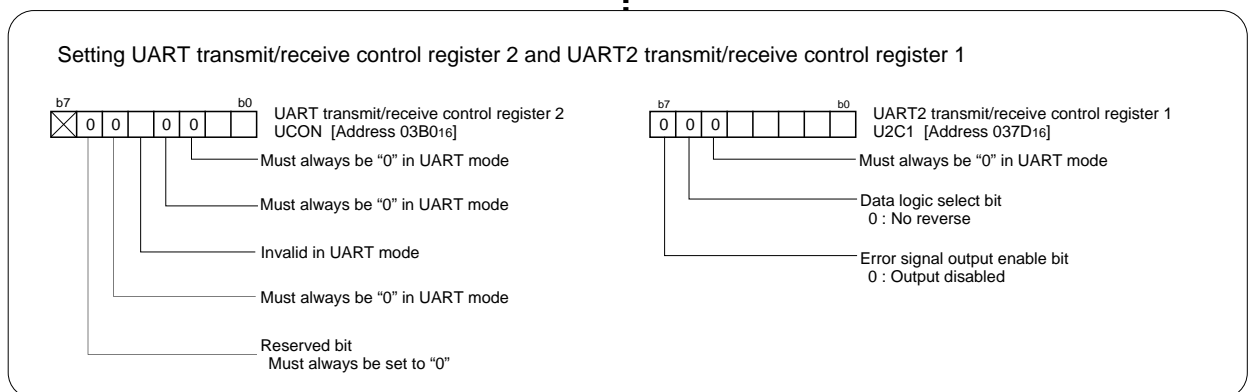
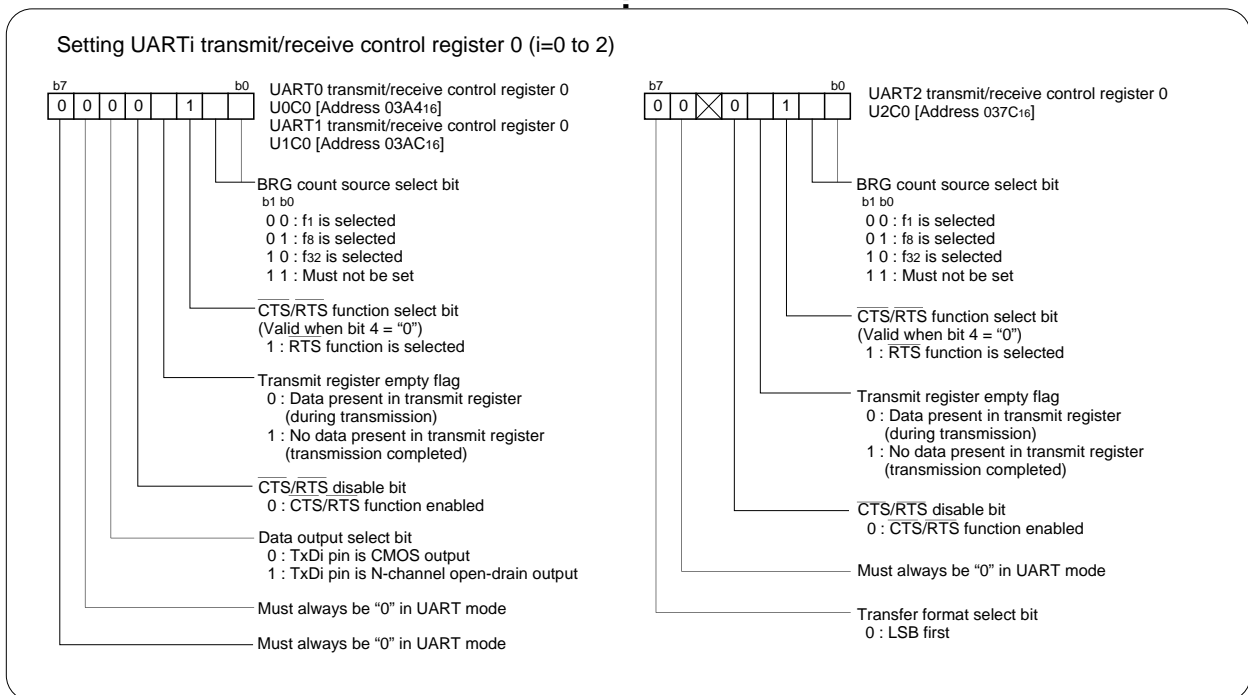
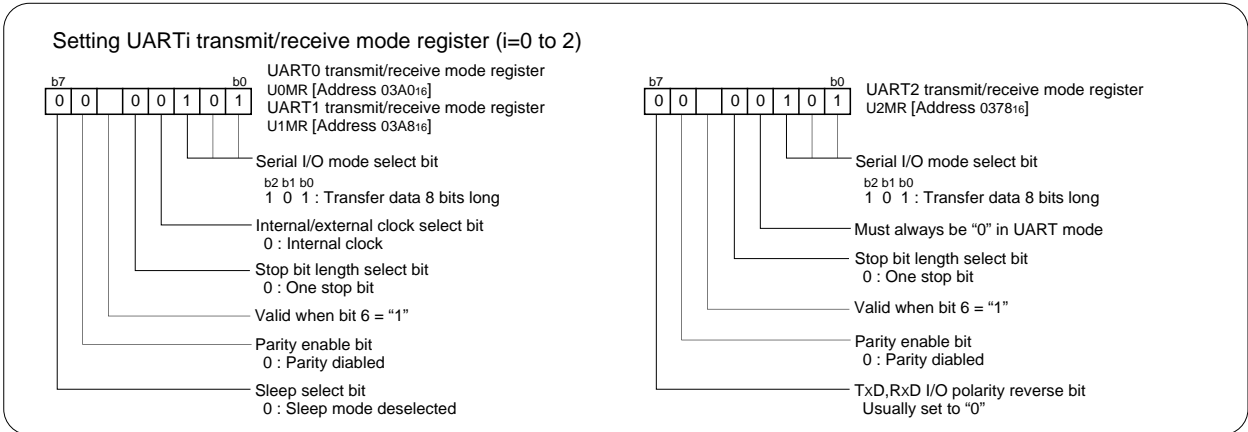
(3) When the stop bit(s) is (are) received, the content of the UARTi receive register is transmitted to the UARTi receive buffer register.

At this time, the receive complete flag goes to "1" to indicate that the reception is completed, the UARTi receive interrupt request bit goes to "1", and output from the  $\overline{\text{RTS}}$  pin goes to "H" level.

(4) The receive complete flag goes to "0" when the lower-order byte of the UARTi buffer register is read.



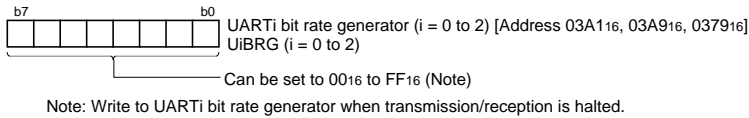
### 3.0 Set-up procedure



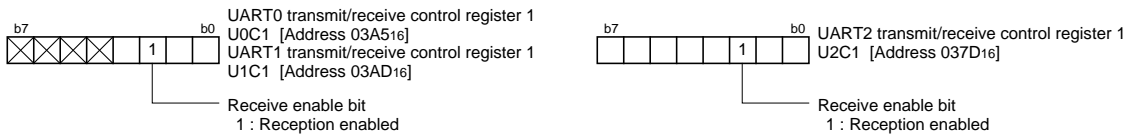
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### Setting UARTi bit rate generator (i = 0 to 2)

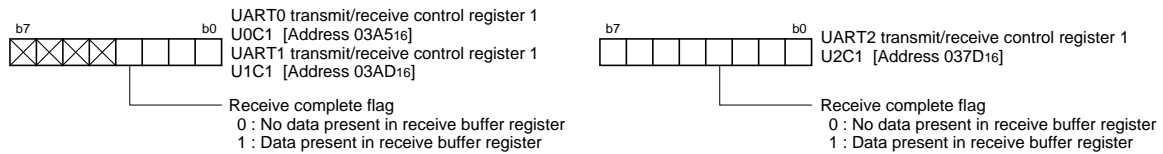


### Reception enabled

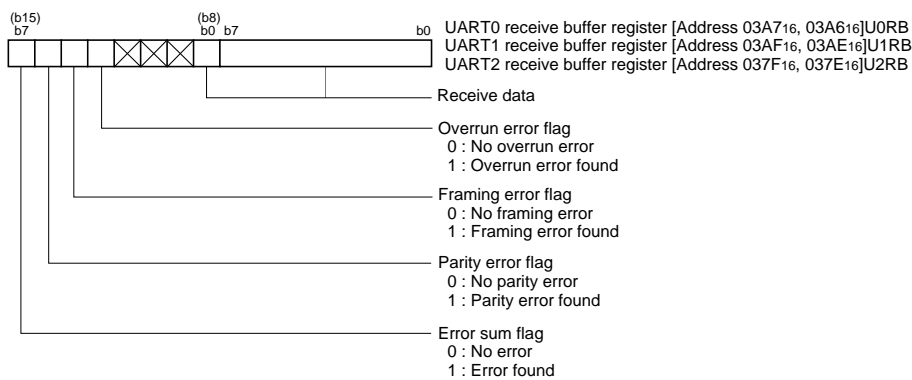


Start reception

### Checking completion of reception



### Checking error



Processing after reading out reception data



```

=====
;
;   Serial I/O (reception in UART mode)
;
=====
MOV.B   #00000101B, u0mr   ;Setting UART0 transmit/receive mode register
;
;   ||| | | | ++-----;Serial I/O mode select bit (101:Transfer data 8 bits long)
;   ||| | | | +-----;Internal/external clock select bit (0:Internal clock)
;   ||| | | | +-----;Stop bit length select bit (0:One stop bit)
;   ||| | | | +-----;Valid when bit 6="1"
;   ||| | | | +-----;Parity enable bit (0:Parity disabled)
;   +-----;Sleep select bit (0:Sleep mode deselected)
MOV.B   #00001100B, u0c0   ;Setting UART0 transmit/receive control register 0
;
;   ||| | | | ++-----;BRG count source select bit (00:f1 is selected)
;   ||| | | | +-----;RTS function is selected (Valid when bit 4="0")
;   ||| | | | +-----;Transmit register empty flag (Write disable)
;   ||| | | | +-----;CTS/RTS disable bit (0:CTS/RTS function enabled)
;   ||| | | | +-----;Data output select bit (0:TxDi pin is CMOS output)
;   +-----;Must always be "0" in UART mode
MOV.B   #00000000B, ucon   ;Setting UART transmit/receive control register 2
;
;   ||| | | | ++-----;Must always be "0" in UART mode
;   ||| | | | +-----;Invalid in UART mode
;   ||| | | | +-----;Must always be "0" in UART mode
;   +-----;Reserved bit (Must always be set to "0")
MOV.B   #103, u0brg       ;Setting UART0 bit rate generator (Approx. 9600bps @16MHz,f1)
MOV.B   #00000100B, u0c1   ;Reception enabled
;
;   +-----;Receive enable bit (1:Reception enabled)
;
=====
;
;   Main program
;
=====
WAIT_RECEIVE:
    BTST    ri_u0c1           ;Checking completion of reception
    JNC     WAIT_RECEIVE
;
CHK_ERR:
;   ; Reading out error information and received data to R0 register
;   ; (ex)
MOV.W    u0rb, R0
;   ; Check error (ex. Check error sum flag)
BTST    15, R0
JC      ERR_REC
;
;   ; No error
;   ; Processing after reading out reception data
JMP     WAIT_RECEIVE

=====
;
;   Error found
;
=====
ERR_REC:
    NOP
    JMP     ERR_REC
;

```



```

;=====
;      Dummy interrupt processing program
;=====
dummy:
    REIT
;
;*****
;      Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD     dummy    ;Undefined instruction interrupt vector
    .LWORD     dummy    ;Overflow (INT0 instruction) interrupt vector
    .LWORD     dummy    ;BRK instruction interrupt vector
    .LWORD     dummy    ;Address match interrupt vector
    .LWORD     dummy    ;Single-step interrupt vector
    .LWORD     dummy    ;Watchdog timer interrupt vector
    .LWORD     dummy    ;DBC interrupt vector
    .LWORD     dummy    ;NMI interrupt vector
    .LWORD     RESET    ;Sets reset vector
;
    .END

```

**5.0 Reference**

**Renesas Technology Corporation Semiconductor Home page**  
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**Technical Support**

E-mail: [support\\_apl@renesas.com](mailto:support_apl@renesas.com)

**Data Sheet**

M16C/62A group Rev. C.1  
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**User's Manual**

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