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Renesas Electronics Corporation

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## M16C/64 Group

### Operation of serial I/O (reception in clock-synchronous serial I/O mode)

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#### 1. Abstract

In receiving data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

#### 2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

### 3. Chosen functions

**Table 1. Chosen functions**

Item	Set-up		Item	Set-up	
Transfer clock source		Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	Continuous receive mode	<input type="radio"/>	Disabled
	<input type="radio"/>	External clock (CLKi pin)			Enabled
RTS function	<input type="radio"/>	RTS function enabled	Output transfer clock to multiple pins (Note 1)	<input type="radio"/>	Not selected
		RTS function disable			Selected
CLK polarity	<input type="radio"/>	Input reception data at the rising edge of the transfer clock	Data logic select function	<input type="radio"/>	No reverse
		Input reception data at the falling edge of the transfer clock			Reverse
Transfer clock	<input type="radio"/>	LSB first	TxD, RxD I/O polarity reverse bit	<input type="radio"/>	No reverse
		MSB first			Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1  $\overline{\text{CTS}}$  /  $\overline{\text{RTS}}$  function can not be utilized. Set the UART1  $\overline{\text{CTS}}$  /  $\overline{\text{RTS}}$  disable bit to "1".

### 4. Operation

(1) Writing dummy data to the UARTi transmit buffer register, setting the receive enable bit to "1", and the transmit enable bit to "1", makes the data receivable status ready. At this time, the output from the RTSi pin goes to "L" level, which informs the transmission side that the data receivable status is ready (output the transfer clock from the IC on the transmission side after checking that the RTS output has gone to "L" level).

(2) In synchronization with the first rising edge of the transfer clock, the input signal to the RxDi pin is stored in the highest bit of the UARTi receive register. Then, data is taken in by shifting right the content of the UARTi reception data in synchronization with the rising edges of the transfer clock.

(3) When 1-byte data lines up in the UARTi receive register, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. The transfer clock stops at "H" level. At this time, the receive complete flag and the UARTi receive interrupt request bit goes to "1".

(4) The receive complete flag goes to "0" when the lower-order byte of the UARTi buffer register is read.

### (reception in clock-synchronous serial I/O mode)

Figure 1 shows the operation timing.

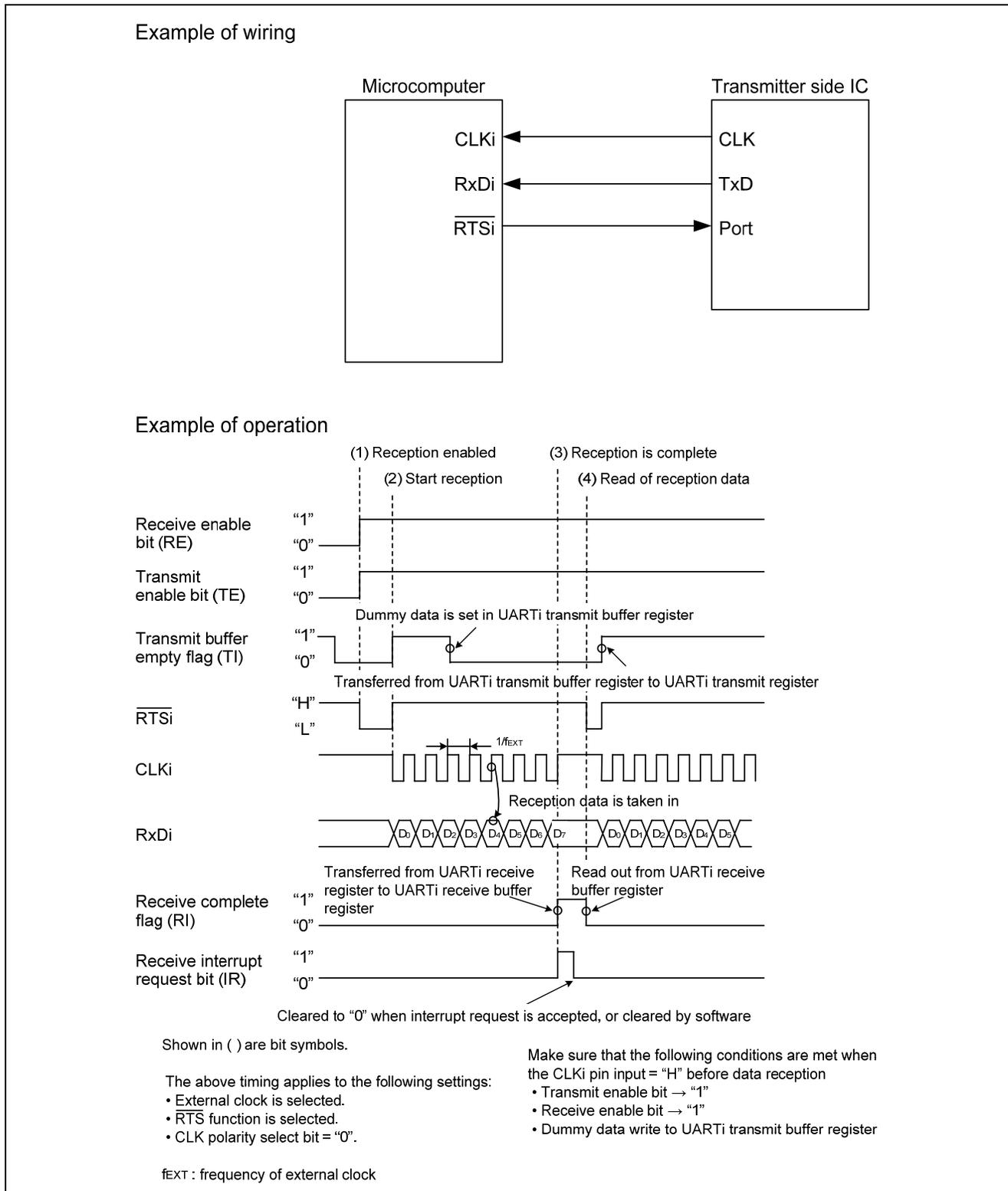
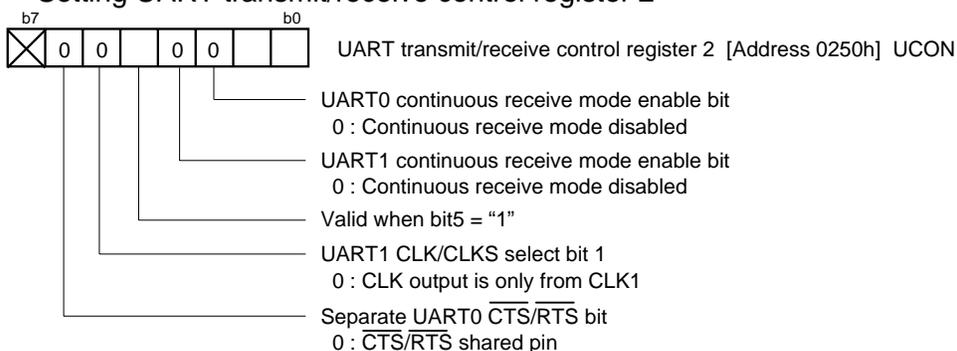


Figure 1. Operation timing of reception in clock-synchronous serial I/O mode

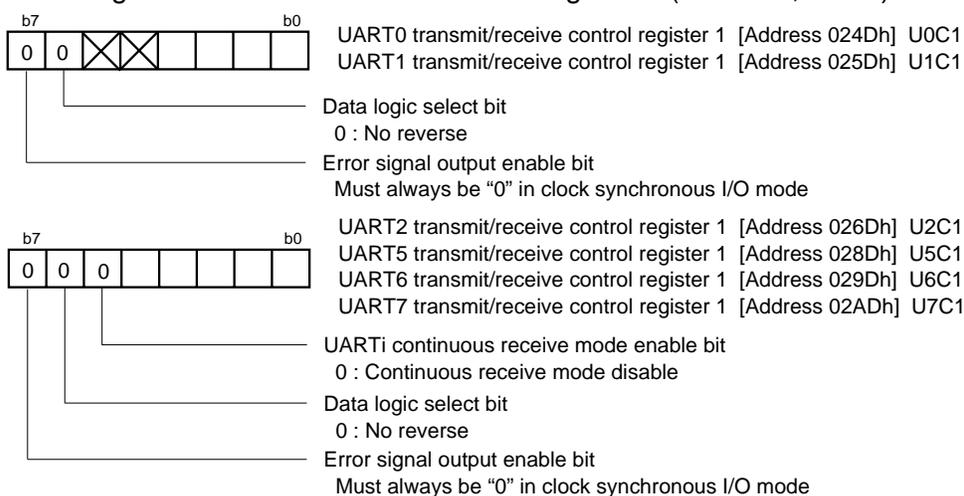


### (reception in clock-synchronous serial I/O mode)

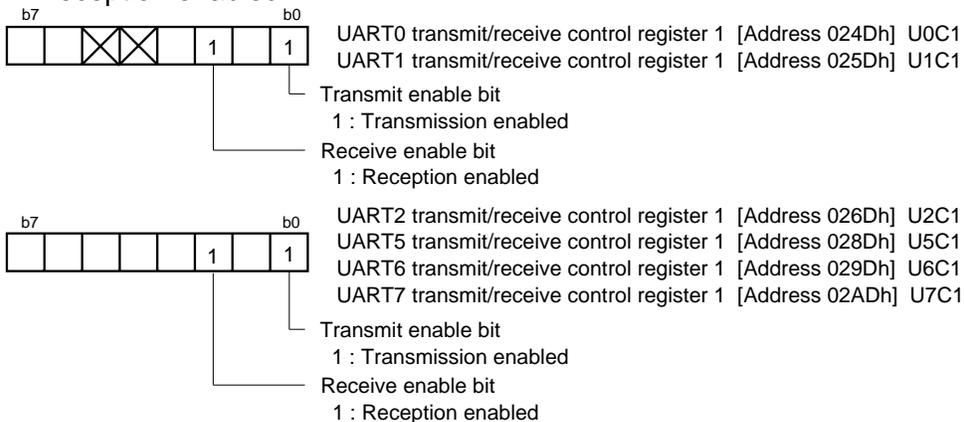
#### Setting UART transmit/receive control register 2



#### Setting UARTi transmit/receive control register 1 (i = 0 to 2, 5 to 7)

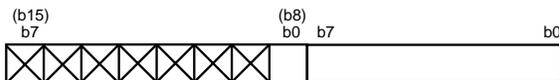


#### Reception enabled



### (reception in clock-synchronous serial I/O mode)

#### Writing dummy data



UART0 transmit buffer register [Address 024Bh, 024Ah] U0TB  
 UART1 transmit buffer register [Address 025Bh, 025Ah] U1TB  
 UART2 transmit buffer register [Address 026Bh, 026Ah] U2TB  
 UART5 transmit buffer register [Address 028Bh, 028Ah] U5TB  
 UART6 transmit buffer register [Address 029Bh, 029Ah] U6TB  
 UART7 transmit buffer register [Address 02ABh, 02AAh] U7TB

Setting dummy data

#### Start reception

#### Checking completion of reception



UART0 transmit/receive control register 1 [Address 024Dh] U0C1  
 UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Receive complete flag

0 : No data present in receive buffer register  
 1 : Data present in receive buffer register

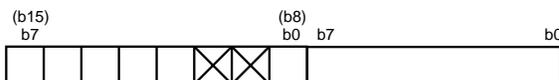


UART2 transmit/receive control register 1 [Address 026Dh] U2C1  
 UART5 transmit/receive control register 1 [Address 028Dh] U5C1  
 UART6 transmit/receive control register 1 [Address 029Dh] U6C1  
 UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Receive complete flag

0 : No data present in receive buffer register  
 1 : Data present in receive buffer register

#### Checking error



UART0 receive buffer register [Address 024Fh, 024Eh] U0RB  
 UART1 receive buffer register [Address 025Fh, 025Eh] U1RB  
 UART2 receive buffer register [Address 026Fh, 026Eh] U2RB  
 UART5 receive buffer register [Address 028Fh, 028Eh] U5RB  
 UART6 receive buffer register [Address 029Fh, 029Eh] U6RB  
 UART7 receive buffer register [Address 02AFh, 02AEh] U7RB

Receive data

Overrun error flag

0 : No overrun error  
 1 : Overrun error found

#### Processing after reading out reception data

## 6. Reference

### Hardware manual

M16C/64 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

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**Revision**

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		Page	Point
1.00	2008.06	-	First edition issued

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