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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M16C/80 Group

Operation of DMAC (repeated transfer mode)

1.0 Abstract

In repeated transfer mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosed functions

Item	Set-up	
Transfer space		Fixed address from an arbitrary 16 M bytes space
	○	Arbitrary 16 M bytes space from a fixed address
Unit of transfer		8 bits
	○	16 bits

2.0 Introduction

- Operation
- (1) When software trigger is selected, setting software DMA request bit and DMA request bit to “1” simultaneously generates a DMA transfer request signal.
 - (2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi SFR address register are transferred to the address indicated by the DMAi memory address register. Each time a DMA transfer request signal is generated, 2 bytes of data (1 data) is transferred. The DMAi transfer count register is down counted, and the DMAi memory address register is up counted.
 - (3) If the DMAi transfer counter shifts from 0001₁₆ to 0000₁₆, the DMAi interrupt request bit changes to “1”.
 - (4) When the DMAi transfer count register shifts from 0001₁₆ to 0000₁₆, the value of DMAi memory address reload register is reloaded into the DMAi memory address register and the value of DMAi transfer count reload register is reloaded into the DMAi transfer count register. After that, DMA transfer is repeated from (1).

Figure 1 shows example of operation of repeated transfer mode.

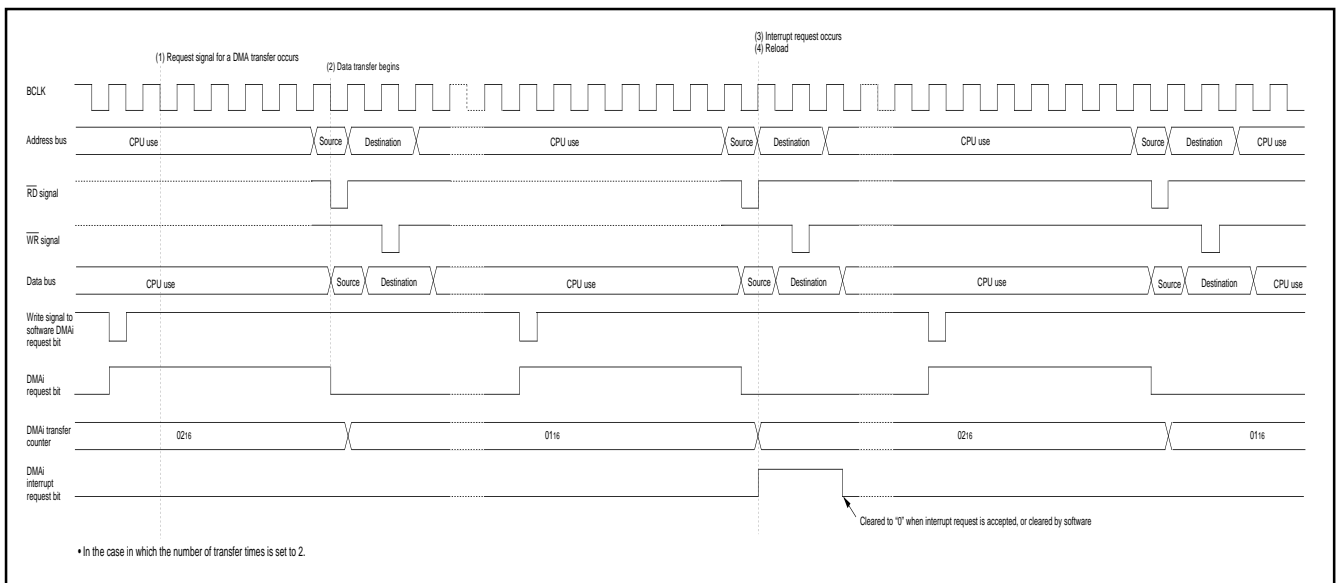


Figure 1. Example of operation of repeated transfer mode

3.0 Set-up procedure

Selecting DMA_i request cause select register

DMA_i request cause select register (i=0 to 3) [Address 0378₁₆ to 037B₁₆]
 DMA_iSL (i=0 to 3)
 DMA request cause select bit
 b_{4b3b2b1}
 0 0 0 0 : Software trigger
 Software DMA request bit
 Set to "0"
 DMA request bit
 Set to "1"

(Note) When changing DMA request cause select bit, set "1" to the DMA request bit, simultaneously. In this case, the corresponding DMA channel is set to disabled.

Setting DMA_i memory address register (i=0 to 3)

DMA0 memory address register [CPU internal register] DMA0
 DMA1 memory address register [CPU internal register] DMA1
 DMA2 memory address register [CPU internal register] DMA2 (Bank 1 A0)
 DMA3 memory address register [CPU internal register] DMA3 (Bank 1 A1)

Store a memory address at the destination of DMA transfer

Setting DMA_i memory address reload register (i=0 to 3)

DMA0 memory address reload register [CPU internal register] DRA0
 DMA1 memory address reload register [CPU internal register] DRA1 (SVP)
 DMA2 memory address reload register [CPU internal register] DRA2 (SVP)
 DMA3 memory address reload register [CPU internal register] DRA3 (VCT)

Store a reloaded memory address at the destination of DMA transfer

Setting DMA_i SFR address register (i=0 to 3)

DMA0 SFR address register [CPU internal register] DSA0
 DMA1 SFR address register [CPU internal register] DSA1 (Bank 1 SB)
 DMA2 SFR address register [CPU internal register] DSA2 (Bank 1 SB)
 DMA3 SFR address register [CPU internal register] DSA3 (Bank 1 SB)

Store a memory address at the source of DMA transfer

Setting DMA_i transfer count register (i=0 to 3)

DMA0 transfer count register [CPU internal register] DCT0
 DMA1 transfer count register [CPU internal register] DCT1
 DMA2 transfer count register [CPU internal register] DCT2 (Bank 1 R0)
 DMA3 transfer count register [CPU internal register] DCT3 (Bank 1 R1)

Transfer counter
 Set a value of transfer number

Setting DMA_i transfer count reload register (i=0 to 3)

DMA0 transfer count reload register [CPU internal register] DRC0
 DMA1 transfer count reload register [CPU internal register] DRC1
 DMA2 transfer count reload register [CPU internal register] DRC2 (Bank 1 R2)
 DMA3 transfer count reload register [CPU internal register] DRC3 (Bank 1 R3)

Reload value of transfer counter
 Set a value of transfer number

Selecting DMA mode register i (i=1,0)

DMA mode register 0 [CPU internal register] DMD0
 Channel 0 transfer mode select bit
 1 1 : Repeat transfer
 Channel 0 transfer unit select bit
 1 : 16 bits
 Channel 0 transfer direction select bit
 0 : Fixed address to Memory
 Channel 1 transfer mode select bit
 1 1 : Repeat transfer
 Channel 1 transfer unit select bit
 1 : 16 bits
 Channel 1 transfer direction select bit
 0 : Fixed address to Memory

DMA mode register 1 [CPU internal register] DMD1
 Channel 2 transfer mode select bit
 1 1 : Repeat transfer
 Channel 2 transfer unit select bit
 1 : 16 bits
 Channel 2 transfer direction select bit
 0 : Fixed address to Memory
 Channel 3 transfer mode select bit
 1 1 : Repeat transfer
 Channel 3 transfer unit select bit
 1 : 16 bits
 Channel 3 transfer direction select bit
 0 : Fixed address to Memory

When software DMA request bit and DMA request bit = "1" simultaneously
 Start DMA transmission


```

=====
;      DMAC (repeated transfer mode)
=====
MOV.W   #055AAH, v_Src_DMA   ;Setting DMA transmit data
;
; Disable DMA0
STC     dmd0, R0             ;Read DMA mode register
AND.B   #11111100B, R0L
;
;          ++-----;Channel 0 transfer mode select bit (00:DMA0 inhibit)
LDC     R0, dmd0            ;Disable DMA0
; Setting DMA0 request cause select register
MOV.B   #10000000B, dm0s1
;
;   | |++++-----;DMA request cause select bit (00000:Software trigger)
;   | |-----;Software DMA request bit (Set to 0)
;   | |-----;DMA request bit (Set to 1)
; Setting DMA0 memory address register (Setting destination memory address)
;                               ;When the transfer direction is "fixed address to memory",
;                               ;this register is destination memory address.
LDC     #(v_Dst_DMA & 0FFFFFFh), dma0
; Setting DMA0 memory address reload register
LDC     #(v_Dst_DMA & 0FFFFFFh), dra0
; Setting DMA0 SFR address register (Setting source fixed address)
;                               ;When the transfer direction is "fixed address to memory",
;                               ;this register is source fixed address.
LDC     #(v_Src_DMA & 0FFFFFFh), dsa0
; Setting DMA0 transfer count register
LDC     #(C_CNT_DMA & 0FFFFh), dct0
; Setting DMA0 transfer count reload register
LDC     #(C_CNT_DMA & 0FFFFh), drc0
; Selecting DMA mode register
OR.B    #00000111B, R0L
;
;   |||||++-----;Channel 0 transfer mode select bit (11:Repeat transfer)
;   |||||
;   |||||+-----;Channel 0 transfer unit select bit (1:16bits)
;   |||||+-----;Channel 0 transfer direction select bit (0:Fixed address to Memory)
;   ||++-----;Channel 1 transfer mode select bit
;   |+-----;Channel 1 transfer unit select bit
;   +-----;Channel 1 transfer mode select bit
; Dummy cycles 8+6N (N is the number of other DMA channels that may generate a DMA request)
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
LDC     R0, dmd0            ;Enable DMA0
;
; Start DMA transmission
; Write software DMA request bit and DMA request bit = "1" simultaneously
OR.B    #0A0H, dm0s1
;
MAIN:
JMP     MAIN
;
=====
;      Dummy interrupt processing program
=====
dummy:
REIT
;

```

```

;*****
;      Setting of fixed vector
;*****
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD     dummy    ;Undefined instruction
        .LWORD     dummy    ;Overflow
        .LWORD     dummy    ;BRK instruction execution
        .LWORD     dummy    ;Address match
        .LWORD     dummy    ;
        .LWORD     dummy    ;Watchdog timer
        .LWORD     dummy    ;
        .LWORD     dummy    ;NMI
        .LWORD     RESET    ;Reset
;
        .END
  
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page
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Data Sheet

M16C/80 group Rev. E3
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