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Renesas Electronics website: http://www.renesas.com

April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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1.0 Abstract

In repeated transfer mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosseed functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer space</td>
<td>Fixed address from an arbitrary 16 M bytes space</td>
</tr>
<tr>
<td></td>
<td>Arbitrary 16 M bytes space from a fixed address</td>
</tr>
<tr>
<td>Unit of transfer</td>
<td>8 bits</td>
</tr>
<tr>
<td></td>
<td>16 bits</td>
</tr>
</tbody>
</table>

2.0 Introduction

Operation
(1) When software trigger is selected, setting software DMA request bit and DMA request bit to “1” simultaneously generates a DMA transfer request signal.

(2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi SFR address register are transferred to the address indicated by the DMAi memory address register. Each time a DMA transfer request signal is generated, 2 bytes of data (1 data) is transferred. The DMAi transfer count register is down counted, and the DMAi memory address register is up counted.

(3) If the DMAi transfer counter shifts from \(0001_{16}\) to \(0000_{16}\), the DMAi interrupt request bit changes to “1”.

(4) When the DMAi transfer count register shifts from \(0001_{16}\) to \(0000_{16}\), the value of DMAi memory address reload register is reloaded into the DMAi memory address register and the value of DMAi transfer count reload register is reloaded into the DMAi transfer count register. After that, DMA transfer is repeated from (1).

Figure 1 shows example of operation of repeated transfer mode.
3.0 Set-up procedure

**Selecting DMAi request cause select register**

<table>
<thead>
<tr>
<th>DMA request cause select bit</th>
<th>b4b3b2b1</th>
<th>DMA request bit</th>
<th>Set to “1”</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 : Software trigger</td>
<td></td>
<td>Software DMA request bit</td>
<td>Set to “0”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DMA request bit</td>
<td>Set to “1”</td>
</tr>
</tbody>
</table>

(Note) When changing DMA request cause select bit, set “1” to the DMA request bit, simultaneously. In this case, the corresponding DMA channel is set to disabled.

**Setting DMAi memory address register (i=0 to 3)**

<table>
<thead>
<tr>
<th>DMA0 memory address register</th>
<th>DMA1 memory address register</th>
<th>DMA2 memory address register</th>
<th>DMA3 memory address register</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
</tr>
<tr>
<td>DMAM0</td>
<td>DMAM1</td>
<td>DMAM2</td>
<td>DMAM3</td>
</tr>
<tr>
<td>(Bank 1 A0)</td>
<td>(Bank 1 A1)</td>
<td>(Bank 1 A0)</td>
<td>(Bank 1 A1)</td>
</tr>
</tbody>
</table>

Store a memory address at the destination of DMA transfer

**Setting DMAi memory address reload register (i=0 to 3)**

<table>
<thead>
<tr>
<th>DMA0 memory address reload register</th>
<th>DMA1 memory address reload register</th>
<th>DMA2 memory address reload register</th>
<th>DMA3 memory address reload register</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CPU internal register] DRA0</td>
<td>[CPU internal register] DRA1</td>
<td>[CPU internal register] DRA2</td>
<td>[CPU internal register] DRA3</td>
</tr>
<tr>
<td>SVP</td>
<td>(Bank 1 A0)</td>
<td>(Bank 1 A0)</td>
<td>(Bank 1 A1)</td>
</tr>
</tbody>
</table>

Store a reloaded memory address at the destination of DMA transfer

**Setting DMAi SFR address register (i=0 to 3)**

<table>
<thead>
<tr>
<th>DMA0 SFR address register</th>
<th>DMA1 SFR address register</th>
<th>DMA2 SFR address register</th>
<th>DMA3 SFR address register</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
</tr>
<tr>
<td>DMAS0</td>
<td>DMAS1</td>
<td>DMAS2</td>
<td>DMAS3</td>
</tr>
<tr>
<td>(Bank 1 SB)</td>
<td>(Bank 1 SB)</td>
<td>(Bank 1 SB)</td>
<td>(Bank 1 SB)</td>
</tr>
</tbody>
</table>

Store a memory address at the source of DMA transfer

**Setting DMAi transfer count register (i=0 to 3)**

<table>
<thead>
<tr>
<th>DMA0 transfer count register</th>
<th>DMA1 transfer count register</th>
<th>DMA2 transfer count register</th>
<th>DMA3 transfer count register</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
<td>[CPU internal register]</td>
</tr>
<tr>
<td>DCT0</td>
<td>DCT1</td>
<td>DCT2 (Bank 1 R0)</td>
<td>DCT3 (Bank 1 R1)</td>
</tr>
<tr>
<td>(Bank 1 R0)</td>
<td>(Bank 1 R1)</td>
<td>(Bank 1 R0)</td>
<td>(Bank 1 R1)</td>
</tr>
</tbody>
</table>

Transfer counter
Set a value of transfer number

**Setting DMAi transfer count reload register (i=0 to 3)**

<table>
<thead>
<tr>
<th>DMA0 transfer count reload register</th>
<th>DMA1 transfer count reload register</th>
<th>DMA2 transfer count reload register</th>
<th>DMA3 transfer count reload register</th>
</tr>
</thead>
<tbody>
<tr>
<td>[CPU internal register] DRC0</td>
<td>[CPU internal register] DRC1</td>
<td>[CPU internal register] DRC2</td>
<td>[CPU internal register] DRC3</td>
</tr>
<tr>
<td>SVP</td>
<td>(Bank 1 R0)</td>
<td>(Bank 1 R2)</td>
<td>(Bank 1 R3)</td>
</tr>
</tbody>
</table>

Reload value of transfer counter
Set a value of transfer number

**Selecting DMA mode register i (i=1,0)**

<table>
<thead>
<tr>
<th>DMA mode register 0</th>
<th>[CPU internal register] DMD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 0 transfer mode select bit</td>
<td>1 1 : Repeat transfer</td>
</tr>
<tr>
<td>Channel 0 transfer unit select bit</td>
<td>1 : 16 bits</td>
</tr>
<tr>
<td>Channel 0 transfer direction select bit</td>
<td>0 : Fixed address to Memory</td>
</tr>
<tr>
<td>Channel 1 transfer mode select bit</td>
<td>1 1 : Repeat transfer</td>
</tr>
<tr>
<td>Channel 1 transfer unit select bit</td>
<td>1 : 16 bits</td>
</tr>
<tr>
<td>Channel 1 transfer direction select bit</td>
<td>0 : Fixed address to Memory</td>
</tr>
</tbody>
</table>

**Selecting DMA mode register 1**

<table>
<thead>
<tr>
<th>DMA mode register 1</th>
<th>[CPU internal register] DMD1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 2 transfer mode select bit</td>
<td>1 1 : Repeat transfer</td>
</tr>
<tr>
<td>Channel 2 transfer unit select bit</td>
<td>1 : 16 bits</td>
</tr>
<tr>
<td>Channel 2 transfer direction select bit</td>
<td>0 : Fixed address to Memory</td>
</tr>
<tr>
<td>Channel 3 transfer mode select bit</td>
<td>1 1 : Repeat transfer</td>
</tr>
<tr>
<td>Channel 3 transfer unit select bit</td>
<td>1 : 16 bits</td>
</tr>
<tr>
<td>Channel 3 transfer direction select bit</td>
<td>0 : Fixed address to Memory</td>
</tr>
</tbody>
</table>

When software DMA request bit and DMA request bit = “1” simultaneously
Start DMA transmission
4.0 Programming Code

;******************************************************************************
;  Include
;******************************************************************************
.LIST OFF ; Stops outputting lines to the assembler list file
.INCLUDE sr80100.inc ; Reads the file that defined SFR
.LIST ON ; Starts outputting lines to the assembler list file

;******************************************************************************
;  Symbol definition
;******************************************************************************
RAM_TOP .EQU 000400H ; Start address of RAM
RAM_END .EQU 002BFFH ; End address of RAM
ROM_TOP .EQU 0FFC000H ; Start address of ROM
FIXED_VECT_TOP .EQU 0FFFFDCH ; Start address of fixed vector
C_CNT_DMA .EQU 2 ; DMA transfer counter

;******************************************************************************
;  Allocation of work RAM area
;******************************************************************************
.SECTION WORKRAM, DATA
.ORG RAM_TOP
WORKRAM_TOP:
  v_Src_DMA: .BLKW 1 ; DMA source
  v_Dst_DMA: .BLKW (C_CNT_DMA); DMA destination area
WORKRAM_END:

;******************************************************************************
;  Program area
;******************************************************************************

;******************************************************************************
;  Start up
;******************************************************************************
.SECTION PROGRAM, CODE ; Declares section name and section type
.ORG ROM_TOP ; Declares start address
RESET:
  LDC #RAM_END+1, ISP ; Sets initial value in stack pointer
  ; Sets Processor mode, System clock and Main clock division
  MOV.B #03H, prcr ; Removes protect
  MOV.B #1000000B, pm0 ; Single-chip mode
  MOV.B #1100000B, pm1 ; Flash memory version
  MOV.B #0001000B, cm0 ; Xcin-Xcout High
  MOV.B #0010000B, cm1 ; Xin-Xout High
  MOV.B #00010010B, mcd ; No division mode
  MOV.B #00H, prcr ; Protects all registers
; DMAC (repeated transfer mode)
;=============================================================================
MOV.W    #055AAH, v_Src_DMA    ; Setting DMA transmit data

; Disable DMA
STC    dmd0, R0              ; Read DMA mode register
AND.B   #11111100B, R0L
; -----------; Channel 0 transfer mode select bit (00:DMA0 inhibit)
LDC    R0, dmd0               ; Disable DMA0
; Setting DMA0 request cause select register
MOV.B   #10000000B, dm0sl
; | |+++++---------; DMA request cause select bit (00000:Software trigger)
; | +--------------; Software DMA request bit (Set to 0)
; +----------------; DMA request bit (Set to 1)
; Setting DMA0 memory address register (Setting destination memory address)
; When the transfer direction is "fixed address to memory", 
; this register is destination memory address.
LDC     #(v_Dst_DMA & 0FFFFFFh), dma0
; Setting DMA0 memory address reload register
LDC     #(v_Dst_DMA & 0FFFFFFh), dra0
; Setting DMA0 SFR address register (Setting source fixed address)
; When the transfer direction is "fixed address to memory", 
; this register is source fixed address.
LDC     #(v_Src_DMA & 0FFFFFFh), dsa0
; Setting DMA0 transfer count register
LDC     #(C_CNT_DMA & 0FFFFh), dct0
; Setting DMA0 transfer count reload register
LDC     #(C_CNT_DMA & 0FFFFh), drc0
; Selecting DMA mode register
OR.B    #00000111B, R0L
; ||||||++---------; Channel 0 transfer mode select bit (11:Repeat transfer)
; |||||++---------; Channel 0 transfer unit select bit (1:16bits)
; |||||++---------; Channel 0 transfer direction select bit (0:Fixed address to Memory)
; ||+++++---------; Channel 1 transfer mode select bit
; |+++++---------; Channel 1 transfer unit select bit
; +---------------; Channel 1 transfer mode select bit
; Dummy cycles 8+6N (N is the number of other DMA channels that may generate a DMA request)
NOP
NOP
NOP
NOP
NOP
NOP
NOP
LDC    R0, dmd0               ; Enable DMA0

; Start DMA transmission
; Write software DMA request bit and DMA request bit = "1" simultaneously
OR.B   #0A0H, dm0sl

MAIN:
    JMP     MAIN
; Dummy interrupt processing program
dummy:
    REIT
;
;******************************************************************************
;       Setting of fixed vector
;******************************************************************************

.SECTION    F_VECT, ROMDATA
.ORG        FIXED_VECT_TOP

.LWORD    dummy    ;Undefined instruction
.LWORD    dummy    ;Overflow
.LWORD    dummy    ;BRK instruction execution
.LWORD    dummy    ;Address match
.LWORD    dummy    ;
.LWORD    dummy    ;Watchdog timer
.LWORD    dummy    ;
.LWORD    dummy    ;NMI
.LWORD    RESET    ;Reset

.END
5.0 Reference
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