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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group

Operation of DMAC (one-shot transfer mode)

1.0 Abstract

In one-shot transfer mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up	
Transfer space	o	Fixed address from an arbitrary 16 M bytes space
		Arbitrary 16 M bytes space from a fixed address
Unit of transfer	o	8 bits
		16 bits

2.0 Introduction

Operation (1) When software trigger is selected, setting software DMA request bit and DMA request bit to “1” simultaneously generates a DMA transfer request signal.

(2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi memory address register are transferred to the address indicated by the DMAi SFR address register. Each time a DMA transfer request signal is generated, 1 byte of data is transferred. The DMAi transfer count register is down counted, and the DMAi memory address register is up counted.

(3) If the DMAi transfer counter shifts from 0001_{16} to 0000_{16}, DMA transfer is completed. The DMAi interrupt request bit changes to “1” simultaneously.

Figure 1 shows example of operation of one-shot transfer mode.

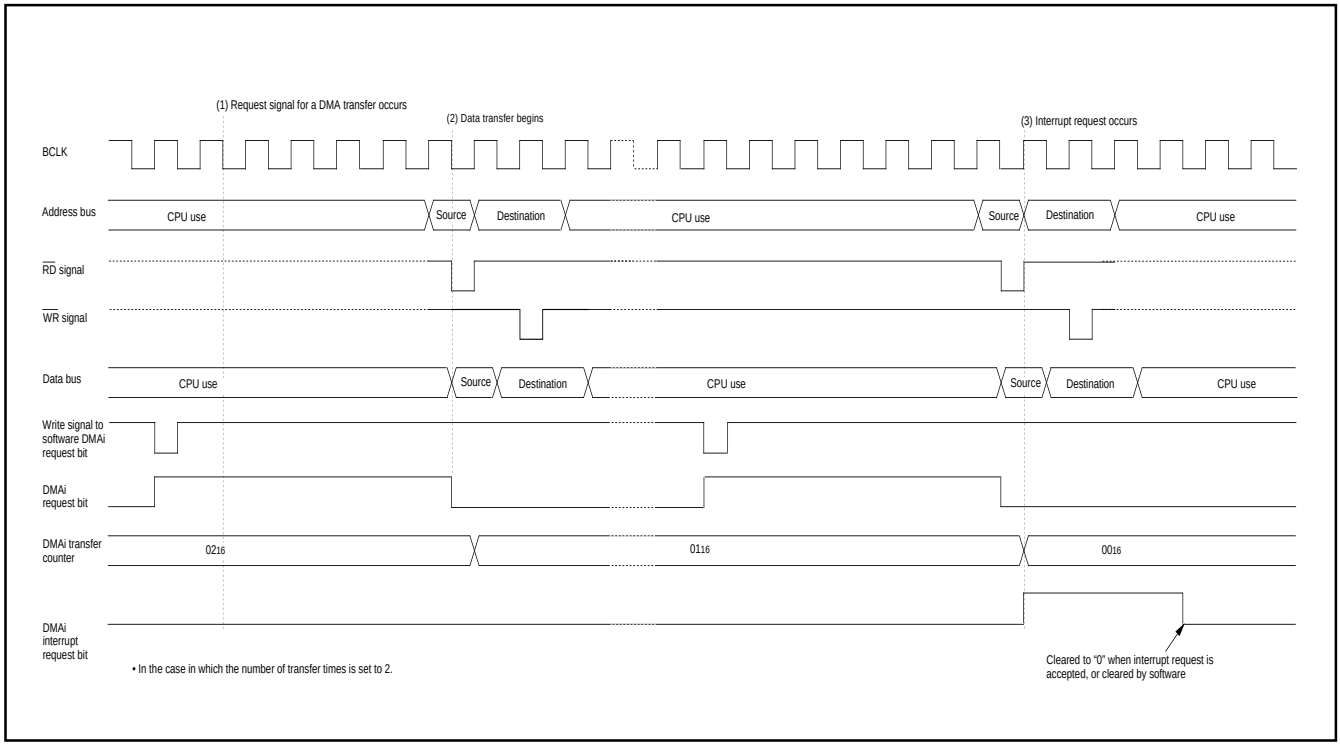
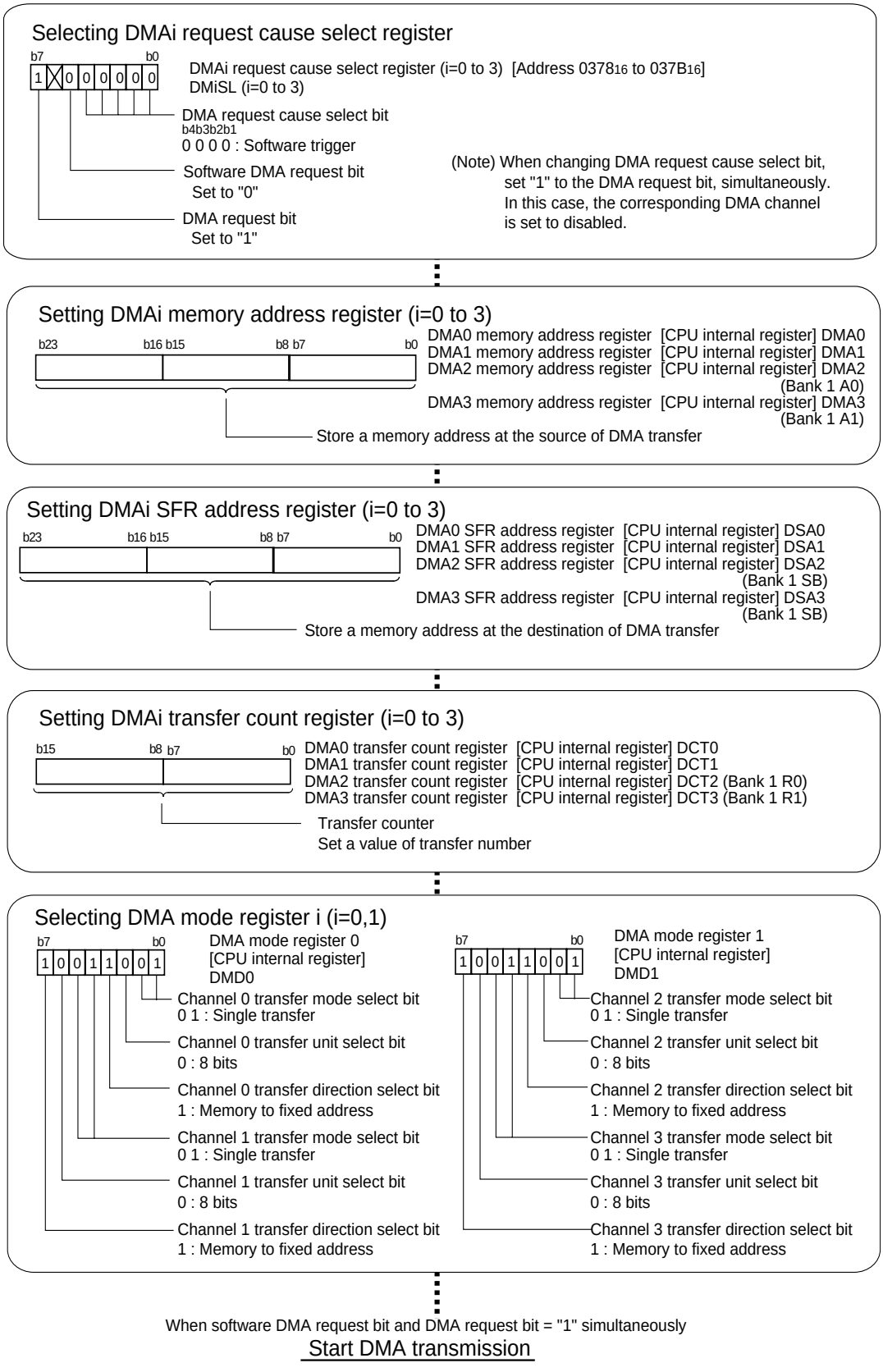


Figure 1. Example of operation of one-shot transfer mode

3.0 Set-up procedure



4.0 Programming Code

```
;*****************************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0484_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Operation of DMAC
;               (one-shot transfer mode)
;   HISTORY   : 2004.03.15  Ver 1.00
;
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;
;*****************************************************************************************
;*****************************************************************************************
;       Include
;*****************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;*****************************************************************************************
;       Symbol definition
;*****************************************************************************************
RAM_TOP          .EQU    000400H    ;Start address of RAM
RAM_END          .EQU    002BFFH    ;End address of RAM
ROM_TOP          .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP   .EQU    0FFFFDCH   ;Start address of fixed vector
C_CNT_DMA        .EQU    2          ;DMA transfer counter
;*****************************************************************************************
;       Program area
;*****************************************************************************************
;=========================================================================
;       Start up
;=========================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        LDC      #RAM_END+1, ISP   ;Sets initial value in stack pointer
        ; Sets Processor mode, System clock and Main clock division
        MOV.B    #03H, prcr        ;Removes protect
        MOV.B    #10000000B, pm0   ; Single-chip mode
        MOV.B    #11000000B, pm1   ; Flash memory version
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High
        MOV.B    #00010010B, mcd   ; No division mode
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
;=============================================================================
;       DMAC (one-shot transfer mode)
;=============================================================================
        MOV.B    #00H, p10          ;Setting DMA destination (Set P10 as output port)
        MOV.B    #0FFH, pd10
;
        ; Disable DMA0
        STC      dmd0, R0           ;Read DMA mode register
        AND.B    #11111100B, R0L
;                      ++---------;Channel 0 transfer mode select bit (00:DMA0 inhibit)
        LDC      R0, dmd0           ;Disable DMA0
        ; Setting DMA0 request cause select register
        MOV.B    #10000000B, dm0sl
;                | |+++++---------;DMA request cause select bit (00000:Software trigger)
;                | +--------------;Software DMA request bit (Set to 0)
;                +---------------;DMA request bit (Set to 1)
        ; Setting DMA0 memory address register (Setting source memory address)
                                   ;When the transfer direction is "memory to fixed address",
                                   ;this register is source memory address.
        LDC      #(SRC_DMA_TOP & 0FFFFFFh), dma0
        ; Setting DMA0 SFR address register (Setting destination fixed address)
                                   ;When the transfer direction is "memory to fixed address",
                                   ;this register is destination fixed address.
        LDC      #(p10 & 0FFFFFFh), dsa0
        ; Setting DMA0 transfer count register
        LDC      #(C_CNT_DMA & 0FFFFh), dct0
        ; Selecting DMA mode register
        OR.B     #00001001B, R0L
;                |||||++---------;Channel 0 transfer mode select bit (01:Single transfer)
;                ||||||
;                |||||+----------;Channel 0 transfer unit select bit (0:8bits)
;                ||||+-----------;Channel 0 transfer direction select bit (1:Memory to fixed address)
;                ||++-------------;Channel 1 transfer mode select bit
;                |+---------------;Channel 1 transfer unit select bit
;                +----------------;Channel 1 transfer mode select bit
        ; Dummy cycles 8+6N (N is the number of other DMA channels that may generate a DMA request)
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        LDC      R0, dmd0           ;Enable DMA0
;
        ; Start DMA transmission
        ; Write software DMA request bit and DMA request bit = "1" simultaneously
        OR.B     #0A0H, dm0sl
;
MAIN:
        JMP      MAIN
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*****************************************************************************
;       DMA source area
;*****************************************************************************
    .SECTION    SRC_DMA, ROMDATA, ALIGN
SRC_DMA_TOP:
        .BYTE    01h, 02h    ;DMA transmission data
;
```

```
;*******************************************************************************
;       Setting of fixed vector
;*******************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

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Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/80 group Rev. E3

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