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April 1st, 2010
Renesas Electronics Corporation

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1.0 Abstract
In repeat sweep mode 1, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chossed functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation clock φAD</td>
<td>Divided by 4 / divided-by-2</td>
<td>Trigger for starting</td>
<td>Software trigger</td>
</tr>
<tr>
<td></td>
<td>by 2 φAD</td>
<td>A-D conversion</td>
<td>Trigger by ADTRG</td>
</tr>
<tr>
<td>Resolution</td>
<td>8-bit / 10-bit</td>
<td>Expanded analog</td>
<td>Not used</td>
</tr>
<tr>
<td>Analog input pin</td>
<td>ANo (1 pin) / ANo and ANi (2</td>
<td>Sample &amp; Hold</td>
<td>External ope-amp connection mode</td>
</tr>
<tr>
<td></td>
<td>pins) / ANo to ANi (3 pins) /</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ANo to ANs (4 pins)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.0 Introduction
Operation  
(1) Setting the A-D conversion start flag to “1” causes the A-D converter to start the conversion on voltage input to the AN0 pin.

(2) After the A-D conversion on voltage input to the AN0 pin is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register 0.

(3) Every time the A-D converter carries out A-D conversion on a selected analog input pin, the A-D converter carries out A-D conversion on only one unselected pin, and then the A-D converter carries out A-D conversion from the AN0 pin again. The conversion result is transmitted to the corresponding A-D register each time conversion on a pin is completed. The A-D conversion interrupt request bit does not change.

(4) The A-D converter continues operating until software goes the A-D conversion start flag to “0”.

Note  
- In repeat sweep mode 1, the A-D conversion interrupt request bit does not change. By using Timer, it is possible to make it synchronize with the timing which A-D conversion completes, and to read conversion results repeatedly.

Figure 1 shows ANi pin’s sweep sequence, Figure 2 shows the operation timing.

Figure 1. ANi pin’s sweep sequence in repeat sweep mode 1

Figure 2. Operation timing of repeat sweep mode 1 (When AN0 is selected)
3.0 Set-up procedure

Selecting Sample and hold

Setting A-D control register 0 and A-D control register 1

Setting A-D conversion start flag

Converting non-selected pin after converting pins selected through the A-D sweep pin select bit.

Start A-D conversion

Transmitting conversion result to A-D register i

Setting A-D conversion start flag

Stop A-D conversion
4.0 Programming Code

;************************************************************************************
;  M16C/80 Program Collection
;  FILE NAME : rjj05b0482_src.a30
;  CPU       : M16C/80 Group
;  FUNCTION  : Operation of A-D Converter
;               (in repeat sweep mode 1)
;  HISTORY   : 2004.02.02  Ver 1.00
;  Copyright(C)2003, Renesas Technology Corp.
;  Copyright(C)2003, Renesas Solutions Corp.
;  All rights reserved.
; ************************************************************************************
;************************************************************************************
;   Include
;************************************************************************************
.LIST OFF ;Stops outputting lines to the assembler list file
.INCLUDE sfr80100.inc ;Reads the file that defined SFR
.LIST ON ;Starts outputting lines to the assembler list file
;
;Symbol definition
;************************************************************************************
RAM_TOP   .EQU    000400H    ;Start address of RAM
RAM_END   .EQU    002BFFH    ;End address of RAM
ROM_TOP   .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFFDCH   ;Start address of fixed vector
;
;Program area
;************************************************************************************
;Start up
;************************************************************************************
.SECTION PROGRAM, CODE ;Declares section name and section type
.ORG      ROM_TOP ;Declares start address
RESET:
LDC      #RAM_END+1, ISP ;Sets initial value in stack pointer
MOV.B    #03H, prcr ;Removes protect
MOV.B    #10000000B, pm0 ; Single-chip mode
MOV.B    #11000000B, pm1 ; Flash memory version
MOV.B    #00010000B, cm0 ; Xcin-Xcout High
MOV.B    #00100000B, cm1 ; Xin-Xout High
MOV.B    #00010101B, mcd ; No division mode
MOV.B    #00H, prcr ; Protects all registers
; Operation of A-D Converter (in repeat sweep mode 1)

; Selecting sample and hold
MOV.B #00000001B, adcon2
;                        +---------;A-D conversion method select bit
;                                   (1:With sample and hold)
; Setting A-D control register 0 and A-D control register 1
MOV.B #10011000B, adcon0
;                 |||||+++---------;Invalid in repeat sweep mode 1
;                 |||++------------;Repeat sweep mode 1 is selected
;                 ||+--------------;Trigger select bit (0:Software trigger)
;                 |+---------------;A-D conversion start flag (0:A-D conversion disabled)
;                 +----------------;Frequency select bit 0 (1:fAD/2 is selected)
MOV.B #00101100B, adcon1
;                 ||||||++---------;A-D sweep pin select bit (00:AN0(1pin))
;                 |||||+-----------;A-D operation mode select bit1
;                 |||||             (Must always be "1" in repeat sweep mode 1)
;                 ||||+------------;8/10-bit mode select bit (1:10-bit mode)
;                 |||+-------------;Frequency select bit 1 (0:fAD/2 or fAD/4 is selected)
;                 ||+--------------;Vref connect bit (1:Vref connected) (Note)
;                 ++---------------;External op-amp connection mode bit
;                                   (00:ANEX0 and ANEX1 are not used) (Note)
; Setting the direction register of the relevant port to input
MOV.B #00H, pd10        ;AN0-AN7(P100-P107):Analog input pin
; (Note) Setting function select register B3 (ANEX0 & ANEX1 are not used)
BCLR psl3_5            ;P95:Input peripheral function enabled
BCLR psl3_6            ;P96:Input peripheral function enabled

;-----------------------------------------------------------------------------
;       Start A-D conversion
;-----------------------------------------------------------------------------
; (Note) When the Vref connection bit is changed from 0 to 1,
;        start A-D conversion after an elapsing of 1 us or longer.
MOV.W #10, R0           ; 10 * 2cy = 20cy = 1 us or longer (@20MHz)
PRE_START:
NOP
NOP
ADJNZ.W #-1, R0, PRE_START
; START_AD:
BSET adst              ; Setting A-D conversion start flag
; REPEAT_AD_CNV:
;
; Processing of reading A-D conversion result
; depending on the application program.
;
JMP REPEAT_AD_CNV
;
;-----------------------------------------------------------------------------
;       Stop A-D conversion
;-----------------------------------------------------------------------------
STOP_AD:
BCLR adst              ; A-D conversion stop
; STOPPED_AD:
JMP STOPPED_AD
;
; Dummy interrupt processing program
; Setting of fixed vector

;rese:        REIT

; SECTION F_VECT, ROMDATA
; ORG FIXED_VECT_TOP

.LWORD   dummy ; Undefined instruction
.LWORD   dummy ; Overflow
.LWORD   dummy ; BRK instruction execution
.LWORD   dummy ; Address match
.LWORD   dummy ;
.LWORD   dummy ; Watchdog timer
.LWORD   dummy ;
.LWORD   dummy ; NMI
.LWORD   RESET ; Reset

.END
5.0 Reference
Renesas Technology Corporation Semiconductor Home page
http://www.renesas.com/

Technical Support
E-mail: support_apl@renesas.com

Data Sheet
M16C/80 group Rev. E3
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