To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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**1.0 Abstract**

In repeat mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

**Table 1. Chosen functions**

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation clock ( \phi_{AD} )</td>
<td>Divided-by-4 ( \phi_{AD} ) / divided-by-2 ( \phi_{AD} )</td>
<td>Expanded analog input pin</td>
<td>Not used</td>
</tr>
<tr>
<td>Resolution</td>
<td>8-bit / 10-bit</td>
<td></td>
<td>Either ANEX0 pin or ANEX1 pin</td>
</tr>
<tr>
<td>Analog input pin</td>
<td>One of ANi pin to ANr pin</td>
<td></td>
<td>External operation amplifier connection mode</td>
</tr>
<tr>
<td>Trigger for starting A-D conversion</td>
<td>Software trigger</td>
<td>Sample &amp; Hold</td>
<td>Not activated</td>
</tr>
<tr>
<td></td>
<td>Trigger by ADTRG</td>
<td></td>
<td>Activated</td>
</tr>
</tbody>
</table>

**2.0 Introduction**

Operation (1) Setting the A-D conversion start flag to “1” causes the A-D converter to start operating.

(2) After the first conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i. The A-D conversion interrupt request bit does not change.

(3) The A-D converter continues operating until the A-D conversion start flag is set to “0” by software. The conversion result is transmitted to A-D register i every time a conversion is completed.

Note • In repeat mode, the A-D conversion interrupt request bit does not change. By using Timer, it is possible to make it synchronize with the timing which A-D conversion completes, and to read conversion results repeatedly.

Figure 1 shows the operation timing

---

**Note:** When \( \phi_{AD} \) frequency is less than 1MHz, sample and hold function cannot be selected. Conversion rate per analog input pin is 49 \( \phi_{AD} \) cycles for 8-bit resolution and 59 \( \phi_{AD} \) cycles for 10-bit resolution.
3.0 Set-up procedure

### Setting A-D control register 0 and A-D control register 1

<table>
<thead>
<tr>
<th>Register 0</th>
<th>Register 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog input pin select bit (Note 1)</td>
<td>Analog input pin select bit (Note 1)</td>
</tr>
<tr>
<td>0 0 0 : AN0 is selected</td>
<td>b7 b6</td>
</tr>
<tr>
<td>0 0 1 : AN1 is selected</td>
<td>0 0 : Vref connected</td>
</tr>
<tr>
<td>0 1 0 : AN2 is selected</td>
<td>b2 b1 b0</td>
</tr>
<tr>
<td>0 1 1 : AN3 is selected</td>
<td>0 0 0 : ANEX0 and ANEX1 are not used</td>
</tr>
<tr>
<td>1 0 0 : AN4 is selected</td>
<td>(Note 3)</td>
</tr>
<tr>
<td>1 0 1 : AN5 is selected</td>
<td>1 0 1 : AN6 is selected</td>
</tr>
<tr>
<td>1 1 0 : AN6 is selected</td>
<td>1 1 1 : AN7 is selected</td>
</tr>
<tr>
<td>1 1 1 : AN7 is selected</td>
<td>0 0 1</td>
</tr>
</tbody>
</table>

**Note 1**: Rewrite to analog input pin select bit after changing A-D operation mode.

**Note 2**: When f(XIN) is over 10 MHz, the fAD frequency must be under 10 MHz by dividing and set fAD frequency to 10 MHz or lower.

**Note 3**: Set “0” to PSL3_5 and PSL3_6 of the function select register B3.

### Transmitting conversion result to A-D register

- Eight low-order bits of A-D conversion result
- During 10-bit mode
- Two high-order bits of A-D conversion result
- During 8-bit mode
- When read, the content is indeterminate

### Setting A-D conversion start flag

<table>
<thead>
<tr>
<th>Register 0</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A-D conversion start flag</td>
<td>0 : A-D conversion disabled</td>
</tr>
<tr>
<td>1 : A-D conversion started</td>
<td></td>
</tr>
</tbody>
</table>

### Repeatedly carries out A-D conversion on pins selected through the A-D sweep pin select bit.

**Start A-D conversion**

**Stop A-D conversion**
4.0 Programming Code

;****************************************************************************
;  M16C/80 Program Collection
;  FILE NAME : rjj05b0479_src.a30
;  CPU       : M16C/80 Group
;  FUNCTION  : Operation of A-D Converter
;               (in repeat mode)
;  HISTORY   : 2004.02.02  Ver 1.00
;  Copyright(C)2003, Renesas Technology Corp.
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;  All rights reserved.
;****************************************************************************

;*****************************************************************************
; Include
;*****************************************************************************
.LIST       OFF            ;Stops outputting lines to the assembler list file
.INCLUDE    sfr80100.inc   ;Reads the file that defined SFR
.LIST       ON             ;Starts outputting lines to the assembler list file

;*****************************************************************************
; Symbol definition
;*****************************************************************************
RAM_TOP         .EQU    000400H    ;Start address of RAM
RAM_END         .EQU    002BFFH    ;End address of RAM
ROM_TOP         .EQU    0FFC000H   ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFFDCH   ;Start address of fixed vector

;*****************************************************************************
; Program area
;*****************************************************************************

;*****************************************************************************
; Start up
;*****************************************************************************
.RESET:
LDC      #RAM_END+1, ISP   ;Sets initial value in stack pointer
; Sets Processor mode, System clock and Main clock division
MOV.B    #03H, prcr        ;Removes protect
MOV.B    #10000000B, pm0   ;Single-chip mode
MOV.B    #11000000B, pm1   ;Flash memory version
MOV.B    #00000100B, cm0   ;Xcin-Xcout High
MOV.B    #00100000B, cm1   ;Xin-Xout High
MOV.B    #00010010B, mcd   ;No division mode
MOV.B    #00H, prcr        ;Protects all registers
; Operation of A-D Converter (in repeat mode)

; Selecting sample and hold
MOV.B #00000001B, adcon2
;                        +---------;A-D conversion method select bit
;                                   (1:With sample and hold)

; Setting A-D control register 0 and A-D control register 1
MOV.B #10001000B, adcon0
;                 |||||+++---------;Analog input pin select bit (000:AN0 is selected)
;                 |||++------------;Repeat mode is selected
;                 ||+--------------;Trigger select bit (0:Software trigger)
;                 |+---------------;A-D conversion start flag (0:A-D conversion disabled)
;                 +----------------;Frequency select bit 0 (1:fAD/2 is selected)
MOV.B #00101000B, adcon1
;                 |||||++---------;Invalid in Repeat mode
;                 |||||+-----------;A-D operation mode select bit1
;                 |||||             (Must always be "0" in repeat mode)
;                 ||||+------------;8/10-bit mode select bit (1:10-bit mode)
;                 |||+-------------;Frequency select bit 1 (0:fAD/2 or fAD/4 is selected)
;                 ||+--------------;Vref connect bit (1:Vref connected) (Note)
;                 ++---------------;External op-amp connection mode bit
;                                           (00:ANEX0 and ANEX1 are not used) (Note)

; Setting the direction register of the relevant port to input
BCLR pd10_0            ; AN0(P100):Analog input pin
; (Note) Setting function select register B3 (ANEX0 & ANEX1 are not used)
BCLR psl3_5            ; P95:Input peripheral function enabled
BCLR psl3_6            ; P96:Input peripheral function enabled

;-----------------------------------------------------------------------------
;       Start A-D conversion
;-----------------------------------------------------------------------------

; (Note) When the Vref connection bit is changed from 0 to 1,
;       start A-D conversion after an elapsing of 1 us or longer.
MOV.W #10, R0           ; 10 * 2cy = 20cy = 1 us or longer (@20MHz)
PRE_START:
NOP
NOP
ADJNZ.W #-1, R0, PRE_START

START_AD:
; Setting A-D conversion start flag
BSET adst              ; A-D conversion started

REPEAT_AD_CNV:

; Processing of reading A-D conversion result
; depending on the application program.
; JMP REPEAT_AD_CNV

;-----------------------------------------------------------------------------
;       Stop A-D conversion
;-----------------------------------------------------------------------------

STOP_AD:
BCLR adst              ; A-D conversion stop

STOPPED_AD:
JMP STOPPED_AD
; Dummy interrupt processing program
; ************************************************
dummy:
   REIT
;
; ************************************************
; Setting of fixed vector
; ************************************************
   .SECTION  F_VECT, ROMDATA
   .ORG     FIXED_VECT_TOP
;
   .LWORD    dummy    ;Undefined instruction
   .LWORD    dummy    ;Overflow
   .LWORD    dummy    ;BRK instruction execution
   .LWORD    dummy    ;Address match
   .LWORD    dummy    ;
   .LWORD    dummy    ;Watchdog timer
   .LWORD    dummy    ;
   .LWORD    dummy    ;NMI
   .LWORD    RESET    ;Reset
;
   .END
5.0 Reference
Renesas Technology Corporation Semiconductor Home page  
http://www.renesas.com/

Technical Support  
E-mail: support_apl@renesas.com

Data Sheet  
M16C/80 group Rev. E3  
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