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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group
Operation of A-D Converter (in one-shot mode, an external trigger)

1.0 Abstract
In one-shot mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosen functions

<table>
<thead>
<tr>
<th>Item</th>
<th>Set-up</th>
<th>Item</th>
<th>Set-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation clock φAD</td>
<td>Divided-by-4 φAD / divided-by-2 φAD</td>
<td>Expanded analog input pin</td>
<td>Not used</td>
</tr>
<tr>
<td>Resolution</td>
<td>8-bit / 10-bit</td>
<td>External operation amplifier connection mode</td>
<td>Either ANEX0 pin or ANEX1 pin</td>
</tr>
<tr>
<td>Analog input pin</td>
<td>One of ANx pin to ANy pin</td>
<td>Sample &amp; Hold</td>
<td>Not activated</td>
</tr>
<tr>
<td>Trigger for starting A-D Conversion</td>
<td>Software trigger</td>
<td>Trigger by ADTRG</td>
<td>Activated</td>
</tr>
</tbody>
</table>

2.0 Introduction
Operation
1) If the level of the ADTRG changes from “H” to “L” with the A-D conversion start flag set to “1”, the A-D converter begins operating.
2) After A-D conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i. At this time, the A-D conversion interrupt request bit goes to “1”. Also the A-D converter stops operating.
3) If the level of the ADTRG pin changes from “H” to “L”, the A-D converter carries out conversion from step (1) again. If the level of the ADTRG pin changes from “H” to “L” while conversion is in progress, the A-D converter stops the A-D conversion in process, and carries out conversion from step (1) again.

Figure 1 shows the operation timing.

Figure 1. Operation timing of one-shot mode, with an external trigger selected

Note: When φAD frequency is less than 1MHz, sample and hold function cannot be selected.
Conversion rate per analog input pin is 49 φAD cycles for 8-bit resolution and 59 φAD cycles for 10-bit resolution.
3.0 Set-up procedure

Selecting sample and hold

- A-D control register 2 [Address 0394H]
- A-D conversion method select bit
  1 : With sample and hold

Setting A-D control register 0 and A-D control register 1

- A-D control register 0 [Address 0396H]
- A-D conversion start flag
  0 : A-D conversion disabled
  1 : A-D conversion started
- Analog input pin select bit (Note 1)
  0 0 0 : AN0 is selected
  0 0 1 : AN1 is selected
  0 1 0 : AN2 is selected
  0 1 1 : AN3 is selected
  1 0 0 : AN4 is selected
  1 0 1 : AN5 is selected
  1 1 0 : AN6 is selected
  1 1 1 : AN7 is selected
- Frequency select bit 0 (Note 2)
  0 : fAD/4 is selected
  1 : fAD/2 is selected
- One-shot mode is selected (Note 1)
- Trigger select bit
  0 : ADTRG trigger
  1 : A-D conversion disabled
- A-D operation mode select bit 1 (Note 1)
  0 (Must always be "0" in one-shot mode)
- 8/10-bit mode select bit
  0 : 8-bit mode
  1 : 10-bit mode
- Frequency select bit 1 (Note 2)
  0 : fAD/4 is selected
  1 : fAD/2 is selected
- Vref connect bit
  0 : Vref connected
  1 : Vref disconnected
- External op-amp connection mode bit
  0 0 : ANEX0 and ANEX1 are not used (Note 3)

- Invalid in one-shot mode
- A-D conversion disabled

Note 1 : Rewrite to analog input pin select bit after changing A-D operation mode.
Note 2 : When f(XIN) is over 10 MHz, the fAD frequency must be under 10 MHz by dividing and set fAD frequency to 10 MHz or lower.
Note 3 : Set "0" to PS03_5 and PS03_6 of the function select register B3.

Setting A-D conversion start flag

- A-D control register 0 [Address 0396H]
- A-D conversion start flag
  0 : A-D conversion disabled
  1 : A-D conversion started

When ADTRG pin level becomes from "H" to "L"

Start A-D conversion

Reading conversion result

- Eight low-order bits of A-D conversion result
- During 10-bit mode
  Two high-order bits of A-D conversion result
- During 8-bit mode
  When read, the content is indeterminate

Setting A-D conversion start flag

- A-D control register 0 [Address 0396H]
- A-D conversion start flag
  0 : A-D conversion disabled
  1 : A-D conversion started

Stop A-D conversion
4.0 Programming Code

;****************************************************************************
; 4.0 Programming Code
;****************************************************************************

;****************************************************************************
; M16C/80 Program Collection
;****************************************************************************

;****************************************************************************
; FILE NAME : rj05b0476_src.a30
; CPU : M16C/80 Group
; FUNCTION : Operation of A-D Converter
;            (in one-shot mode, an external trigger)
; HISTORY : 2004.02.02  Ver 1.00
; Copyright(C)2003, Renesas Technology Corp.
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; All rights reserved.
;****************************************************************************

;****************************************************************************
; Include
;****************************************************************************

.LIST       OFF            ;Stops outputting lines to the assembler list file
.INCLUDE    sfr80100.inc   ;Reads the file that defined SFR
.LIST       ON             ;Starts outputting lines to the assembler list file

;****************************************************************************
; Symbol definition
;****************************************************************************

RAM_TOP   .EQU    000400H    ;Start address of RAM
RAM_END    .EQU    002BFFH    ;End address of RAM
ROM_TOP    .EQU    0FFC000H   ;Start address of ROM
FIXED_VEC_TOP .EQU    0FFFFDCH   ;Start address of fixed vector

;****************************************************************************
; Allocation of work RAM area
;****************************************************************************

;****************************************************************************
; .SECTION WORKRAM, DATA
; .ORG RAM_TOP
;****************************************************************************

WORKRAM_TOP:
v_AD_result:   .BLKW   1          ; RAM area where A-D conversion result is stored
WORKRAM_END:

;****************************************************************************
; Program area
;****************************************************************************

;****************************************************************************
; Start up
;****************************************************************************

;****************************************************************************
; .SECTION PROGRAM, CODE
; .ORG ROM_TOP
;****************************************************************************

RESET:
  LDC      #RAM_END+1, ISP   ;Sets initial value in stack pointer
  ; Sets Processor mode, System clock and Main clock division
  MOV.B    #03H, prcr       ;Removes protect
  MOV.B    #10000000B, pm0  ; Single-chip mode
  MOV.B    #11000000B, pm1  ; Flash memory version
  MOV.B    #00001000B, cm0  ; Xcin-Xcout High
  MOV.B    #00100000B, cm1  ; Xin-Xout High
  MOV.B    #00010010B, mcd  ; No division mode
  MOV.B    #00H, prcr       ;Protects all registers
  MOV.W    #0, v_AD_result  ;Clear area where A-D conversion result will be stored
Operation of A-D Converter (in one-shot mode, an external trigger)

; Disabling A-D conversion interrupt and clearing interrupt request bit to "0"
MOV.B #000, adic
; Setting sample and hold
MOV.B #00000001B, adcon2
; A-D conversion method select bit
(1: With sample and hold)
; Setting A-D control register 0 and A-D control register 1
MOV.B #10100000B, adcon0
; Analog input pin select bit (000: AN0 is selected)
; One-shot mode is selected
; Trigger select bit (1: ADTRG trigger)
; A-D conversion start flag (0: A-D conversion disabled)
; Frequency select bit 0 (1: fAD/2 is selected)
MOV.B #00101000B, adcon1
; Invalid in one-shot mode
; A-D operation mode select bit
; 8/10-bit mode select bit (1: 10-bit mode)
; Vref connect bit (1: Vref connected) (Note)
; External op-amp connection mode bit
; (Note) Setting function select register B3 (ANEX0 and ANEX1 are not used) (Note)

; Setting direction register of the relevant port to input
BCLR pd10_0 ; AN0 (P100): Analog input pin
; Setting direction register of the external trigger input pin
MOV.B #00000100B, prcr ; Clearing the protect (set to write-enabled state)
BCLR pd9_7 ; ADTRG (P97): A-D external trigger input pin
BCLR ps3_7 ; ADTRG (P97) is I/O port
; (Note) Setting function select register B3 (ANEX0 & ANEX1 are not used)
BCLR ps13_5 ; P95: Input peripheral function enabled
BCLR ps13_6 ; P96: Input peripheral function enabled

; Setting the direction register of the relevant port to input

; Start A-D conversion

; (Note) When the Vref connection bit is changed from 0 to 1,
; start A-D conversion after an elapsing of 1 us or longer.
MOV.W #10, R0 ; 10 * 2cy = 20cy = 1 us or longer (@20MHz)
PRE_START:
NOP
NOP
ADJNZ.W #-1, R0, PRE_START
; Setting A-D conversion start flag
BSET adst
START_AD:
; When ADTRG pin level becomes from "H" to "L", start A-D conversion
WAIT_AD_CNV:
BTST ir_adic ; Waiting A-D conversion completing
JNC WAIT_AD_CNV
BCLR ir_adic ; Clear to "0" A-D conversion interrupt request
COMPLETE_CNV:
; Reading conversion result
MOV.W ad0, v_AD_result ; Read conversion result
AND.W #03FFH, v_AD_result ; Mask 10 bits result
JMP START_AD

Operation of A-D Converter (in one-shot mode, an external trigger)

;-----------------------------------------------------------------------------
; Stop A-D conversion
;-------------------------------------------------------------------------------
STOP_AD:
  BCLR    adst            ; A-D conversion stop
;
STOPPED_AD:
  JMP     STOPPED_AD
;
;-------------------------------------------------------------------------------
; Dummy interrupt processing program
;-------------------------------------------------------------------------------
dummy:
  REIT
;
; Setting of fixed vector
;-------------------------------------------------------------------------------
 SECTION  F_VECT, ROMDATA
 .ORG    FIXED_VECT_TOP
 ;
 .LWORD    dummy    ;Undefined instruction
 .LWORD    dummy    ;Overflow
 .LWORD    dummy    ;BRK instruction execution
 .LWORD    dummy    ;Address match
 .LWORD    dummy    ;
 .LWORD    dummy    ;Watchdog timer
 .LWORD    dummy    ;
 .LWORD    dummy    ;NMI
 .LWORD    RESET    ;Reset
 ;
 .END
5.0 Reference
Renesas Technology Corporation Semiconductor Home page
http://www.renesas.com/

Technical Support
E-mail: support_apl@renesas.com

Data Sheet
M16C/80 group Rev. E3
(Use the latest version on the Home page: http://www.renesas.com/)

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