

This application note describes the power dissipation and junction temperature calculation for LVCMOS clock buffers with series termination and parallel termination. ICS8701 is used as an example to describe the calculations. A similar approach can be used for calculating the power dissipation and junction temperature for other clock buffers with LVCMOS drivers.

## **LVCMOS Power Dissipation for Serial Termination**

The total power dissipation *Pd\_total* is composed of Static Power Dissipation *Pd\_static* and Dynamic Power Dissipation *Pd\_dynamic*.

### Pd\_total = Pd\_static + Pd\_dynamic

Where **Pd\_static** is static power dissipation under DC conditions **Pd\_dynamic** is dynamic power dissipation due to clocking.

### Static Power Dissipation

Static power dissipation is the power dissipation when the part is not switching. There are two sections in the ICS8701 circuitry, core and output driver. The core circuitry draws current  $I_{DDI}$  from the  $V_{DD}$  supply. The output driver circuitry draws current  $I_{DDO}$  from the  $V_{DDO}$  Supply.

The static power dissipation *Pd\_static* is composed of Core static power dissipation, *Pd\_core\_static* and output driver static power dissipation, *Pd\_drive\_static* 

#### Pd\_static = Pd\_core\_static + Pd\_drive\_static

Where Pd\_core\_static = I<sub>DDI</sub> \* V<sub>DD</sub> Pd\_drive\_static = I<sub>DDO</sub> \* V<sub>DDO</sub>

Since the supply current  $I_{DD}$  data provided in the data sheet is the sum of  $I_{DDI}$  and  $I_{DDO}$ 

#### $I_{DD} = I_{DDI} + I_{DDO}$

For  $V_{DD}$  =  $V_{DDO}$ , the total static power can be calculated as

 $Pd\_static = V_{DD}*I_{DD}$ 

### Dynamic Power Dissipation

Dynamic power dissipation *Pd\_dynamic* is composed of *Pd\_drive\_dynamic* and *Pd\_Rout*. For ICS8701, frequency has a very small effect on the core supply current  $I_{DDI}$ . To simplify the calculation, using the worst case  $I_{DDI}$  in the static power dissipation covers the core dynamic power dissipation. The dynamic core power dissipation is not required to be included in this section. Serial termination scheme is used as an example to calculate the dynamic power dissipation.

### Pd\_dynamic = Pd\_drive\_dynamic + Pd\_Rout

*Pd\_output\_dynamic* is the power dissipation within the output driver circuitry and can be calculated as

 $Pd_drive_dynamic = Cpd * (V_{DDO})^2 *F * N_out$ 

Where *Cpd* is Power dissipation capacitor per output *F* is driver clock frequency *N\_out* is total number of outputs enable. For 8701, N\_out = 20 *V<sub>DDO</sub>* is output power supply voltage.

**Pd\_Rout** is power dissipation on the output impedance due to loading condition. For series termination as shown in Figure 1, the output current will hold the peak current for a short period of time. The duration depends on the time delay of the transmission line Td.



Figure 1 LVCMOS output Series Termination

Figure 2 shows the timing diagram for the load current, related voltages on each point, and the power dissipation on Ro. For Td <  $\frac{1}{4}$  T, (where T is clock period), during each clock period, the load current will hold the peak load current *I\_load\_peak* for a duration of 2xTd for PMOS ON, NMOS OFF and additional 2xTd for PMOS OFF and NMOS ON. Calculating the power dissipation on the clock buffer chip due to the load current should not include the power dissipation on the loading. This element should only include power dissipation on the output resistor *R*<sub>o</sub>.

Pd\_Rout = [I\_load\_peak]<sup>2</sup> \* R<sub>0</sub> \*2\* (2\*Td/T) \* N\_load





For series termination,  $R_0 + R_s = Z_0$ , the peak load current is

 $I_load_peak = V_{DDO}/(2*Z_O)$ 

The peak power dissipation on R<sub>O</sub> is

 $Pd_peak = (I_load_peak)^2 * R_o$ 

The peak power Pd\_peak will hold for 4\*Td per clock period. Therefore the total average power dissipation for all N\_load is

 $Pd_Rout = [V_{DDO}/(2*Z_O)]^2 * R_O * (4*Td/T) * N_load$ 

Where *Td* is the time delay for the transmission line *T* is clock period *Z*<sub>o</sub> is characteristic impedance of the transmission line. *N\_load* is number of output being loaded with series termination

#### Summary

#### **Power Dissipation**

To calculate Power Dissipation for series terminations

Pd\_total = Pd\_static + Pd\_dynamic = Pd\_core\_static + Pd\_drive\_static + Pd\_drive\_dynamic + Pd\_Rout

Where,

 $\begin{array}{l} Pd\_core\_static = I_{DD} ^{*}V_{DD} \\ Pd\_drive\_static = I_{DDO} ^{*}V_{DDO} \\ Pd\_drive\_dynamic = Cpd ^{*}F ^{*}(V_{DDO}) ^{2} ^{*}N\_out \end{array}$ 

For transmission line delay Td less than ¼ T, clock time period

$$Pd_Rout = [V_{DDO}/(2*Z_O)]^2 * R_O * 2 * (2*Td/T) * N_load$$

### **Junction Temperature**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pads and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS<sup>TM</sup> devices is 125 °C

## $T_j = T_A + \theta_{AJ} * P\_Total$

Where,  $T_A$  is ambient temperature  $\theta_{AJ}$  is thermo resistance

### Example:

For ICS8701 with series termination,

All outputs enabled and loaded with one to one series termination.  $Z_0 = 50$  Ohm, Td = 1 nsec, Clock frequency, F = 100 MHz (or time period, T=10 nsec)

 $\label{eq:Rs} \begin{array}{l} \mathsf{R}_{\mathsf{S}} = \mathsf{Z}_{\mathsf{O}} - \mathsf{R}_{\mathsf{O}} = \mathsf{50} \ \mathsf{Ohm} - \mathsf{7} \ \mathsf{Ohm} = \mathsf{43} \ \mathsf{Ohm} \\ \mathsf{V}_{\mathsf{DD}}\mathsf{max} = \mathsf{V}_{\mathsf{DDO}}\mathsf{max} = \mathsf{3.465V} \end{array}$ 

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To calculated maximum static power dissipation, the power supply current  $I_{DD}$  given in the data sheet is combination of core power current  $I_{DDI}$  and driver power current  $I_{DDO}$ 

 $P\_core\_static\_max = V_{DD}max * I_{DD}max$ = 3.465V \* 95mA= 329.2mW

The core static power and the driver static power can be calculated separately using  $I_{DDI}$  and  $I_{DDO}$ . The  $I_{DD}$ \_max current can be split to  $I_{DDI}$ \_max = 50 mA,  $I_{DDO}$ \_max = 45mA

$$\label{eq:p_core_static_max} \begin{split} &\mathsf{P}\_core\_static\_max = \mathsf{I}_{\text{DD}} ^*\mathsf{V}_{\text{DD}} = 50 \text{ mA} ^* 3.465\mathsf{V} = 173.3 \text{ mW} \\ &\mathsf{P}\_drive\_static\_max = \mathsf{I}_{\text{DDO}} ^*\mathsf{V}_{\text{DDO}} = 45\mathsf{mA} ^* 3.465\mathsf{V} = 155.9 \text{ mW} \\ &\mathsf{P}\_static = \mathsf{P}\_core\_static\_max + \mathsf{P}\_drive\_static\_max = 329.2 \text{ mW} \end{split}$$

#### Dynamic power dissipation

Cpd\_max = 15pF Pd\_dynamic\_max = Cdp\_max \* Fclk \*  $(V_{DDO}_max)^2 * N_{out}$ = 15 pF \* 100MHz \*  $(3.465V)^2 * 20$ = 360 mW Pd\_Rout =  $[V_{DDO}/(2*Z_{O})]^2 * R_{O} * 2 * (2*Td/T) * N_{load}$ =  $[3.465V/(2*50 \text{ Ohm})]^2 * 7 * 2* (2* 1nsec/10nsec) * 20$ = 67.2 mW Pd total = 756.4 mW

#### **Junction Temperature**

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{AJ}$  must be used. Assuming a moderate airflow of 200 linear feet per minute and a multi-layer board, the appropriate value for ICS8701 is 42.1 °C/W shown in the data sheet. The Tj for an ambient temperature of  $T_A$  = 70 °C for this example is

#### $T_{j} = T_{A} + P_{Total} + \theta_{AJ}$

= 70 °C + 0.756 W \* 42.1 °C/W = 101.8 °C

Tj should be kept below 125 °C.

Figure 3 and Figure 4 show charts of the power dissipation and junction temperature for ICS8701 under the following environment:

Transmission line delay Td = 1ns  $V_{DD}$  = 3.465V  $V_{DDO}$  = 3.465V  $Z_O$  = 50 Ohm  $R_S$  = 43 Ohm







Figure 4 Junction Temperature vs Clock Frequency

## **LVCMOS Power Dissipation for Parallel Termination**

Figure 5 shows a parallel termination that configure for characterization. In actual application, the Figure 6 is an equivalent termination of the Figure 5. Both circuit and have equal result of power dissipation on the buffer. This section, Figure 5 is used for calculation.



Figure 5 LVCMOS Driver Standard Parallel Termination



Figure 6 LVCMOS Driver Equivalent Parallel Termination

To calculate Power Dissipation for parallel terminations

Pd\_total = Pd\_static + Pd\_dynamic = Pd\_core\_static + Pd\_drive\_static + Pd\_drive\_dynamic + Pd\_Rout

The *Pd\_core\_static, Pd\_drive\_static and Pd\_drive\_dynamic* are same as the results obtained from serial termination.

**Pd\_Rout** is power dissipation on the output impedance due to loading condition. For parallel matched load termination with characteristic impedance  $Z_0$ , the driver "sees" the loading impedance of  $Z_0$ . The power **Pd\_Rout** dissipates at PMOS when the output is logic high, and the power dissipated at NMOS when the output is logic low.

## $Pd_Rout = [(V_{DDO}/2)/(Rout+Z_0)]^2 * R_0 * N_load$

Where  $R_o$  is output impedance the LVCMOS driver.  $Z_o$  is characteristic impedance of the transmission line.  $N\_load$  is number of output being loaded with series termination

To calculate Pd\_Rout for Parallel termination

**Pd\_Rout** =  $[(V_{DDO}/2)/(Rout + Z_O)]^2 * R_O * N_load$ =  $[(3.465V/2)/(7 Ohm + 50 Ohm)]^2 * 7 * 20$ = 129.3 mW

For frequency F=100MHz, the total power dissipation is

Pd_total	= Pd_static + Pd_dymanic + Pd_out
	= 329.2 mW + 360 mW + 129.3 mW
	= 818.5 mW

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{AJ}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value for ICS8701 is 42.1 °C/W shown in the data sheet. The Tj for an ambient temperature of  $T_A = 70$  °C for this example is

 $T_j = T_A + P_Total^* \theta_{AJ}$ 

= 70 °C + 0.819 W \* 42.1 °C/W = 104.4 °C

Tj should be kept below 125 °C.

Figure 7 and Figure 8 show charts of the power dissipation and junction temperature for ICS8701 under the following environment:

 $V_{DD}$  = 3.465V  $V_{DDO}$  = 3.465V  $Z_{O}$  = 50 Ohm R1 = 50 Ohm



Figure 5 ICS8701 Power Dissipation for Parallel Termination vs Clock Frequency



Figure 6 Junction Temperature for Parallel Termination vs Clock Frequency

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