

This application note provides general design guide for high speed LVCMOS driver termination. To handle high speed LVCMOS drivers, general rules for high-speed digital board design must be carefully followed. Improper handling of the termination will cause signal reflection, clock ringing and lead to system failure. Proper termination is required to ensure signal integrity and Electro-Magnetic Interference (EMI) reduction. There are many different termination schemes for single ended LVCMOS drivers. This application note discusses parallel termination, AC termination and series termination. The following termination approaches are only general recommendations under ideal conditions. Board designers should consult with their signal integrity engineers and verify through simulations in their system environment.

### Parallel Termination

The standard termination of an LVCMOS driver in a  $Z_0=50$  ohm transmission line environment is shown in Figure 1. The driver is terminated with 50 Ohm pull down to  $V_{TT}=V_{DDO}/2$  at the receiver end. The LVCMOS clock buffer characterization set up is terminated in similar manner using split power supplies approach (See test condition in data sheet of an LVCMOS driver). In actual applications, the equivalent parallel termination shown in Figure 2 can be used. The LVCMOS parallel termination has the same effect as the standard LVCMOS shown in Figure 1. The parallel termination shown in Figure 2 can eliminate the need of  $V_{TT}=V_{DDO}/2$  power supply (or reference voltage). The power dissipation calculation is described in a separate application note.

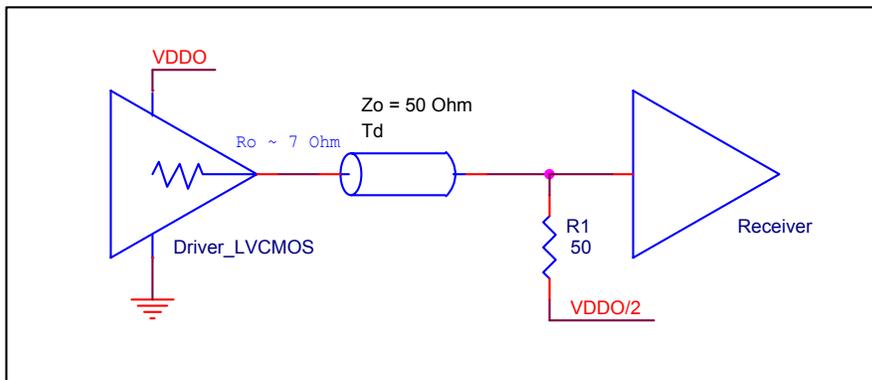


Figure 1 LVCMOS Driver Standard Termination

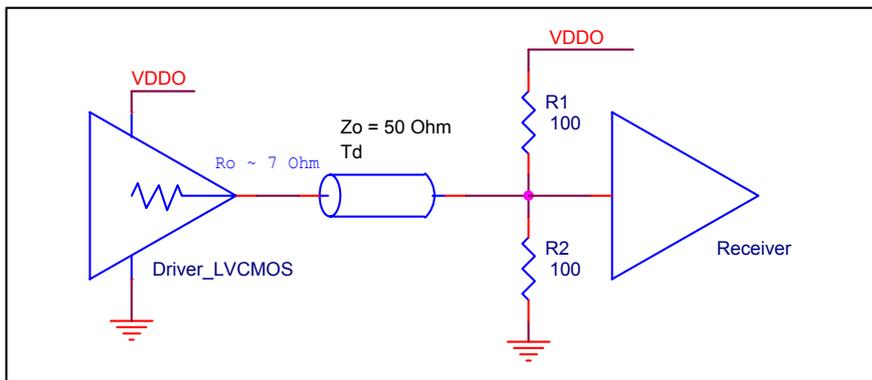


Figure 2 LVCMOS Parallel Termination

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### AC Termination

The LVCMOS driver AC termination in a 50-ohm transmission line environment is shown in Figure 3. The majority of load current is drawn during transient region (i.e. rising edge and falling edge). This termination consumes less power than the parallel termination. The proper value of capacitor C1 depends on the trace delay and capacitance of the transmission line. Some software tools such as Hyperlynx provides a feature of calculating the transmission line capacitance by entering the trace information [1].

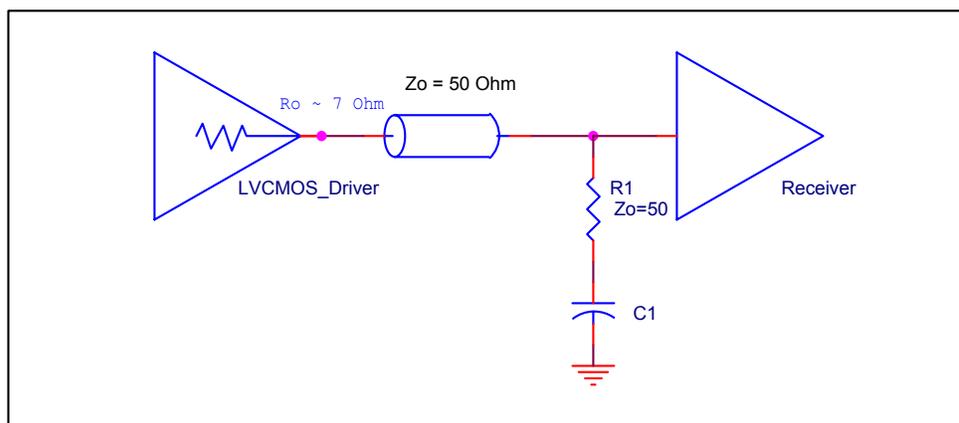


Figure 3 AC Termination

### Series Termination

Series termination is a popular termination scheme for LVCMOS drivers. Figure 4 shows a simple series termination for LVCMOS drivers with output impedance of 7 Ohm. The Power Dissipation of this termination scheme is described in a separate document.

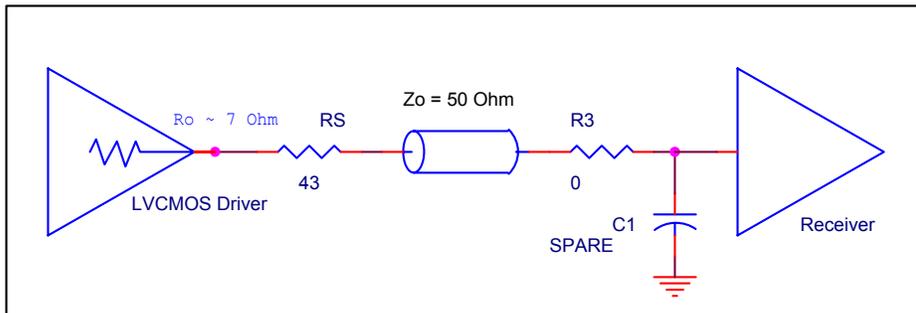
The typical output impedance  $R_O$  of a HiPerClockS™ LVCMOS driver is approximately 7 ohms. (Some parts might have different  $R_O$  value. Refer to data sheet for the output impedance). The closest series resistor value,  $R_S$ , can be calculated as follows

$$R_S = Z_O - R_O = 43 \text{ ohms}$$

In the Figure 4, the footprint for optional series resistor R3 or optional capacitor C1 at the receiver input is recommend for adjusting edge rate or overshoot if necessary.

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**Figure 4 One to One LVCMOS Series Termination**

When the number of drivers is not equal to number of receivers as shown in Figure 6, the series resistor value  $R_S$  is calculated as follows:

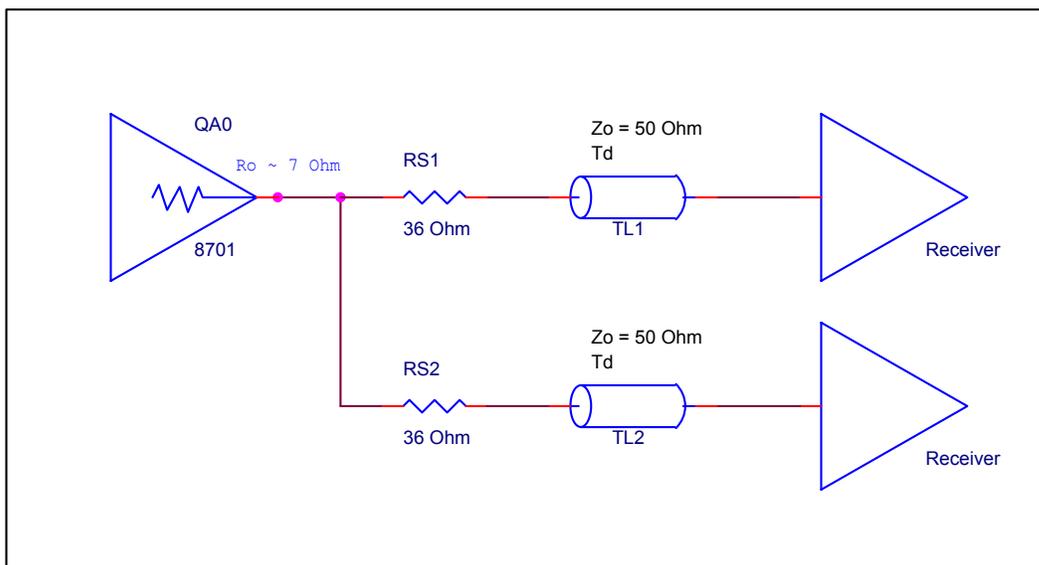
$$R_S = Z_0 - (R_O \times M)/(N)$$

Number of driver = N

Number of receiver = M

This configuration assumes that all the trace delays and load conditions are equally matched.

For example, one driver driving 2 receivers as shown in Figure 5, with  $N=1$  and  $M=2$ , the series resistor is calculated to be  $R_S = 36$  Ohms. The trace delays  $T_d$  on TL1 are equal. The loading conditions on both receivers should also be equal.



**Figure 5 Series Termination for one LVCMOS Driver Driving Two Receiver**

For 5 drivers driving 6 receivers, the closest series resistor can be calculated as follows:

$$N=5, M=6, Z_0=50 \text{ Ohms}, R_O = 7 \text{ Ohm}$$

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$$R_s = 50 - (7 \times 6)/5 = 41.6 \text{ Ohm}$$

The result above is straight from calculations. The closest available resistor value should be chosen.

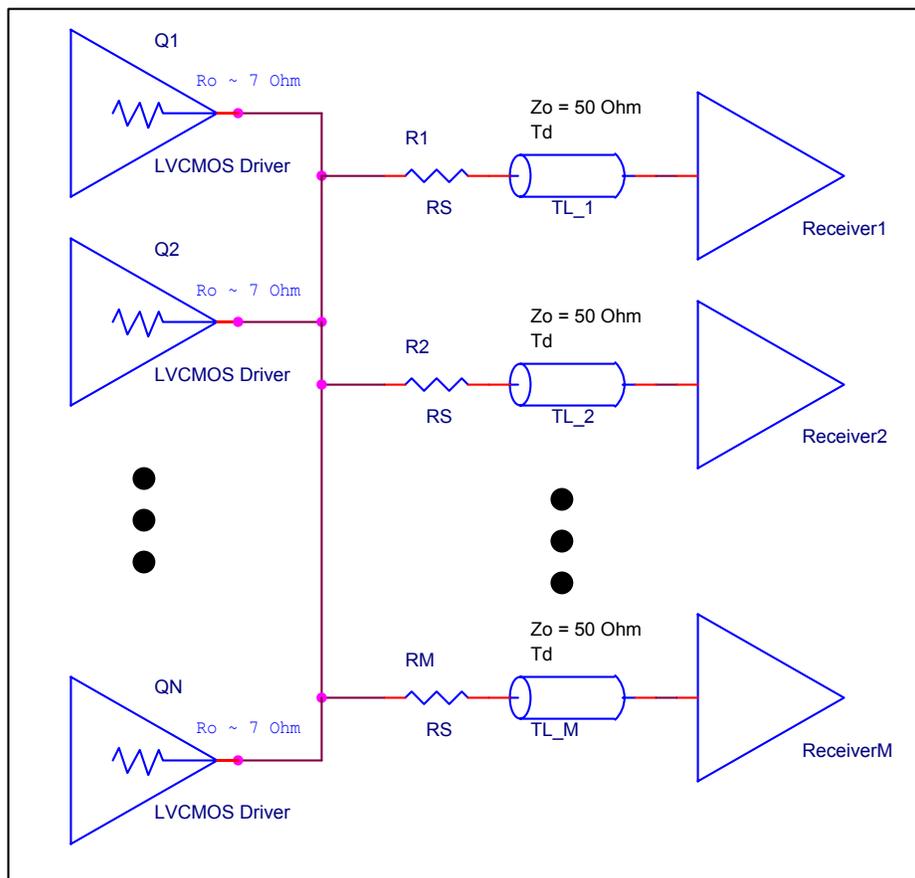


Figure 6 Tie N Outputs together to drive M receivers

### PC Board Layout With Option of Multi Termination Schemes

For signal integrity, take the necessary precaution and follow the high-speed digital design rules as much as possible. In most cases, the board design cannot fully comply the high-speed design rules due to constraints on the board environment, e.g. space available, cost etc. There is always some unknown parameters or interference in the system environment. The signal quality can only be optimized through the experiment during prototype phase. One termination scheme may work better than the other. While capturing a schematic for PC Board layout, if there is space available, it is recommended to provide options to choose different termination schemes on the prototype board. Figure 7 shows an example schematic for a PC board footprint that provides an option of choosing various types of terminations.

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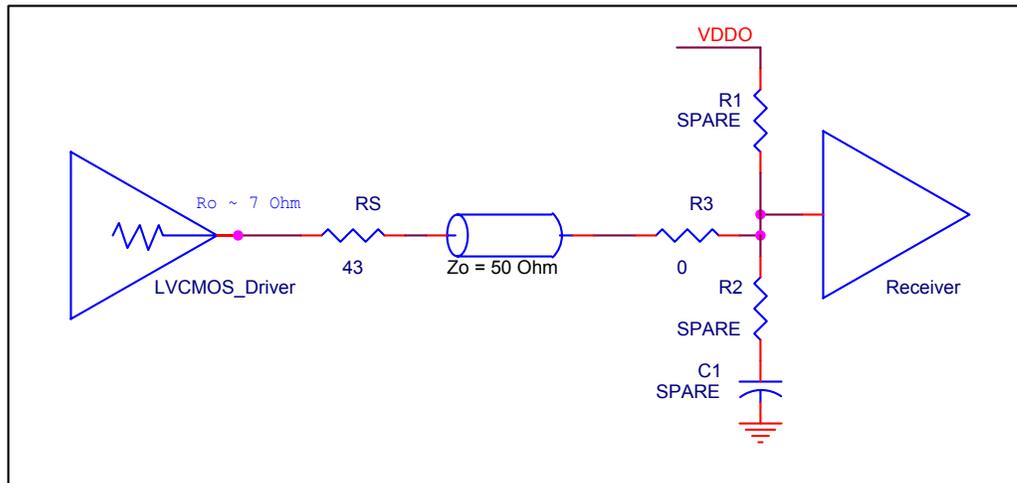


Figure 7 P.C. Board layout provides footprint to choose various termination options

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### References:

- [1] Kaufer, Steve, Crisafulli, Kellee, Terminating Trace on High-Speed PCBs, Printed Circuit Design, March 1998
- [2] Dr. Johnson, Howard, Dr. Graham, Martin, High-Speed Digital Design, A Handbook of Black Magic, Prentice Hall, 1993

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