To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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H8SX Family

Multiple-Bit Shifting

Introduction

This application note describes the multiple-bit shift function, which is one enhancement to the instruction set for the H8SX family relative to the set for the H8S.

Target Devices

H8SX family

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1. Overview ....................................................................................................................... 2
2. Applicable Conditions ................................................................................................. 2
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1. **Overview**

The H8SX CPU used in H8SX-family products is a 32-bit CPU having an architecture that maintains upward compatibility with the H8/300, H8/300H, and H8S CPUs, and an instruction set that has been strengthened for better CPU performance. This leads to greatly improved code efficiency relative to the earlier series. This improved code efficiency reduces the amount of space that programs take up in ROM and the number of instruction-fetching cycles in program execution.

In the H8SX CPU, instructions for bit shift operations incorporate the capability of shifting by 1, 2, 4, 8, or 16 bits. This is one way to realize programs that take up less space in ROM and requires less time for instruction fetching. This application note describes this enhancement to the instruction set, i.e., the availability of the multiple-bit shift function.

2. **Applicable Conditions**

<table>
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<th>Table 1</th>
<th>Applicable Conditions</th>
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<td>Item</td>
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<td>Development tool</td>
<td>High-performance Embedded Workshop Version 4.00.03</td>
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<td>C/C++ compiler</td>
<td>H8S, H8/300 Series C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)</td>
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<td>H8S compiler options</td>
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<td>Address</td>
<td>Section Name</td>
</tr>
<tr>
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<td>P</td>
</tr>
<tr>
<td>H'FF2000</td>
<td>B</td>
</tr>
</tbody>
</table>
3. Configuration

The earlier H8/300, H8/300H, and H8S CPUs provide bit shift instructions for only 1- and 2-bit shift operations. In contrast, the H8SX CPU has additional 2-byte-code instructions for 1-, 2-, 4-, 8-, and 16-bit shift operations and 4-byte-code instructions for up to 32-bit shift operations. For example, with the earlier H8S CPU, an 8-bit shift operation is done by repeating a 2-bit shift instruction four times. With the H8SX CPU, however, the same operation is achieved with a single 8-bit shift instruction. This is illustrated in figure 1.

Shift the value in the R0 register left by eight bits.

```
11111110 00000000
```

8-bit shift left

```
00000000 11111111
```

### Table

<table>
<thead>
<tr>
<th>Shift Operation with the H8S CPU</th>
<th>Shift Operation with the H8SX CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHLL.W #2, R0</td>
<td>SHLL.W #8, R0</td>
</tr>
<tr>
<td>SHLL.W #2, R0</td>
<td></td>
</tr>
<tr>
<td>SHLL.W #2, R0</td>
<td></td>
</tr>
<tr>
<td>SHLL.W #2, R0</td>
<td></td>
</tr>
</tbody>
</table>

Figure 1  Example: 8-Bit Shifting
4. Sample Program

4.1 Flowchart

This sample program is intended to convey an understanding of the multiple-bit shift function, one way in which the H8SX instruction set has been enhanced relative to that of the H8S. Shown below is a flowchart of the sample program, which performs right and left shift operations.

```
Start

lwDst[0] ← lwSrc[0] shifted right by 28 bits


```

Note: * The results of compilation given in the following pages are to allow comparison with the H8S CPU. However, the results of compiling actual application programs will vary significantly with the source program and conditions of compilation. Therefore, the results of compilation in this application note are only for reference.
4.2 Program Listing

A listing of the sample program in the C programming language is shown below. The results of compilation for the H8S CPU and H8SX CPU are given in section 4.3.

```c
/*****************************
/*  Application Note      */
*****************************
#include "machine.h"

/*****************************
/* RAM allocation          */
*****************************
unsigned long lwSrc[8];  /* Shift data */
unsigned long lwDst[8];  /* Execute data shifting*/

/*****************************
/* function prototype       */
*****************************
void main ( void );

/*****************************
/*  Vector Address           */
*****************************
#pragma entry main(sp=0xFFC000,vect=0) /* H'0000 : Reset */
#pragma section /* P */
/*****************************
/*  Main Program             */
*****************************
void main ( void )
{
    unsigned char i;
    for ( i = 0; i < 8; i++ ) {
        lwSrc[i] = 0x12345678;
    }

    lwDst[0] = lwSrc[0]>>28; /* 28-bit right shift */

    while(1);
}
```
4.3 Results of Compilation

4.3.1 Results for the H8S CPU

The assembly code is shown below.

```
00000000 _main: ; function: main
00000000     MOV.L       #H'00FFC000,SP
00000006     MOV.B       #8:8,R3L
00000008     SUB.L       ER2,ER2
0000000A     MOV.L       #H'12345678,ER1
00000010 L23:     MOV.L       ER2,ER0
00000012     SHLL.L      #2,ER0
00000014     MOV.L       ER1,@(_lsrc:32,ER0)
00000016     INC.L       #1,ER2
00000018     DEC.B       R3L
0000001A     BNE         L23:8
00000024     MOV.L       #_lsrc,ER2
00000026     MOV.L       @ER2,ER1
00000028     MOV.W       E1,R0
0000002A     MOV.B       R0H,R0L
0000002C     SUB.B       R0H,R0H
0000002E     SUB.W       E0,E0
00000030     SHLR.L      #2,ER0
00000032     SHLR.L      #2,ER0
00000034     MOV.L       #_ldst,ER3
00000036     MOV.L       ER0,@ER3
00000038     MOV.L       @(4:16,ER2),ER0
0000003A     MOV.W       E0,R0
0000003C     SUB.W       E0,E0
0000003E     SHLR.L      #2,ER0
00000040     SHLR.L      #2,ER0
00000042     SHLR.L      #2,ER0
00000044     SHLR.L      #2,ER0
00000046     SHLR.L      #2,ER0
00000048     SHLR.L      #2,ER0
0000004A     SHLR.L      #2,ER0
0000004C     SHLR.L      #2,ER0
0000004E     SHLR.L      #2,ER0
00000050     SHLR.L      #2,ER0
00000052     MOV.L       ER0,@(4:16,ER3)
00000054     MOV.L       @0:16,ER0,ER0
00000056     MOV.L       E0,R0
00000058     MOV.L       @0:16,ER2,ER0
0000005A     SHLR.L      #2,ER0
0000005C     SHLR.L      #2,ER0
0000005E     SHLR.L      #2,ER0
00000060     SHLR.L      #2,ER0
00000062     SHLR.L      #2,ER0
00000064     SHLR.L      #2,ER0
00000066     SHLR.L      #2,ER0
00000068     SHLR.L      #2,ER0
0000006A     MOV.L       ER0,@(8:16,ER3)
0000006C     MOV.L       @0:16,ER2,ER0
0000006E     SHLR.L      #2,ER0
00000070     SHLR.L      #2,ER0
00000072     MOV.L       ER0,@(H'000C:16,ER3)
00000074     MOV.L       @0:16,ER2,ER0
00000076     SHLR.L      #2,ER0
00000078     SHLR.L      #2,ER0
0000007A     MOV.L       ER0,@(H'000C:16,ER3)
0000007C     MOV.L       @0:16,ER2,ER0
0000007E     SHLR.L      #2,ER0
00000080     SHLR.L      #2,ER0
00000082     MOV.L       ER0,@(H'0010:16,ER3)
00000084     MOV.L       @0:16,ER2,ER0
00000086     SHLR.L      #2,ER0
00000088     SHLR.L      #2,ER0
0000008A     MOV.L       ER0,@(H'0010:16,ER3)
```
00000090    MOV.L @(H'0014:16,ER2),ER0
00000096    SHLL.L #2,ER0
00000098    SHLL.L #2,ER0
0000009A    SHLL.L #2,ER0
0000009C    SHLL.L #2,ER0
0000009E    SHLL.L #2,ER0
000000A0    SHLL.L #2,ER0
000000A2    MOV.L ER0,@(H'0014:16,ER3)
000000A8    MOV.L @(H'0018:16,ER2),ER0
000000AE    MOV.W R0,E0
000000B0    SUB.W R0,R0
000000B2    SHLL.L #2,ER0
000000B4    SHLL.L #2,ER0
000000B6    MOV.L ER0,@(H'0018:16,ER3)
000000BC    MOV.L @(H'001C:16,ER2),ER1
000000C2    MOV.W R1,R0
000000C4    MOV.B R0L,R0H
000000C6    SUB.B R0L,R0L
000000C8    MOV.W R0,E0
000000CA    SUB.B R0H,R0H
000000CC    SHLL.L #2,ER0
000000CE    SHLL.L #2,ER0
000000D0    MOV.L ER0,@(H'001C:16,ER3)
000000D6    L25:
            BRA L25:8

B

00000000   _lsrc:          ; section
            .RES.L 8
00000000   _ldst:          ; static: lsrc
            .RES.L 8
00000020   _ldst:          ; static: ldst
00000020   .RES.L 8
$VECT0     ; section

00000000   .DATA.L _main
4.3.2 Results for the H8SX CPU

The assembly code is shown below.

```
00000000 _main:                               ; function: main
00000000     MOV.L       #H'00FFC000,SP
00000006     MOV.B       #8:8,R1L
00000008     SUB.L       ER0,ER0
0000000A L23:                                  
0000000A     MOV.L       #H'12345678:32,@(_lsrc:32,ER0.L)
00000016     INC.L       #1,ER0
00000018     DEC.B       R1L
0000001A     BNE         L23:8
0000001C     MOV.L       #_lsrc,ER1
00000022     MOV.L       @ER1,ER0
00000026     SHLR.L      #28:5,ER0
0000002A     MOV.L       #_ldst,ER2
00000030     MOV.L       ER0,@ER2
00000034     MOV.L       @(4:2,ER1),ER0
00000038     SHLR.L      #20:5,ER0
0000003C     MOV.L       ER0,@(4:2,ER2)
00000040     MOV.L       @(8:2,ER1),ER0
00000044     SHLR.L      #12:5,ER0
00000048     MOV.L       ER0,@(8:2,ER2)
0000004C     MOV.L       @(12:2,ER1),ER0
00000050     SHLR.L      #4,ER0
00000052     MOV.L       ER0,@(12:2,ER2)
00000056     MOV.L       @(H'0010:16,ER1),ER0
0000005C     SHLR.L      #4,ER0
0000005E     MOV.L       ER0,@(H'0010:16,ER2)
00000064     MOV.L       @(H'0014:16,ER1),ER0
0000006A     SHLR.L      #12:5,ER0
0000006E     MOV.L       ER0,@(H'0014:16,ER2)
00000074     MOV.L       @(H'0018:16,ER1),ER0
0000007A     SHLR.L      #20:5,ER0
0000007E     MOV.L       ER0,@(H'0018:16,ER2)
00000084     MOV.L       @(H'001C:16,ER1),ER0
0000008A     SHLR.L      #28:5,ER0
0000008E     MOV.L       ER0,@(H'001C:16,ER2)
00000094 L25:                                  
00000094     BRA         L25:8

B                                               ; section
00000000 _lsrc:                               ; static: lsrc
00000000     .RES.L      8
00000020 _ldst:                                ; static: ldst
00000020     .RES.L      8
$VECT0                                         ; section
00000000 .DATA.L     _main
```
### 4.4 Comparison of the Results of Compilation

The portions of the compilation results of the right shift processing for the H8S CPU and H8SX CPU are shown in tables 3 and 4, respectively. As shown in the tables, a single instruction enables the right shift processing with the H8SX CPU, reducing the total length of the instructions from 36 to 14 bytes and the execution time from 18 to 11 cycles.

#### Table 3 Results for the H8S CPU

<table>
<thead>
<tr>
<th>Number of Bits Shifted Right</th>
<th>Assembly Code</th>
<th>Instruction Length (Bytes)</th>
<th>Execution Time (Number of Cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>MOV.W E1,R0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>MOV.B R0H,R0L</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SUB.B R0H,R0H</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SUB.W E0,E0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SHLR.L #2,ER0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SHLR.L #2,ER0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>20</td>
<td>MOV.W E0,R0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SUB.W E0,E0</td>
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<tr>
<td></td>
<td>SHLR.L #2,ER0</td>
<td>2</td>
<td>1</td>
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<tr>
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<td>SHLR.L #2,ER0</td>
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<td>1</td>
</tr>
<tr>
<td>12</td>
<td>SHLR.L #2,ER0</td>
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<td>1</td>
</tr>
<tr>
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<td>SHLR.L #2,ER0</td>
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<td>1</td>
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<td>1</td>
</tr>
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<td>SHLR.L #2,ER0</td>
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<td>1</td>
</tr>
<tr>
<td></td>
<td>SHLR.L #2,ER0</td>
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<td>1</td>
</tr>
<tr>
<td>Total</td>
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<td>36</td>
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#### Table 4 Results for the H8SX CPU

<table>
<thead>
<tr>
<th>Number of Bits Shifted Right</th>
<th>Assembly Code</th>
<th>Instruction Length (Bytes)</th>
<th>Execution Time (Number of Cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>SHLR.L #28:5,ER0</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>20</td>
<td>SHLR.L #20:5,ER0</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>SHLR.L #12:5,ER0</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>SHLR.L #4,ER0</td>
<td>2</td>
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<td>Total</td>
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