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Renesas Electronics Corporation

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H8/300H Tiny Series

Multi-Interrupt Operation with Internal Interrupts

Introduction

Both timer A and timer V interrupts are handled.

Target Device

H8/3664

Contents

1. Specifications

- Both timer A and timer V interrupts are handled.
- The priority level of the timer V interrupt request is set higher than that of the timer A interrupt request by software so that it is possible to accept timer V interrupt requests during the timer A interrupt handling.
- A timer A interrupt request is set to be generated every 32.768 ms by the interval timing function of timer A.
- A timer V interrupt request is set to be generated every 2.048 ms by the interval timing function of timer A.
- The LED is connected to the P74 output pin of port 7.

2. Description of Functions Used

In this sample task, multi-interrupt operation of the timer A and V interrupts are performed by internal interrupts.

The internal interrupts are described below.

- Each on-chip peripheral module has a flag to show the interrupt request status and an enable bit to enable or disable the interrupt. For timer A interrupt requests and direct transfer interrupt requests that are generated by execution of a SLEEP instruction, this function is included in interrupt request register 1 (IRR1) and interrupt enable register 1 (IENR1). When an on-chip peripheral module requests an interrupt, the corresponding interrupt request status flag is set to 1, requesting the CPU of an interrupt. These interrupts can be masked by writing 0 to clear the corresponding enable bit.
- All interrupts can be masked by setting the I bit in the condition code register (CCR) to 1.
- Interrupt operation is described as follows.
  1. If an interrupt occurs while the corresponding bit in the interrupt enable register is set to 1, an interrupt request signal is sent to the interrupt controller.
  2. On receiving the interrupt request signal, the corresponding interrupt request status flag is set to 1, requesting the CPU of an interrupt.
  3. When multiple interrupt requests are generated, the interrupt controller requests to the CPU for the interrupt handling with the highest priority at that time. Other interrupt requests are held pending.
  4. The CPU checks the I bit setting in CCR. If the I bit is cleared to 0, the interrupt request is accepted. If the I bit is set to 1, the interrupt request is held pending.
  5. If the CPU accepts the interrupt, after processing of the current instruction is completed, interrupt handling will begin. First, both the PC and CCR are pushed onto the stack. The PC value pushed onto the stack is the address of the first instruction to be executed upon return from interrupt handling.
  6. The I bit in CCR is set to 1 to mask further interrupts.
  7. The CPU generates the vector address corresponding to the accepted interrupt, and transfers the address to PC as a start address of the interrupt handling routine. Then a program starts executing from the address indicated in PC.

- When disabling interrupts by clearing bits in IENR1 or IRR1, always do so while interrupts are masked (I bit is set to 1). If the above clear operations are performed while the I bit is cleared to 0, and as a result a conflict arises between the clear instruction and an interrupt request, exception handling for the interrupt will be executed after the clear instruction has been executed.
- The timer A and timer V interrupt cycles in this sample task are calculated by the following equations:

$$\text{Timer A interrupt cycle} = \frac{1}{\text{System clock}/2048} \times 256$$

$$32.768\ \text{ms} = \frac{1}{16\ \text{MHz}/2048} \times 256$$

$$\text{Timer V interrupt cycle} = 2 \times \frac{1}{\text{System clock}/64} \times 256$$

$$2.048\ \text{ms} = 2 \times \frac{1}{16\ \text{MHz}/64} \times 256$$

Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated to perform multi-interrupt operation with internal interrupts.

Table 1 Function Allocation

Function	Description
OVIE	Enables interrupt requests by OVF in TSRW
IENTA	Enables timer A interrupt requests
OVF	Indicates whether or not a TCNTV overflow interrupt request is issued
IRRTA	Indicates whether or not a timer A interrupt request is issued
I bit in CCR	Enables or disables all interrupt requests
P74	LED output pin

3. Description of Operations

Figure 1 shows this sample task's principle of operation. The hardware and software processing shown in figure 1 performs multi-interrupt operation with internal interrupts.

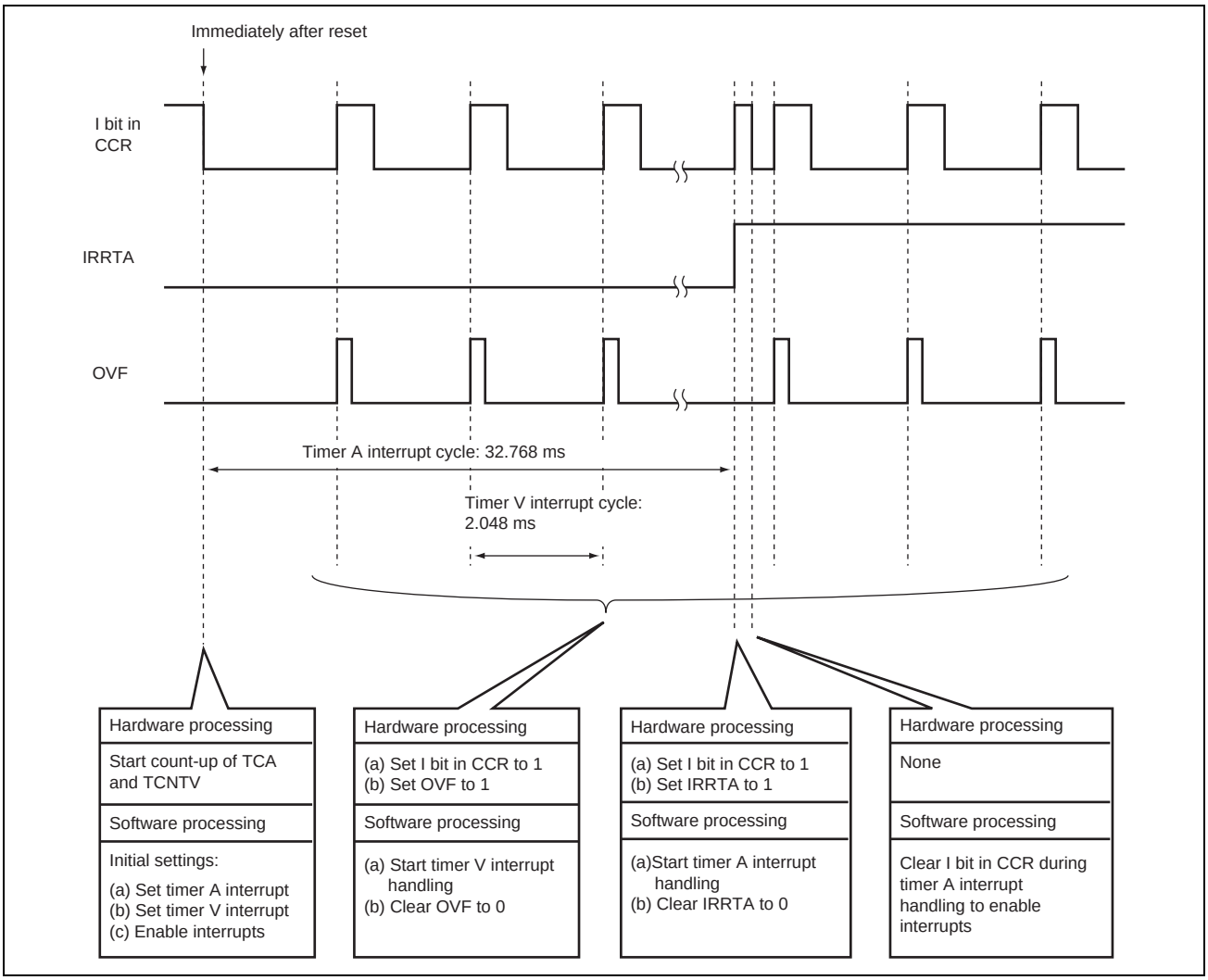


Figure 1 Operation Principle: Multi-Interrupt Operation with Internal Interrupts

4. Description of Software

4.1 Description of Modules

Table 2 describes the software used in this sample task.

Table 2 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets timer A interrupts, timer V interrupts, and port 7, and enables interrupts.
Count	taint	During the timer A interrupt handling routine, enables interrupts, increments the 16-bit counter, and ends TCNT when H'4000 is reached.
LED control	tvint	During the timer V interrupt handling routine, turns on/off the LED.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 3 describes the internal registers used in this sample task.

Table 3 Description of Internal Registers

Register	Name	Function	Address	Setting
TCRV0	OVIE	Timer control register V0 (timer overflow interrupt enable): When OVIE is set to 1, TNCTV overflow interrupts are enabled.	H'FFA0 Bit 5	 0
		Timer control register V0 (clock select 2 to 0):	H'FFA0	
	CKS2	When CKS2 is cleared to 0 and CKS1, CKS0, and ICKS0 are all set to 1, TCNTV is incremented at the falling edge of system clock/64.	Bit 2	CKS2 = 0
	CKS1		Bit 1	CKS1 = 1
	CKS0		Bit 0	CKS0 = 1
TCSRV	OVF	Timer control/status register V (timer overflow flag): When OVF is cleared to 0, a TCNTV overflow interrupt is not requested. When OVF is set to 1, a TCNTV overflow interrupt is requested.	H'FFA1 Bit 5	 0
TNCTV		Timer counter V: 8-bit up-counter incremented by clock input of system clock/64	H'FFA4	H'00

Table 3 Description of Internal Registers (cont)

Register	Name	Function	Address	Setting
TCRV1	ICKS0	Timer control register V1 (internal clock select 0): Selects the TCNTV clock source, together with bits CK2 to CK0 in TCRV0.	H'FFA5 Bit 0	 0
TMA		Timer mode register A: When TMA is set to H'12, timer A is set to the interval timing function, the TCA input clock source to PSS, and the prescaler division ratio to division by 2048.	H'FFA6	H'12
TCA		Timer counter A: Incrementing the 8-bit counter using clock input of system clock/2048.	H'FFA7	H'00
PDR7	P74	Port data register 7 (port data register 74): When P74 is cleared to 0, the P74 pin output level is low. When P74 is set to 1, the P74 pin output level is high.	H'FFDA Bit 4	 0
PCR7	PCR74	Port control register 7 (port control register 74): When PCR74 is set to 1, the P74 pin functions as an output pin.	H'FFEA Bit 4	 1
IENR1	IENTA	Interrupt enable register 1 (timer A interrupt enable): When IENTA is set to 1, timer A interrupt requests are enabled.	H'FFF4 Bit 6	 1
IRR1	IRRTA	Interrupt request register 1 (timer A interrupt request flag): When IRRTA is cleared to 0, no timer A interrupt is requested. When IRRTA is set to 1, a timer A interrupt is requested.	H'FFF6 Bit 6	 0

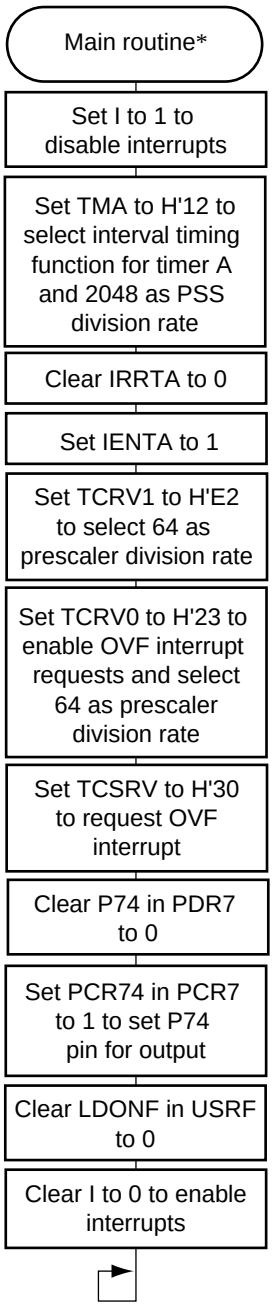
4.4 Description of RAM

Table 4 describes the RAM used in this sample task.

Table 4 Description of RAM

Label	Name	Function	Address	Used in
counter_sub		16-bit counter for counting up to H'4000 in an interrupt routine (timer A)	H'FB80	Interrupt routine Timer A
USRF	LDONF	Flag for judging on/off of the LED	H'FB82 Bit 0	LED control

5. Flowcharts



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 2 Flowchart for Main Routine

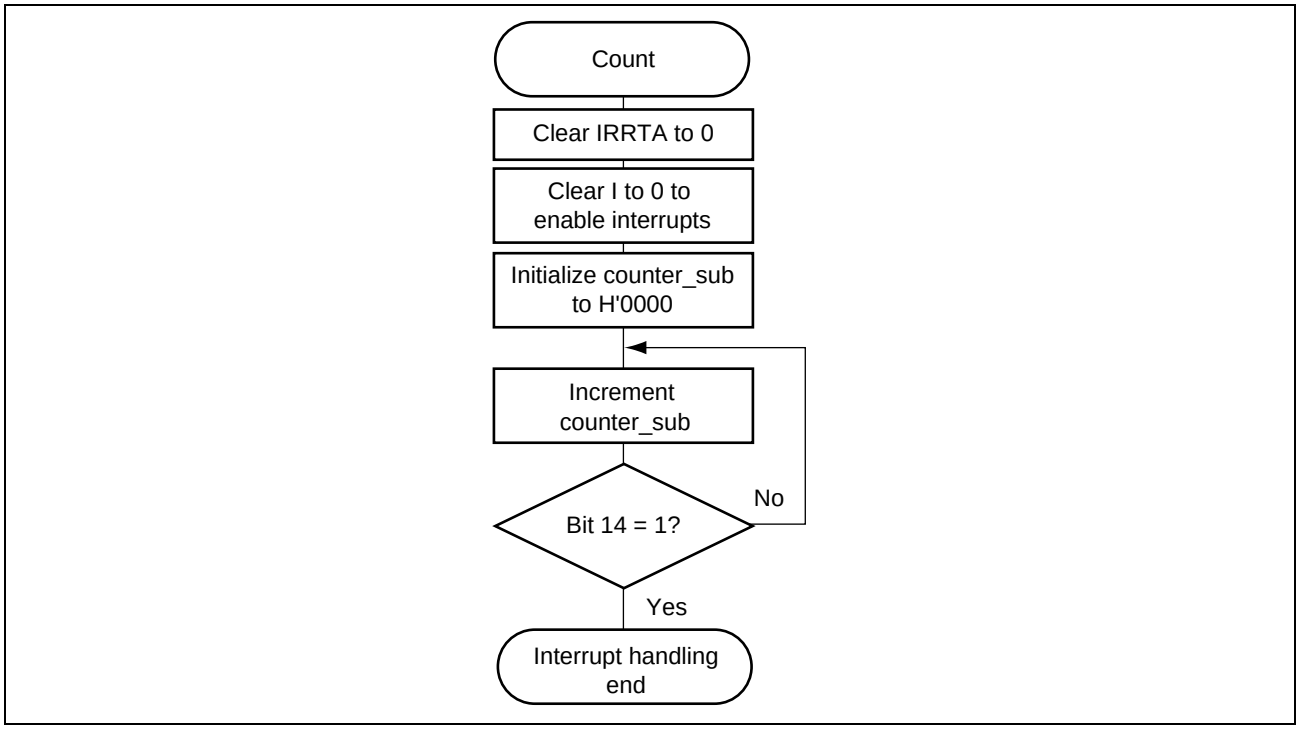


Figure 3 Flowchart for Timer A Interrupt Handling Routine

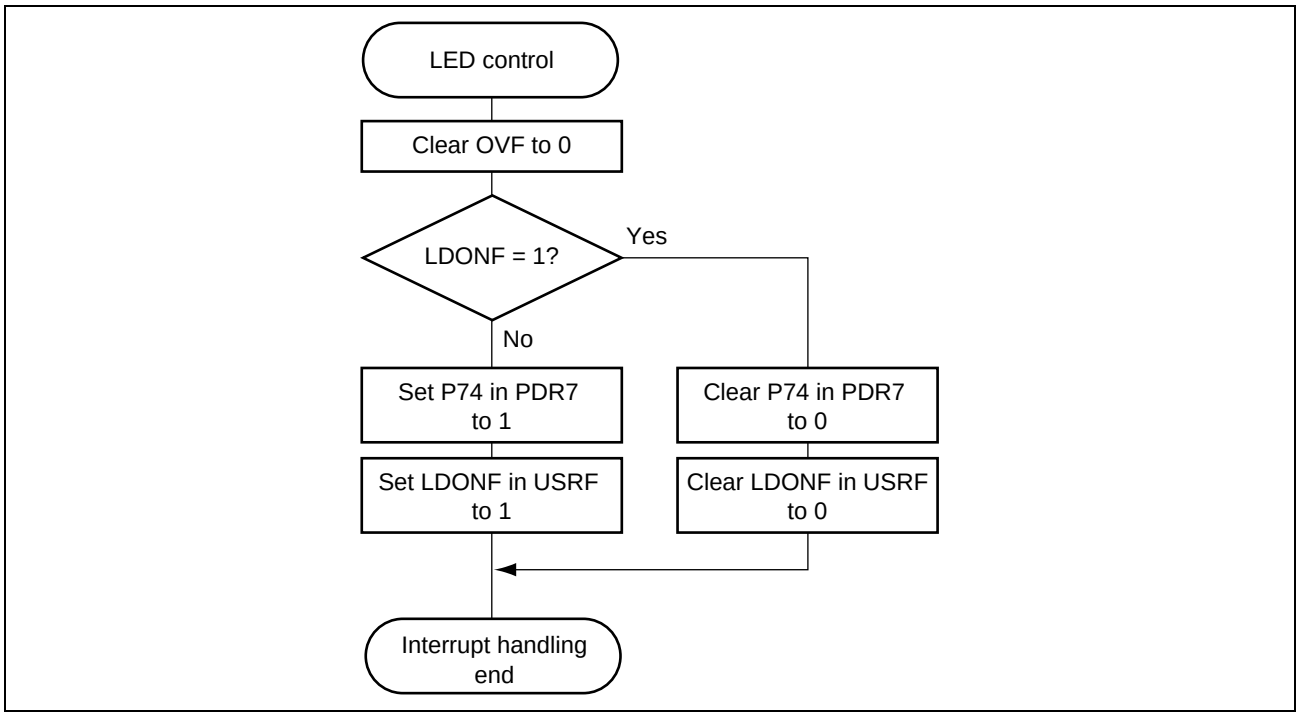


Figure 4 Flowchart for Timer V Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'Multiple Interrupt Operation by Internal             */
/*     Interrupt'                                           */
/*                                                          */
/*    Function                                              */
/*    : Internal Interrupt                                  */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>
```

```
/************************************************************/
/*  Symbol Defnition    */
/************************************************************/
struct BIT {
    unsigned char       b7:1;                   /* bit7                                         */
    unsigned char       b6:1;                   /* bit6                                         */
    unsigned char       b5:1;                   /* bit5                                         */
    unsigned char       b4:1;                   /* bit4                                         */
    unsigned char       b3:1;                   /* bit3                                         */
    unsigned char       b2:1;                   /* bit2                                         */
    unsigned char       b1:1;                   /* bit1                                         */
    unsigned char       b0:1;                   /* bit0                                         */
};

#define    TCRV0        *(volatile unsigned char *)0xFFA0                                        /*
Timer Contorol Register V0                          */
#define    TCSRV        *(volatile unsigned char *)0xFFA1                                        /*
Timer Control/Status Register V                     */
#define    TCSRV_BIT    (*(struct BIT *)0xFFA1)    /* Timer Control/Status Register V          */
#define    OVF          TCSRV_BIT.b5               /* Timer Overflow Flag                      */
#define    TCNTV        *(volatile unsigned char *)0xFFA4                                        /*
Timer Counter V         */
#define    TCRV1        *(volatile unsigned char *)0xFFA5                                        /*
Timer Contorol Register V1                          */
#define    TMA          *(volatile unsigned char *)0xFFA6                                        /*
Timer Mode Register A   */
#define    TCA          *(volatile unsigned char *)0xFFA7                                        /*
Timer Counter A         */
#define    PDR7_BIT     (*(struct BIT *)0xFFDA)    /* Port Data Register 7                     */
#define    P74          PDR7_BIT.b4                /* Port Data Register 7 bit4                */
#define    PCR7_BIT     (*(struct BIT *)0xFFEA)    /* Port Control Register 7                  */
#define    PCR74        PCR7_BIT.b4                /* Port Control Register 7 bit4             */
#define    IENR1_BIT    (*(struct BIT *)0xFFF4)    /* Interrupt Enable Register 1              */
#define    IENTA        IENR1_BIT.b6               /* Timer A Interrupt Enable                 */
#define    IEN0         IENR1_BIT.b0               /* IRQ0 Interrupt Enable                    */
#define    IRR1_BIT     (*(struct BIT *)0xFFF6)    /* Interrupt Request Register 1             */
#define    IRRTA        IRR1_BIT.b6                /* Timer A Interrupt Request Flag           */
#define    IRRI0        IRR1_BIT.b0                /* IRQ0 Interrupt Request Flag              */
#define    PMR1_BIT     (*(struct BIT *)0xFFE0)    /* Port Mode Register 1                     */
#define    IRQ0_SET     PMR1_BIT.b4                /* Port Mode Register 1 bit4                */
#define    TMOW         PMR1_BIT.b0                /* P10/TMOW Terminal Function Change        */
#define    IEGR1_BIT    (*(struct BIT *)0xFFF2)    /* Interrupt Edge Select Register 1         */
#define    IEG0         IEGR1_BIT.b0               /* IRQ0 Edge Select                         */
#pragma    interrupt    (taint)
#pragma    interrupt    (tvint)
```

```
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern     void INIT     ( void );                /* SP Set                                  */
void main   ( void );
void taint  ( void );
void tvint  ( void );

/************************************************************/
/*    RAM define                                            */
/************************************************************/
unsigned int             counter_sub;
unsigned char            USRF;                    /* User Flag Erea                          */

#define    USRF_BIT      (*(struct BIT *)&USRF)
#define    LDONF         USRF_BIT.b0              /* LED On Flag                             */

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section       V1                       /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL1[])(void) = {
    INIT                                          /* 00 Reset                                */
};
#pragma    section       V2                       /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL2[])(void) = {
    taint  /* 26 Timer A  Interrupt                */
};
#pragma    section       V3                       /* VECTOR SECTOIN SET                      */
void (*const VEC_TBL3[])(void) = {
    tvint                                         /* 2C Timer V  Interrupt                   */
};

#pragma    section                                /* P                                       */
```

```
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void main   ( void )
{

    set_imask_ccr(1);                           /* Interrupt Disable                                    */

    TMA = 0x12;                                 /* Initialize TMA Function & TCA Input Clock Period     */

    IRRTA = 0;                                  /* Clear IRRTA                                          */

    IENTA = 1;                                  /* Timer A Interrupt Enable                             */

    TCRV1 = 0xE2;                               /* Initialize Time Control Register    V1               */
    TCRV0 = 0x23;                               /* Initialize TCRV0 Function & TCRV0 Input Clock Period */
    TCSRV = 0x30;                               /* Initialize Timer Control/Status Register V           */

    P74 = 0;                                    /* Clear P74                                            */
    PCR74 = 1;                                  /* Initialize P74 Output Terminal                       */

    LDONF = 0;                                  /* Clear LDONF                                          */

    set_imask_ccr(0);                           /* Interrupt Enable                                     */

    while(1){
           ;
    }
}

/************************************************************/
/*    Timer A Interrupt                                     */
/************************************************************/
void taint  ( void )
{

    IRRTA = 0;                                  /* Clear IRRTA                                          */

    set_imask_ccr(0);                           /* Interrupt Enable                                     */

    counter_sub = 0x0000;                       /* Initialize 16bit Counter                             */

    do{
    counter_sub++;      /* Increment 16bit Counter */
    }while((counter_sub & 0x4000) == 0);        /* 16bit Counter bit14 = 1 ?                            */

}
```

```
/************************************************************/
/*    Timer V Interrupt                                     */
/************************************************************/
void tvint  ( void )
{

    OVF = 0;

    if(LDONF == 1){                          /* LDONF = 1 ?                                    */
           P74 = 0;                          /* Turn off LED                                   */
           LDONF = 0;                        /* Clear LDONF                                    */
    }
           else{
                       P74 = 1;              /* urn on LED                                     */
                       LDONF = 1;            /* Set LDONF                                      */
           }

}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'0026
CV3	H'002C
P	H'0100
B	H'FB80

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
2.00	Sep.01.06	All pages	Format has been changed from Hitachi version to Renesas version.

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