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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series
Multi-Interrupt Operation with Internal Interrupts

Introduction
Both timer A and timer V interrupts are handled.

Target Device
H8/3664

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1. Specifications

- Both timer A and timer V interrupts are handled.
- The priority level of the timer V interrupt request is set higher than that of the timer A interrupt request by software so that it is possible to accept timer V interrupt requests during the timer A interrupt handling.
- A timer A interrupt request is set to be generated every 32.768 ms by the interval timing function of timer A.
- A timer V interrupt request is set to be generated every 2.048 ms by the interval timing function of timer A.
- The LED is connected to the P74 output pin of port 7.

2. Description of Functions Used

In this sample task, multi-interrupt operation of the timer A and V interrupts are performed by internal interrupts.

The internal interrupts are described below.

- Each on-chip peripheral module has a flag to show the interrupt request status and an enable bit to enable or disable the interrupt. For timer A interrupt requests and direct transfer interrupt requests that are generated by execution of a SLEEP instruction, this function is included in interrupt request register 1 (IRR1) and interrupt enable register 1 (IENR1). When an on-chip peripheral module requests an interrupt, the corresponding interrupt request status flag is set to 1, requesting the CPU of an interrupt. These interrupts can be masked by writing 0 to clear the corresponding enable bit.
- All interrupts can be masked by setting the I bit in the condition code register (CCR) to 1.
- Interrupt operation is described as follows.
  1. If an interrupt occurs while the corresponding bit in the interrupt enable register is set to 1, an interrupt request signal is sent to the interrupt controller.
  2. On receiving the interrupt request signal, the corresponding interrupt request status flag is set to 1, requesting the CPU of an interrupt.
  3. When multiple interrupt requests are generated, the interrupt controller requests to the CPU for the interrupt handling with the highest priority at that time. Other interrupt requests are held pending.
  4. The CPU checks the I bit setting in CCR. If the I bit is cleared to 0, the interrupt request is accepted. If the I bit is set to 1, the interrupt request is held pending.
  5. If the CPU accepts the interrupt, after processing of the current instruction is completed, interrupt handling will begin. First, both the PC and CCR are pushed onto the stack. The PC value pushed onto the stack is the address of the first instruction to be executed upon return from interrupt handling.
  6. The I bit in CCR is set to 1 to mask further interrupts.
  7. The CPU generates the vector address corresponding to the accepted interrupt, and transfers the address to PC as a start address of the interrupt handling routine. Then a program starts executing from the address indicated in PC.
When disabling interrupts by clearing bits in IENR1 or IRR1, always do so while interrupts are masked (I bit is set to 1). If the above clear operations are performed while the I bit is cleared to 0, and as a result a conflict arises between the clear instruction and an interrupt request, exception handling for the interrupt will be executed after the clear instruction has been executed.

The timer A and timer V interrupt cycles in this sample task are calculated by the following equations:

\[
\text{Timer A interrupt cycle} = \frac{1}{\text{System clock/2048}} \times 256
\]

\[
32.768 \text{ ms} = \frac{1}{16 \text{ MHz/2048}} \times 256
\]

\[
\text{Timer V interrupt cycle} = 2 \times \frac{1}{\text{System clock/64}} \times 256
\]

\[
2.048 \text{ ms} = 2 \times \frac{1}{16 \text{ MHz/64}} \times 256
\]

Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated to perform multi-interrupt operation with internal interrupts.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OVIE</td>
<td>Enables interrupt requests by OVF in TSRW</td>
</tr>
<tr>
<td>IENTA</td>
<td>Enables timer A interrupt requests</td>
</tr>
<tr>
<td>OVF</td>
<td>Indicates whether or not a TCNTV overflow interrupt request is issued</td>
</tr>
<tr>
<td>IRRTA</td>
<td>Indicates whether or not a timer A interrupt request is issued</td>
</tr>
<tr>
<td>I bit in CCR</td>
<td>Enables or disables all interrupt requests</td>
</tr>
<tr>
<td>P74</td>
<td>LED output pin</td>
</tr>
</tbody>
</table>
3. Description of Operations

Figure 1 shows this sample task's principle of operation. The hardware and software processing shown in figure 1 performs multi-interrupt operation with internal interrupts.

![Operation Principle: Multi-Interrupt Operation with Internal Interrupts](image)

Figure 1  Operation Principle: Multi-Interrupt Operation with Internal Interrupts
4. Description of Software

4.1 Description of Modules

Table 2 describes the software used in this sample task.

Table 2 Description of Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Sets timer A interrupts, timer V interrupts, and port 7, and enables interrupts.</td>
</tr>
<tr>
<td>Count</td>
<td>taint</td>
<td>During the timer A interrupt handling routine, enables interrupts, increments the 16-bit counter, and ends TCNT when H'4000 is reached.</td>
</tr>
<tr>
<td>LED control</td>
<td>tvint</td>
<td>During the timer V interrupt handling routine, turns on/off the LED.</td>
</tr>
</tbody>
</table>

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 3 describes the internal registers used in this sample task.

Table 3 Description of Internal Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCRV0</td>
<td>Timer control register V0 (timer overflow interrupt enable):</td>
<td>H'FFA0</td>
<td>Bit 5</td>
</tr>
<tr>
<td></td>
<td>When OVIE is set to 1, TCNTV overflow interrupts are enabled.</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Timer control register V0 (clock select 2 to 0):</td>
<td>H'FFA0</td>
<td>Bit 2</td>
</tr>
<tr>
<td>CKS2</td>
<td>When CKS2 is cleared to 0 and CKS1, CKS0, and ICKS0 are all set to 1,</td>
<td></td>
<td>CKS2 = 0</td>
</tr>
<tr>
<td></td>
<td>TCNTV is incremented at the falling edge of system clock/64.</td>
<td></td>
<td>CKS1 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CKS0 = 1</td>
</tr>
<tr>
<td>TCSRv</td>
<td>Timer control/status register V (timer overflow flag):</td>
<td>H'FFA1</td>
<td>Bit 5</td>
</tr>
<tr>
<td></td>
<td>When OVF is cleared to 0, a TCNTV overflow interrupt is not requested.</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>When OVF is set to 1, a TCNTV overflow interrupt is requested.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TNCTV</td>
<td>Timer counter V:</td>
<td>H'FFA4</td>
<td>H'00</td>
</tr>
<tr>
<td></td>
<td>8-bit up-counter incremented by clock input of system clock/64</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 3  Description of Internal Registers (cont)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCRV1</td>
<td>ICKS0 Timer control register V1 (internal clock select 0): Selects the TCNTV clock source, together with bits CK2 to CK0 in TCRV0.</td>
<td>H'FFA5</td>
<td>0</td>
</tr>
<tr>
<td>TMA</td>
<td>Timer mode register A: When TMA is set to H'12, timer A is set to the interval timing function, the TCA input clock source to PSS, and the prescaler division ratio to division by 2048.</td>
<td>H'FFA6</td>
<td>H'12</td>
</tr>
<tr>
<td>TCA</td>
<td>Timer counter A: Incrementing the 8-bit counter using clock input of system clock/2048.</td>
<td>H'FFA7</td>
<td>H'00</td>
</tr>
<tr>
<td>PDR7</td>
<td>P74 Port data register 7 (port data register 74): When P74 is cleared to 0, the P74 pin output level is low. When P74 is set to 1, the P74 pin output level is high.</td>
<td>H'FFDA</td>
<td>0</td>
</tr>
<tr>
<td>PCR7</td>
<td>PCR74 Port control register 7 (port control register 74): When PCR74 is set to 1, the P74 pin functions as an output pin.</td>
<td>H'FFEA</td>
<td>1</td>
</tr>
<tr>
<td>IENR1</td>
<td>IENTA Interrupt enable register 1 (timer A interrupt enable): When IENTA is set to 1, timer A interrupt requests are enabled.</td>
<td>H'FFFF</td>
<td>1</td>
</tr>
<tr>
<td>IRR1</td>
<td>IRTA Interrupt request register 1 (timer A interrupt request flag): When IRTA is cleared to 0, no timer A interrupt is requested. When IRTA is set to 1, a timer A interrupt is requested.</td>
<td>H'FFFF</td>
<td>0</td>
</tr>
</tbody>
</table>

4.4 Description of RAM

Table 4 describes the RAM used in this sample task.

Table 4  Description of RAM

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function</th>
<th>Address</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>counter_sub</td>
<td>16-bit counter for counting up to H'4000 in an interrupt routine (timer A)</td>
<td>H'FB80</td>
<td>Interrupt routine Timer A</td>
</tr>
<tr>
<td>USRF</td>
<td>LDONF Flag for judging on/off of the LED</td>
<td>H'FB82</td>
<td>LED control</td>
</tr>
<tr>
<td></td>
<td>Bit 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5. Flowcharts

Figure 2   Flowchart for Main Routine

Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).
Clear IRRTA to 0

Increment counter_sub

Bit 14 = 1?

Count

Yes

No

Interrupt handling end

Figure 3  Flowchart for Timer A Interrupt Handling Routine

Clear OVF to 0

LDONF = 1?

LED control

Yes

No

Set P74 in PDR7 to 1

Clear P74 in PDR7 to 0

Set LDONF in USRF to 1

Clear LDONF in USRF to 0

Interrupt handling end

Figure 4  Flowchart for Timer V Interrupt Handling Routine
6. Program Listing

INIT.SRC (Program listing)

```assembly
.EXPORT  _INIT
.IMPORT  _main
;
.SECTION  P,CODE
_INIT:
    MOV.W  #H'FF80, R7
    LDC.B  #B'10000000, CCR
    JMP   @_main
;
.END

/*******************************************************************************/
/*
 /* H8/300H Tiny Series -H8/3664-  */
 /* Application Note */
 /* 'Multiple Interrupt Operation by Internal */
 /* Interrupt' */
 /* */
 /* Function */
 /* : Internal Interrupt */
 /* */
 /* External Clock : 16MHz */
 /* Internal Clock : 16MHz */
 /* Sub Clock : 32.768kHz */
/*
/********************************************************************************/

#include <machine.h>
```
/************************************************************/
/* Symbol Definition */
/************************************************************/

struct BIT {
    unsigned char b7:1; /* bit7 */
    unsigned char b6:1; /* bit6 */
    unsigned char b5:1; /* bit5 */
    unsigned char b4:1; /* bit4 */
    unsigned char b3:1; /* bit3 */
    unsigned char b2:1; /* bit2 */
    unsigned char b1:1; /* bit1 */
    unsigned char b0:1; /* bit0 */
};

#define TCRV0 *(volatile unsigned char *)0xFFA0 /* Timer Control Register V0 */
#define TCSRV *(volatile unsigned char *)0xFFA1 /* Timer Control/Status Register V */
#define TCSRV_BIT (*(struct BIT *)0xFFA1 /* Timer Control/Status Register V */
#define OVF TCSRV_BIT.b5 /* Timer Overflow Flag */
#define TCNTV *(volatile unsigned char *)0xFFA4 /* Timer Counter V */
#define TCRV1 *(volatile unsigned char *)0xFFA5 /* Timer Control Register V1 */
#define TMA *(volatile unsigned char *)0xFFA6 /* Timer Mode Register A */
#define TCA *(volatile unsigned char *)0xFFA7 /* Timer Counter A */
#define PDR7_BIT (*(struct BIT *)0xFFDA /* Port Data Register 7 */
#define P74 PDR7_BIT.b4 /* Port Data Register 7 bit4 */
#define PCR7_BIT (*(struct BIT *)0xFFEA /* Port Control Register 7 */
#define PCR74 PCR7_BIT.b4 /* Port Control Register 7 bit4 */
#define IENR1_BIT (*(struct BIT *)0xFFF4 /* Interrupt Enable Register 1 */
#define IENTA IENR1_BIT.b6 /* Timer A Interrupt Enable */
#define IEN0 IENR1_BIT.b0 /* IRQ0 Interrupt Enable */
#define IRR1_BIT (*(struct BIT *)0xFFF6 /* Interrupt Request Register 1 */
#define IRRTA IRR1_BIT.b6 /* Timer A Interrupt Request Flag */
#define IRR10 IRR1_BIT.b0 /* IRQ0 Interrupt Request Flag */
#define PMR1_BIT (*(struct BIT *)0xFFE0 /* Port Mode Register 1 */
#define IQRO_SET PMR1_BIT.b4 /* Port Mode Register 1 bit4 */
#define TMOW PMR1_BIT.b0 /* P10/TMOW Terminal Function Change */
#define IEGR1_BIT (*(struct BIT *)0xFFF2 /* Interrupt Edge Select Register 1 */
#define IEG0 IEGR1_BIT.b0 /* IRQ0 Edge Select */
#pragma interrupt (taint)
#pragma interrupt (tvint)
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern void INIT ( void ); /* SP Set */
void main ( void );
void taint ( void );
void tvint ( void );

/************************************************************/
/*    RAM define                                          */
/************************************************************/
unsigned int counter_sub;
unsigned char USRF; /* User Flag Erea */
#define USRF_BIT (*(struct BIT *)&USRF)
#define LDONF USRF_BIT.b0 /* LED On Flag */

/************************************************************/
/*    Vector Address                                       */
/************************************************************/
#pragma section V1 /* VECTOR SECTOIN SET */
void (*const VEC_TBL1[])(void) = {
    INIT /* 00 Reset */
};
#pragma section V2 /* VECTOR SECTOIN SET */
void (*const VEC_TBL2[])(void) = {
    taint /* 26 Timer A Interrupt */
};
#pragma section V3 /* VECTOR SECTOIN SET */
void (*const VEC_TBL3[])(void) = {
    tvint /* 2C Timer V Interrupt */
};
#pragma section P /* P */
/*******************************************************************************/
/* Main Program */
/*******************************************************************************/
void main ( void )
{
    set_imask_ccr(1);        /* Interrupt Disable */
    TMA = 0x12;              /* Initialize TMA Function & TCA Input Clock Period */
    IRRTA = 0;               /* Clear IRRTA */
    IENTA = 1;               /* Timer A Interrupt Enable */
    TCRV1 = 0xE2;            /* Initialize Time Control Register V1 */
    TCRV0 = 0x23;            /* Initialize TCRV0 Function & TCRV0 Input Clock Period */
    TCSRv = 0x30;            /* Initialize Timer Control/Status Register V */
    P74 = 0;                 /* Clear P74 */
    PCR74 = 1;               /* Initialize P74 Output Terminal */
    LDONF = 0;               /* Clear LDONF */
    set_imask_ccr(0);        /* Interrupt Enable */

    while(1){
        ;
    }
}

/*******************************************************************************/
/* Timer A Interrupt */
/*******************************************************************************/
void taint ( void )
{
    IRRTA = 0;                /* Clear IRRTA */

    set_imask_ccr(0);        /* Interrupt Enable */
    counter_sub = 0x0000;    /* Initialize 16bit Counter */

    do{
        counter_sub++;        /* Increment 16bit Counter */
    }while((counter_sub & 0x4000) == 0);    /* 16bit Counter bit14 = 1 ? */
}
/************************************************************/
/*    Timer V Interrupt                                      */
/************************************************************/
void tvint ( void )
{

    OVF = 0;

    if(LDONF == 1){  /* LDONF = 1 ? */
        P74 = 0;  /* Turn off LED */
        LDONF = 0;  /* Clear LDONF */
    }
    else{
        P74 = 1;  /* turn on LED */
        LDONF = 1;  /* Set LDONF */
    }
}

Link Address Setting:

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'0000</td>
</tr>
<tr>
<td>CV2</td>
<td>H'0026</td>
</tr>
<tr>
<td>CV3</td>
<td>H'002C</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
<tr>
<td>B</td>
<td>H'FB80</td>
</tr>
</tbody>
</table>
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