ClockMatrix
Multi-Clock Distribution using Timing Commander for FW4.9.1

When used with firmware 4.9.1 or higher, the ClockMatrix 8A34001 allows a system to distribute multiple timing channels on a single carrier by encoding asynchronous data onto the synchronous carrier clock. This mechanism for multi-clock distribution uses a PWM Frame to represent the synchronization data of a DPLL clock. A system can use this capability to encode the SETS (or synchronous Ethernet) clock onto the Time (PTP) clock, along with PTP 1PPS+ToD information.

This document outlines the steps needed to configure two separate ClockMatrix devices to send asynchronous information over a carrier using PWM.

Contents
1. Overview ............................................................................................................. 2
2. Timing Commander Setup .................................................................................. 2
   2.1 Input Configuration ......................................................................................... 2
   2.2 DPLL Configuration ....................................................................................... 2
   2.3 PWM Configuration ....................................................................................... 4
   2.4 Output Configuration ...................................................................................... 6
   2.5 Hitless Switching ......................................................................................... 6
3. Revision History .................................................................................................. 6

Figures
Figure 1. Setup of Asynchronous Data over PWM....................................................2
Figure 2. DPLL Master Divider ..............................................................................3
Figure 3. Transmitter Side DPLLS .........................................................................3
Figure 4. Receiver Side DPLLS and DPLL D FCW Configuration..........................3
Figure 5. PWM Encoder DPLL A .........................................................................4
Figure 6. ToD1 Accumulator Settings ..................................................................4
Figure 7. PWM Decoder DPLL C .........................................................................5
1. Overview

The ClockMatrix 8A34001 allows the distribution of multiple timing channels on a single carrier by encoding asynchronous data onto the synchronous carrier clock. This mechanism for multi-clock distribution uses a PWM Frame of data to represent the synchronization data of a DPLL clock. A system could use this feature, for example, to encode the SETS (or synchronous Ethernet) clock onto the Time (PTP) clock, along with PTP 1PPS+ToD information.

To use this feature, use Timing Commander GUI version 1.16.4 (or later) with ClockMatrix personality 9.1.1 (or later) and select firmware 4.9.1 for the 8A34001.

The 8A34001 needs its firmware updated after each power cycle. The new firmware can be loaded by the system software via the serial port or by the device from an I2C EEPROM. The application note, ClockMatrix Firmware Update through Serial Port and EEPROM v1.0, describes both methods of loading the firmware (see the 8A34001 product page for details). Figure 1 shows the setup used.

2. Timing Commander Setup

2.1 Input Configuration

2.1.1 Encoder (Transmitter)

The encoder has two external clock inputs: the carrier clock (in1) and the payload clock (in2). In Figure 1, the carrier clock has a frequency of 25MHz, whereas the payload clock has a frequency of 10MHz. The payload is the data/clock to be embedded onto the carrier clock.

2.1.2 Decoder (Receiver)

The decoder has only a single input, which is the modulated PWM signal (in3), coming from the transmitter.

2.2 DPLL Configuration

All four DPLLs being used must be configured to have the same master divider value as shown in Figure 2. This requirement applies to the DPLLs in the encoder and decoder of the ClockMatrix devices.
2.2.1. Encoder
The encoder uses two DPLLS to configure the encoding. DPLL A uses the carrier clock (in1) as its input (PWM DPLL), whereas DPLL B uses the payload clock (in2) as its input (Payload DPLL). Both DPLLS use the system DPLL as a combo source as shown in Figure 3.

2.2.2. Decoder
The decoder uses two DPLLS to configure the decoding. DPLL C uses the modulated PWM signal (in3) as its input, whereas DPLL D has no input and is configured as **Write Frequency Input**. DPLL D also uses DPLL C as a combo source (no SysDPLL). This allows DPLL D to regenerate the payload clock from the PWM signal coming in at DPLL C. DPLL C uses the system DPLL as a combo source. The receiver DPLLS and the DPLL D Write Frequency Input configuration are shown in Figure 4.
2.3 PWM Configuration

2.3.1 Encoder

The PWM encoder and PWM_SYNC (Async) must be enabled for DPLL A. Enabling Async allows asynchronous message transmission by PWM through this carrier channel. Encoder 1 is chosen as displayed in Figure 5 because Channel 1 is selected as the PWM Encoder. Also, notice that the trigger for the Q2 carrier is the ToD1 accumulator. The ToD1 accumulator settings are shown in Figure 6.

![Figure 5. PWM Encoder DPLL A](image)

At the time of this document's completion, the Async button (far right) is not available in the diagram view as shown above but can be found in the Bit Sets view as shown below. It is called:

- PWM_SYNC'A'_ENCODER_CMD_PWM_SYNC (0xCD82 bit [0])

![PWM1 Encoder Cmd Sync TX (PWM1_ENCODER_CMD_SYNC_TX)](image)

Other settings must be enabled via the Bit Sets in order to enable the asynchronous data mode:

- PWM'A' Encoder Sync Payload Channel 'B' TX Enable
  - PWM1_ENCODER_SYNC_PAYLOAD_CH_2_EN (0xCD84 bit [2])
- PWM'A' Encoder Sync Payload Channel 'B' TX Squelch
  - PWM1_ENCODER_SYNC_PAYLOAD_2_SQUELCH (0xCD85 bit [2])

In our example, Channel 1 is DPLL A and Channel 2 is DPLL B in the transmitter.

![PWM1 Encoder Sync Payload Channel 2 TX Enable and Squelch](image)

The settings in Figure 6 are the ToD1 Accumulator settings.

![Figure 6. ToD1 Accumulator Settings](image)
2.3.2. Decoder

The PWM decoder and PWM_SYNC (Async) must be enabled for DPLL C. Enabling Async notifies the decoder that the PWM messages it receives are asynchronous as shown in Figure 7. Decoder 3 is chosen because the input to DPLL C is CLK3.

![PWM Decoder DPLL C](image)

At the time of this document's completion, the Async button (far right) is not available in the diagram view as shown above but can be found in the Bit Sets view as shown below. It is called:

- PWM'in3'DECODER_CMD_PWM_SYNC (0xCE16 bit [0])

Other settings must be enabled via the Bit Sets in order to enable the asynchronous data mode:

- PWM'in3'Decoder Sync Payload Channel 'D' Enable
  - PWM3_DECODER_SYNC_PAYLOAD_CH_2_EN (0xCE13 bit [3])
- PWM'in3'Decoder Sync Payload Channel 'D' Source Channel Index
  - PWM3_DECODER_SYNC_PAYLOAD_SRC_INDEX_2 (0xCE13 bits [2:0])
- PWM'in3'Decoder Sync Carrier Index
  - PWM3_DECODER_SYNC_CARRIER_INDEX (0xCE16 bits [4:1])

In our example, Channel 1 is DPLL C and Channel 2 is DPLL D in the receiver.
2.4 Output Configuration

2.4.1. Encoder
The encoder has two clock outputs: the carrier clock modulated with the payload clock (out1) and the payload clock (out2). In Figure 1, the modulated clock has a carrier frequency of 25MHz, whereas the payload clock has a frequency of 10MHz. Out1 is sent to the receiver to be demodulated and Out2 is used as an observable output.

2.4.2. Decoder
The decoder has two clock outputs: the demodulated carrier clock (out3) and the payload clock (out4). In Figure 1, the demodulated carrier clock has a carrier frequency of 25MHz, whereas the payload clock has a frequency of 10MHz. Out4 should be a match to Out2.

2.5 Hitless Switching
When the hitless switch capabilities need to be tested between two asynchronous clock sources, unique decoder and encoder IDs must be configured for each encoder and decoder.

3. Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>May 21, 2021</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas’ products are provided only subject to Renesas’ Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.