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SH7137 Group

MTU2: Output of Complementary Pairs of PWM Signals in Three Phases
(Complementary PWM Mode)

Introduction
This application note describes an example of setting up multi-function timer pulse unit 2 (MTU2) for the output of complementary pulse width modulation (PWM) waveforms in three phases with a non-overlapping relationship between states of the positive and inverse signals.

Target Device
SH7137

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1. Preface ........................................................................................................................2
2. Description of the Sample Application ......................................................................3
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1. Preface

1.1 Specifications

The sample program employs MTU2 in complementary PWM mode for the three-phase output of complementary PWM waveforms. Figure 1 shows an overview.

1. Channels 3 and 4 of MTU2 are used to make settings for complementary PWM mode (complementary PWM mode 3). The output pins for the positive PWM signals are TIOC3B, TIOC4A, and TIOC4B. The corresponding inverse signals are output on pins TIOC3D, TIOC4C, and TIOC4D. The low level is selected as active for PWM output.
2. For both the positive and inverse signals, MTU2 outputs PWM waveforms with a dead time (interval for preventing short-circuits) in which the state transitions of the positive and inverse signals do not overlap. The duration of the dead time is set to 4 μs.
3. PWM carrier cycle is set to 400 μs.
4. The PWM duty cycle is incremented or decremented by an interrupt signal generated every PWM cycle.
5. Waveforms are output by toggling the level on the TIOC3A pin in synchronization with half cycles of the PWM carrier.

![Figure 1 Three-Phase Output of Complementary PWM (Complementary PWM Mode 3)](image)

1.2 Module Used

Channels 3 and 4 of MTU2

1.3 Applicable Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>SH7137 [R5F7137]</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>Internal clock: Iφ = 80 MHz</td>
</tr>
<tr>
<td></td>
<td>Bus clock: Bφ = 40 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral clock: Pφ = 40 MHz</td>
</tr>
<tr>
<td></td>
<td>MTU2S clock: MPφ = 40 MHz</td>
</tr>
<tr>
<td></td>
<td>AD clock: MIφ = 80 MHz</td>
</tr>
<tr>
<td>MCU operating mode</td>
<td>Single-chip</td>
</tr>
<tr>
<td>Compiler</td>
<td>SuperH RISC engine C/C++ Compiler Ver.9.02.00 from Renesas Technology</td>
</tr>
<tr>
<td>C compiler options</td>
<td>Default settings of the C compiler</td>
</tr>
</tbody>
</table>
2. Description of the Sample Application

In this sample program, MTU2 is used in complementary PWM mode.

2.1 Operational Overview of Module Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

MTU2 is a multi-functional timer unit that has six 16-bit timer channels. Settings for compare-match function, input-capture function, etc. can be made for each channel. Settings for complementary PWM mode and reset-synchronized PWM mode are made for channels 3 and 4, enabling the control of six PWM output lines.

For details on MTU2, see the section on MTU2 in the SH7137 Group Hardware Manual (REJ09B0402).

Table 2 gives an overview of MTU2 and figure 2 is a block diagram of MTU2.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>16-bit timer × 6 channels (channels 0 to 5)</td>
</tr>
<tr>
<td>Counter clock</td>
<td>The clock signal for counter input can be selected from among 8 different input clock signals (except for channel 5, with only 4 different clock signals available).</td>
</tr>
</tbody>
</table>
| Operation of channels 0 to 5 | • Waveform output on compare match  
• Input capture function  
• Counter clearing  
• Simultaneous writing to multiple timer counters (TCNT)  
• Simultaneous clearing by compare match and input capture  
• Input to and output from registers are synchronized with counter operation.  
• PWM output in up to 12 phases in combination with synchronous operation |
| Triggers for A/D converter | • A/D converter start trigger can be generated.  
• In complementary PWM mode, interrupts at the crest and trough of the counter value and A/D converter start triggers can be skipped. |
| Buffered operation | • Settings for buffered operation of registers can be made to channels 0, 3, and 4. |
| Operating modes | • Settings for PWM mode can be made on channels 0 to 4.  
• Settings for phase counting mode can be set for each of channels 1 and 2 individually.  
• Waveform output in a total of six phases, including the positive and inverse signals for three phases, is possible in reset-synchronized PWM mode or complementary PWM mode. |
| Interrupt requests | • 28 different interrupt sources  
(interrupt generation by compare match, input capture, etc.) |
| Others | • Cascade-connection operation  
• High-speed access by internal 16-bit bus  
• Automatic transfer of register data is enabled.  
• Module standby mode can be set.  
• Dead time compensation counter is available in channel 5. |
MTU2: Output of Complementary Pairs of PWM Signals in Three Phases
(Complementary PWM Mode)

Input/output pins
Channel 3: TIOC3A
TIOC3B
TIOC3C
TIOC3D
Channel 4: TIOC4A
TIOC4B
TIOC4C
TIOC4D

Input pins
Channel 5: TIC5U
TIC5V
TIC5W

Clock input
Internal clock: MPφ/1
MPφ/4
MPφ/16
MPφ/64
MPφ/256
MPφ/1024
External clock: TCLKA
TCLKB
TCLKC
TCLKD

Input/output pins
Channel 1: TIOC1A
TIOC1B
Channel 2: TIOC2A
TIOC2B
Channel 3: TIOC3A
TIOC3B
TIOC3C
TIOC3D
Channel 4: TIOC4A
TIOC4B
TIOC4C
TIOC4D
Channel 5: TIOC5U
TIOC5V
TIOC5W

Interrupt request signals
Channel 0: TGIA_0
TGIB_0
TGIC_0
TGID_0
TGIE_0
TGIF_0
TCIV_0
Channel 1: TGIA_1
TGIB_1
TCIV_1
TCIU_1
Channel 2: TGIA_2
TGIB_2
TCIV_2
TCIU_2
Channel 3: TGIA_3
TGIB_3
TGIC_3
TGID_3
TCIV_3
TCIU_3
Channel 4: TGIA_4
TGIB_4
TGIC_4
TGID_4
TCIV_4
TCIU_4
Channel 5: TGIA_5
TGIB_5
TGIC_5
TGID_5
TCIV_5

Input/output pins
Channel 0: TIOC0A
TIOC0B
TIOC0C
TIOC0D
Channel 1: TIOC1A
TIOC1B
Channel 2: TIOC2A
TIOC2B
Channel 3: TIOC3A
TIOC3B
TIOC3C
TIOC3D
Channel 4: TIOC4A
TIOC4B
TIOC4C
TIOC4D
Channel 5: TIOC5U
TIOC5V
TIOC5W

Internal data bus
TCR
TIOR
TSR
TIER

[Legend]
TSTR: Timer start register
TSYR: Timer synchronous register
TCR: Timer control register
TMDR: Timer mode register
TGRP: Timer control register
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRG: Timer general register G
TGRH: Timer general register H
TGRJ: Timer general register I
TGRL: Timer general register L
TGRC: Timer general register M
TGRR: Timer general register N
TGRI: Timer general register O
TGRJ: Timer general register P
TGRK: Timer general register Q
TGRM: Timer general register R
TGRN: Timer general register S
TGRP: Timer general register T
TGRQ: Timer general register U
TGRS: Timer general register V
TGRT: Timer general register W
TGRA: Timer general register X
TGRB: Timer general register Y
TGRC: Timer general register Z
TGRD: Timer general register AA
TGRE: Timer general register AB
TGRF: Timer general register AC
TGRG: Timer general register AD
TGRH: Timer general register AE
TGRJ: Timer general register AF
TGRK: Timer general register AG
TGRM: Timer general register AH
TGRN: Timer general register AI
TGRP: Timer general register AJ
TGRQ: Timer general register AK
TGRS: Timer general register AL
TGRT: Timer general register AM

Figure 2  Block Diagram of MTU2
2.1.2 Complementary PWM Mode

Setting for complementary PWM mode can be made by the combination of channels 3 and 4 of MTU2. In complementary PWM mode, PWM waveforms are output in three phases with a non-overlapping relationship between the states of the positive and inverse signals. The output of PWM waveforms which do not have the non-overlapping time (interval for preventing short circuits) can also be set up. PWM output pins for complementary PWM mode are pins TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D. Furthermore, toggling of the output level in synchronization with the PWM cycle can be set up on the TIOC3A pin.

Figure 3 is a block diagram of channels 3 and 4 of MTU2 in complementary PWM mode.
The followings are register functions of channel 3 and 4 when complementary PWM mode is set.

- **Timer general register A_3 (TGRA_3)**
  TGRA_3 functions as a compare match register. The upper limit (1/2 carrier cycle + dead time) for counting is set here. Moreover, when the value in this register is changed during timer operation, the new value is that set in timer general register C_3 (TGRC_3).

- **Timer general register B_3 (TGRB_3)**
  TGRB_3 functions as a comparison register. The duty cycle of the PWM waveforms which are output from pins TIOC3B and TIOC3D is set by the values in this register. Moreover, when the value in this register is changed during timer operation, the new value is that set in timer general register D_3 (TGRD_3).

- **Timer general register C_3 (TGRC_3)**
  TGRC_3 functions as the buffer register for TGRA_3. During timer operation, the values set in this register are written to TGRA_3.

- **Timer general register D_3 (TGRD_3)**
  TGRD_3 functions as the buffer register for TGRB_3. During timer operation, the values set in this register are written to TGRB_3.

- **Timer general register A_4 (TGRA_4)**
  TGRA_4 functions as a comparison register. The duty cycle of PWM the waveforms which are output from pins TIOC4A and TIOC4C are set in this register. Moreover, when the value in this register is changed during timer operation, the value is that set in the timer general register C_4 (TGRC_4).

- **Timer general register B_4 (TGRB_4)**
  TGRB_4 functions as a comparison register. The duty cycle of the PWM waveforms which are output from pins TIOC4B and TIOC4D are set in this register. Moreover, when the value in this register is changed during timer operation, the value to be changed is set in the timer general register D_4 (TGRD_4).

- **Timer general register C_4 (TGRC_4)**
  TGRC_4 functions as a buffer register for TGRA_4. During timer operation, the values set in this register are written to TGRA_4.

- **Timer general register D_4 (TGRD_4)**
  TGRD_4 functions as a buffer register for TGRB_4. During timer operation, the values set in this register are written to TGRB_4.

- **Temporary registers 1, 2, and 3 (Temp1, 2, and 3)**
  Temporary registers 1, 2, and 3 are between the respective buffer and comparison registers. Data written in a buffer register are transferred to the corresponding temporary register and then to the comparison register. The temporary registers cannot be accessed by the CPU.

- **Timer counter _3 (TCNT_3)**
  TCNT_3 is a 16-bit counter. TCNT_3 decrementation on compare matches with TGRA_3, and incrementation on compare matches with the timer dead-time data register (TDDR).

- **Timer counter _4 (TCNT_4)**
  TCNT_4 is a 16-bit counter. TCNT_4 decrementation on compare matches with the timer cycle data register (TCDR), and incrementation when timer counting reaches H'0000.

- **Timer dead time data register (TDDR)**
  The TDDR is a 16-bit readable and writable register. The dead time for the PWM waveforms is set in this register.

- **Timer cycle data register (TCDR)**
  The TCDR is a 16-bit register. The setting in this register defines half of the cycle for the PWM carrier.

- **Timer cycle buffer register (TCBR)**
  The TCBR functions as the buffer register for the TCDR. During timer operation, the values set in this register are written to TCDR.
## 2.2 Operation of the Sample Program

### 2.2.1 Settings for Operation of the Sample Program

In this sample program, the output of complementary PWM waveforms in three phases on channels 3 and 4 of MTU2 is obtained by selecting complementary PWM mode 3. An output level is also toggled in synchronization with the PWM carrier cycle. Table 3 gives the setting conditions for operation in complementary PWM mode in this sample program. Figure 4 shows a sample of output waveforms in complementary PWM mode.

### Table 3 Setting for Operation in Complementary PWM Mode

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels in use</td>
<td>3 and 4</td>
</tr>
<tr>
<td>Operating mode</td>
<td>Complementary PWM mode 3 (data transfer at the crest and trough of the counter value)</td>
</tr>
<tr>
<td>Functions of pins</td>
<td>• TIOC3A pin: Output toggled in synchronization with the PWM cycle</td>
</tr>
<tr>
<td></td>
<td>• TIOC3B pin: PWM output 1 (positive waveform)</td>
</tr>
<tr>
<td></td>
<td>• TIOC3D pin: PWM output 1' (inverse waveform for PWM output 1)</td>
</tr>
<tr>
<td></td>
<td>• TIOC4A pin: PWM output 2 (positive waveform)</td>
</tr>
<tr>
<td></td>
<td>• TIOC4C pin: PWM output 2' (inverse waveform for PWM output 2)</td>
</tr>
<tr>
<td></td>
<td>• TIOC4B pin: PWM output 3 (positive waveform)</td>
</tr>
<tr>
<td></td>
<td>• TIOC4D pin: PWM output 3' (inverse waveform for PWM output 3)</td>
</tr>
<tr>
<td>Active level</td>
<td>• Output of positive signal: Active low</td>
</tr>
<tr>
<td></td>
<td>• Output of inverse signal: Active low</td>
</tr>
<tr>
<td>Counter clock</td>
<td>10 MHz (Obtained by dividing Pϕ clock frequency by 4)</td>
</tr>
<tr>
<td>PWM carrier cycle</td>
<td>400 μs (carrier frequency: 2.5 kHz)</td>
</tr>
<tr>
<td>Short-circuit prevention interval (dead time)</td>
<td>4 μs</td>
</tr>
<tr>
<td>PWM duty cycle</td>
<td>• Initial duty cycle for PWM outputs 1, 2, 3: 50%</td>
</tr>
<tr>
<td></td>
<td>PWM duty cycle value is updated every time the TGRA_3 interrupt is generated (setting is incremented or decremented).</td>
</tr>
<tr>
<td>Interrupt</td>
<td>• Compare match interrupt for TGRA_3</td>
</tr>
<tr>
<td></td>
<td>A TGRA_3 compare match is generated once per PWM-carrier cycle.</td>
</tr>
</tbody>
</table>

![Figure 4 Output Waveforms in Complementary PWM Mode Operation](image)

**Figure 4** Output Waveforms in Complementary PWM Mode Operation
2.2.2 Description of Operation by the Sample Program

1. Operation of Timer Counters

Figure 5 shows the operation of two timer counters in complementary PWM mode. Counters TCNT_3 and TCNT_4 of channels 3 and 4 count up and then down. The initial setting of the TCNT_3 counter is the same as the value set in the TDDR. The initial setting of the TCNT_4 counter is H’0000. Timer counting starts simultaneously on channels 3 and 4.

Figure 5   Operation of Timer Counters

2. PWM Waveform Output

The output of complementary PWM waveforms in three phases is controlled by timer counters (TCNT_3, TCNT_4) and comparison registers (TGRB_3, TGRA_4, TGRB_4). The counters for PWM output are constantly compared with the comparison registers (TGRB_3, TGRA_4, and TGRB_4). When the counter values match the values of these registers, the output levels of the positive and inverse PWM signals are switched according to the values of bits OLSN and OLSP in the timer output control register (TOCR).

Figure 6 shows the output signals (the positive and inverse phases) for a single complementary pair. The output signal of the positive and inverse phases is controlled by timer counters (TCNT_3, TCNT_4) and compare match registers.

Figure 6   Output of PWM Waveforms in Complementary PWM Mode
3. Changes to PWM Duty Cycle

Figure 7 shows the timing of updating values for the PWM duty cycle. In this sample program, the register settings for PWM duty cycle are incremented or decremented from the handler for a compare-match interrupt with TGRA_3 (that generated at the highest counter value). Changes to three buffer registers TGRD_3, TGRC_4, and TGRD_4 are used to increment or decrement the values of PWM duty cycle. When the duty cycle is changed, make sure that the last setting to be made is that for TRGR_4. Furthermore, if the value in TGRD_4 is neither incremented nor decremented, make sure that a value is written to TGRD_4 after the registers with values to be incremented or decremented have been updated.

![Figure 7 Timing of Updating the PWM Duty Cycle](image)

4. Output Toggling in Synchronization with the PWM Cycle

Figure 8 shows the operations for toggling of an output level in synchronization with the PWM cycle. The PSYE bit in the timer output control register (TOCR) is set to 1 to select toggling of an output in synchronization with the PWM carrier cycle. Toggling is of the signal on the TIOC3A pin. The initial value for output is 1.

![Figure 8 Operation for Toggling an Output in Synchronization with the PWM Cycle](image)
2.2.3  Examples of Output with Desired PWM Duty Cycles

Table 4 gives relations between register settings for PWM duty cycle and the behavior of the positive and inverse waveforms in one phase. In complementary PWM mode, when the value in a comparison register (TGRB_3, in this sample program) is H'0000, the positive output remains ON while the inverse output remains OFF; i.e. the output levels are fixed. Furthermore, when the value in the comparison register is greater than or equal to the value in the TGRA_3 register, the level of the positive signal is fixed to the OFF state while the level of the inverse signal is fixed to the ON state.

Figures 9 and 10 shows examples of output waveforms of the positive and inverse signals. When changing the PWM duty cycle, make sure that the values are set in the corresponding buffer registers rather than directly in the comparison registers and that changing comparison registers should be made via the buffer registers.

Table 4  Examples of Setting that Control the PWM Duty Cycle and Output Waveforms

<table>
<thead>
<tr>
<th>Value in TGRB_3</th>
<th>Positive output (TIOC3B pin)</th>
<th>Inverse output (TIOC3D pin)</th>
<th>Waveform Chart</th>
</tr>
</thead>
<tbody>
<tr>
<td>TGRB_3 ≥ TGRA_3</td>
<td>Fixed to the OFF state (high)</td>
<td>Fixed to the ON state (low)</td>
<td>Figure 9 (a)</td>
</tr>
<tr>
<td>Between TGRA_3 and TCDR</td>
<td>Fixed to the OFF state (high)</td>
<td>Output of the OFF waveform (pulse)</td>
<td>—</td>
</tr>
<tr>
<td>TGRB_3 = TCDR</td>
<td>Fixed to the OFF state (high)</td>
<td>Output of the OFF waveform (to be a pulse twice the width of the short-circuit prevention interval)</td>
<td>Figure 9 (b)</td>
</tr>
<tr>
<td>Between (TCDR – Td) and TCDR</td>
<td>Output of the ON waveform (pulse)</td>
<td>Output of the OFF waveform</td>
<td>—</td>
</tr>
<tr>
<td>TGRB_3 = (TCDR – Td)</td>
<td>Output of the ON waveform (to be a pulse twice the width of the short-circuit prevention interval)</td>
<td>Output of the OFF waveform (to be a pulse four times the width of the short-circuit prevention interval)</td>
<td>Figure 9 (c)</td>
</tr>
<tr>
<td>Between (TDDR × 2) and (TCDR – Td)</td>
<td>Output of complementary PWM waveforms</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>TGRB_3 = (TDDR × 2)</td>
<td>Output of the OFF waveform (to be a pulse four times the width of the short-circuit prevention interval)</td>
<td>Output of the ON waveform (to be a pulse twice the width of the short-circuit prevention interval)</td>
<td>Figure 10 (a)</td>
</tr>
<tr>
<td>Between TDDR and (TDDR × 2)</td>
<td>Output of the OFF waveform (pulse)</td>
<td>Output of the ON waveform</td>
<td>—</td>
</tr>
<tr>
<td>TGRB_3 = TDDR</td>
<td>Output of the OFF waveform (to be a pulse twice the width of the short-circuit prevention interval)</td>
<td>Fixed to the OFF state (high)</td>
<td>Figure 10 (b)</td>
</tr>
<tr>
<td>Between H'0000 and TDDR</td>
<td>Output of the OFF waveform (pulse)</td>
<td>Fixed to the OFF state (high)</td>
<td>—</td>
</tr>
<tr>
<td>TGRB_3 = H'0000</td>
<td>Fixed to the ON state (low)</td>
<td>Fixed to the OFF state (high)</td>
<td>Figure 10 (c)</td>
</tr>
</tbody>
</table>

Note: 1. The active level of the PWM output is set to low. The descriptions of the output waveforms refer to the positive and inverse signals for a single complementary pair.
Figure 9  Examples of PWM Waveform Output (1)
Figure 10  Examples of PWM Waveform Output (2)
2.3 Configuration of the Sample Program

2.3.1 Description of Functions
Table 5 lists functions used in this sample program.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Label</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main</td>
<td>main ()</td>
<td>Initializes other modules and makes settings for timers of MTU2</td>
</tr>
<tr>
<td>Standby setting</td>
<td>stbcr_init ()</td>
<td>Makes setting to release MTU2 from standby</td>
</tr>
<tr>
<td>Initialization of MTU2</td>
<td>mtu2_init ()</td>
<td>Initializes MTU2 (channels 3 and 4) Places channels 3 and 4 in complementary PWM mode 3</td>
</tr>
<tr>
<td>Initialization of PFC</td>
<td>pfc_init ()</td>
<td>Initializes the pin function controller (PFC) Selects the required MTU2-related pin functions, so that the pins function as timer pins</td>
</tr>
<tr>
<td>TGRA_3 interrupt</td>
<td>int_mtu2_tgia3()</td>
<td>Handles the TGRA_3 compare match interrupt from MTU2 (channel 3) Increments or decrements the setting to control the three-phase PWM duty cycle Generates an interrupt for every cycle of the PWM carrier cycle (400 μs)</td>
</tr>
</tbody>
</table>

2.3.2 Variable Usage
Table 6 gives a list of variables used in the sample program.

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Description</th>
<th>Name of Employing Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dead_time</td>
<td>Setting for dead time (value set in the TDDR)</td>
<td>mtu2_init ()</td>
</tr>
<tr>
<td>C_cycle</td>
<td>1/2 the PWM carrier cycle (value set in the TCBR)</td>
<td></td>
</tr>
<tr>
<td>Pul_cycle</td>
<td>1/2 the PWM carrier cycle + value of dead time (value set in the TGRC_3)</td>
<td></td>
</tr>
<tr>
<td>Pul_pwm_duty1</td>
<td>PWM duty-cycle setting for the PWM1 output (pins TIOC3B and TIOC3D) (value set in the TGRD_3)</td>
<td>mtu2_init () int_mtu2_tgia3()</td>
</tr>
<tr>
<td>Pul_pwm_duty2</td>
<td>PWM duty-cycle setting for the PWM2 output (pins TIOC4A and TIOC4C) (value set in the TGRC_4)</td>
<td></td>
</tr>
<tr>
<td>Pul_pwm_duty3</td>
<td>PWM duty-cycle setting for the PWM3 output (pins TIOC4B and TIOC4D) (value set in the TGRD_4)</td>
<td></td>
</tr>
</tbody>
</table>
2.4 Procedure for Setting the Module Used

The following subsections describe the flow of processing by the sample program.

2.4.1 Main Function

Figure 11 shows the flow of processing by the main function.

![Figure 11 Processing by Function main](image)

- **main()**
  - 0→Duty_select
  - Initialization: release from standby
    - stbcr_init()
  - Initialization: MTU2
    - mtu2_init()
  - Set interrupt priority register E
    - (IPRE)
  - Initialization: PFC
    - pfc_init()
  - Set timer start register (TSTR)
  - Release interrupt mask
    - set_imask(0)

2.4.2 Initialization for Standby

Figure 12 shows the flow of processing for standby processing.

![Figure 12 Initialization: Release from Standby](image)

- **stbcr_init()**
  - Set standby control register 3
    - (STBCR3)
  - END

[1] Variable initialization
Flag (Duty_select) to judge the need to update the PWM duty cycle is initialized.

[2] On-chip peripheral modules are released from standby

[3] Initialization of multi-function timer pulse unit 2 (MTU2)

[4] Interrupt controller (INTC) setting
Interrupt priority level of the interrupt sources (TGI3A to TGI3D) from MTU2 is set to D'15 (FF).

[5] Initialization of pin function controller (PFC)

[6] Setting for timer start register (TSTR) of MTU2
  - CST4 bit = B'1: Specifies counting by timer counter TCNT_4.
  - CST3 bit = B'1: Specifies counting by timer counter TCNT_3.
  - The CST3 and CST4 bits are set simultaneously.

[7] Setting the interrupt mask bit to 0
CPU interrupts at all interrupt priority levels are enabled.
2.4.3 Initialization of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 13 shows the flow for initialization of MTU2. Settings are made to set up complementary PWM mode 3 on channels 3 and 4.

**Figure 13 Initialization of MTU2**

1. **mtu2_init()**
   - Initialize variables

2. **Set timer start register (TSTR)**
   - Clear bits CST3 and CST4 in timer start register (TSTR) to 0 to halt counting by the timer counters (TCNT).

3. **Set timer control register_3 (TCR_3) and timer control register_4 (TCR_4)**
   - Specification of clock source and source for clearing of timer counters
     - CCLR[2:0] bits = B'000: Disables clearing of TCNT.
     - CKEG[1:0] bits = B'00: TCNT counts rising edges.
   - The same initial values are set in registers TCR_3 and TCR_4.

4. **Set timer counter_3 (TCNT_3) and timer counter_4 (TCNT_4)**
   - Initialization of timer counters TCNT_3 and TCNT_4
     - Value of dead time is set in the TCNT_3 register.
     - H'0000 is set in the TCNT_4 register.

5. **Initialization of PWM duty cycles**
   - Initial values for PWM duty cycle are set in compare match registers (TGRA_3, TGRA_4, and TGRB_4) and buffer registers (TGRD_3, TGRC_4, and TGRD_4).
   - The same values are set in the compare match registers and buffer registers.

6. **Set timer general register A_3 (TGRA_3) and timer general register C_3 (TGRC_3)**
   - Value of dead time is set in the dead time data register (TDDR).

7. **Set timer dead time data register (TDDR)**
   - Half the carrier cycle is set in the timer cycle data register (TCDR) and timer cycle buffer register (TCBR).
   - When the setting for non-generation of dead time has been made, set TDDR to 1, and TGRA_3 and TGRC_3 to the value (1/2 the carrier cycle + 1).

8. **Set timer cycle data register (TCDR) and timer cycle buffer register (TCBR)**
   - Using the PSYE bit in timer output control register (TOCR1) to specify enabling or disabling of output toggling in synchronization with the PWM cycle;
   - PWM output level setting by the OLSN and OLSN bits
     - PSYE bit = B'1: Enable toggled output.
     - OLSN bit = B'0: Inverse output is active at the low level.
     - OLSN bit = B'0: Output of positive signals is active at the low level.

9. **Set timer output control register 1 (TOCR1)**
   - Setting to complementary PWM mode 3 by timer mode register_3 (TMDR_3)
     - MD[3:0] bits = B‘1111: Complementary PWM mode 3 (transfer at crest and trough)
     - Do not make any setting in the TMDR_4 register. Additionally, mode setting should be made while TCNT_3 and TCNT_4 are halted.

10. **Set timer interrupt enable register (TIER_3)**
    - Setting to enable or disable interrupt requests
      - TGIEA bit = B’1: Enables interrupt requests (TGIA_3) from channel 3 corresponding to setting of the TGFA bit.
2.4.4 Initialization of Pin Function Controller (PFC)

Figure 14 shows the flow for initialization of the PFC.

2.4.5 Handling of the Compare Match Interrupt

Figure 15 shows the flow for handling the compare match interrupt (TGRA_3) from MTU2.
2.5  Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

### 2.5.1 Clock Pulse Generator (CPG)

Table 7 gives a list of settings for registers of the clock pulse generator (CPG).

#### Table 7  Clock Pulse Generator (CPG)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency control register (FRQCR)</td>
<td>H'FFFFE800</td>
<td>H'0241</td>
<td>Specifies division ratios for operating frequency</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- IFC[2:0] = B'000: ×1, internal clock (I(\phi))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- BFC[2:0] = B'001: ×1/2, bus clock (B(\phi))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- PFC[2:0] = B'001: ×1/2, peripheral clock (P(\phi))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MIFC[2:0] = B'000: ×1, MTU2S clock (MI(\phi))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MPFC[2:0] = B'001: ×1/2, MTU2 clock (MP(\phi))</td>
</tr>
</tbody>
</table>

#### 2.5.2 Power-Down Modes

Table 8 gives register settings related to low-power modes.

#### Table 8  Power-Down Modes

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 4 (STBCR4)</td>
<td>H'FFFFE808</td>
<td>H'BF</td>
<td>Settings for the operation of various modules</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP23 = B'1: Clock supply to MTU2S halted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP22 = B'0: MTU2 runs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP21 = B'1: Clock supply to CMT halted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP20 = B'1: Clock supply to A/D_1 halted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP19 = B'1: Clock supply to AD_0 halted.</td>
</tr>
</tbody>
</table>
### Multi-Function Timer Pulse Unit 2 (MTU2)

Table 9 gives a list of settings for registers of multi-function timer pulse unit 2 (MTU2).

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer control register_3</td>
<td>H’FFFFC200</td>
<td>H’01</td>
<td>Sets details of TCNT control.</td>
</tr>
<tr>
<td>(TCR_3)</td>
<td></td>
<td></td>
<td>• CCLR[2:0] = B’000: TCNT clearing disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• CKEG[1:0] = B’00: TCNT counts rising edge.</td>
</tr>
<tr>
<td>Timer control register_4</td>
<td>H’FFFFC201</td>
<td>H’01</td>
<td>Sets details of TCNT control.</td>
</tr>
<tr>
<td>(TCR_4)</td>
<td></td>
<td></td>
<td>• CCLR[2:0] = B’000: TCNT clearing disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• CKEG[1:0] = B’00: TCNT counts rising edge.</td>
</tr>
<tr>
<td>Timer counter_3 (TCNT_3)</td>
<td>H’FFFFC210</td>
<td>D’40</td>
<td>16-bit counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For complementary PWM mode, the initial value is the same as the value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>in timer dead time data register (TDDR).</td>
</tr>
<tr>
<td>Timer counter_4 (TCNT_4)</td>
<td>H’FFFFC212</td>
<td>H’0000</td>
<td>16-bit counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Initial value is set to H’0000.</td>
</tr>
<tr>
<td>Timer general register A_3</td>
<td>H’FFFFC218</td>
<td>D’2040</td>
<td>For complementary PWM mode, sets the upper limit (1/2 carrier cycle + dead</td>
</tr>
<tr>
<td>(TGRA_3)</td>
<td></td>
<td></td>
<td>time) of TCNT_3.</td>
</tr>
<tr>
<td>Timer general register C_3</td>
<td>H’FFFFC224</td>
<td></td>
<td>For complementary PWM mode, a buffer register for TGRA_3.</td>
</tr>
<tr>
<td>(TGRC_3)</td>
<td></td>
<td></td>
<td>The initial value is the same as the value in TGRA_3.</td>
</tr>
<tr>
<td>Timer general register B_3</td>
<td>H’FFFFC21A</td>
<td>D’1020</td>
<td>For complementary PWM mode, a comparison register for PWM output 1.</td>
</tr>
<tr>
<td>(TGRB_3)</td>
<td></td>
<td></td>
<td>Determines the PWM duty cycle (initial output value).</td>
</tr>
<tr>
<td>Timer general register D_3</td>
<td>H’FFFFC226</td>
<td></td>
<td>In complementary PWM mode, a buffer register for TGRB_3.</td>
</tr>
<tr>
<td>(TGRD_3)</td>
<td></td>
<td></td>
<td>The initial value is the same as the value in TGRB_3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Incremented or decremented value of PWM duty cycle is set in this register</td>
</tr>
<tr>
<td>Timer general register A_4</td>
<td>H’FFFFC21C</td>
<td>D’1020</td>
<td>For complementary PWM mode, a comparison register for PWM output 2.</td>
</tr>
<tr>
<td>(TGRA_4)</td>
<td></td>
<td></td>
<td>Determines the PWM duty cycle (initial output value).</td>
</tr>
<tr>
<td>Timer general register C_4</td>
<td>H’FFFFC228</td>
<td></td>
<td>In complementary PWM mode, a buffer register for TGRA_4.</td>
</tr>
<tr>
<td>(TGRC_4)</td>
<td></td>
<td></td>
<td>The initial value is the same as the value in TGRA_4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Incremented or decremented value of PWM duty cycle is set in this register</td>
</tr>
<tr>
<td>Register Name</td>
<td>Address</td>
<td>Setting</td>
<td>Description</td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>-------------</td>
<td>---------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Timer general register B_4 (TGRB_4)</td>
<td>H'FFFFFC21E</td>
<td>D'1020</td>
<td>For complementary PWM mode, a comparison register for PWM output 3. Determines the PWM duty cycle (initial output value).</td>
</tr>
<tr>
<td>Timer general register D_4 (TGRD_4)</td>
<td>H'FFFFFC22A</td>
<td></td>
<td>In complementary PWM mode, a buffer register for the TGRB_4. The initial value is the same as the value in TGRB_4. Incremented or decremented value of PWM duty cycle is set in this register.</td>
</tr>
<tr>
<td>Timer dead time data register (TDDR)</td>
<td>H'FFFFFC216</td>
<td>D'40</td>
<td>16-bit register used only in complementary PWM mode. Sets the offset value (the dead time) between TCNT_4 and TCNT_3.</td>
</tr>
<tr>
<td>Timer cycle data register (TCDR)</td>
<td>H'FFFFFC214</td>
<td>D'2000</td>
<td>Register used only in complementary PWM mode. Sets the upper limit (1/2 the carrier cycle) of TCNT_4.</td>
</tr>
<tr>
<td>Timer cycle buffer register (TCBR)</td>
<td>H'FFFFFC222</td>
<td></td>
<td>Register used only in complementary PWM mode. Buffer register for the TCDR. Sets the same as the value in TCDR.</td>
</tr>
<tr>
<td>Timer output control register 1 (TOCR1)</td>
<td>H'FFFFFC20E</td>
<td>H'40</td>
<td>Sets output operation in complementary PWM mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PSYE = B'1: Toggled output in synchronization with the PWM cycle is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• TOCL = B'0: Writing to the TOCS, OLSN, and OLSP bits is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• TOCS = B'0: Selects use of the TOCR1 setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OLSN = B'0: Selects levels for inverse output in complementary PWM mode. Initial output = high, active level = low</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OLSP = B'0: Selects levels for output of positive signals in complementary PWM mode. Initial output = high, active level = low</td>
</tr>
<tr>
<td>Timer mode register_3 (TMDR_3)</td>
<td>H'FFFFFC202</td>
<td>H'3F</td>
<td>Sets operation mode (channel 3).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BFB = B'1: TGRB and TGRD are used together (buffered operation)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BFA = B'1: TGRA and TGRC are used together (buffered operation)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• MD[3:0] = B'1111: Complementary PWM mode 3 (transfer at crest and trough)</td>
</tr>
<tr>
<td>Register Name</td>
<td>Address</td>
<td>Setting</td>
<td>Description</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>---------------</td>
<td>---------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Timer mode register_4 (TMDR_4)</td>
<td>H'FFFFC203</td>
<td>—</td>
<td>Sets operation mode (channel 4).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: When channel 3 is set to complementary PWM mode, settings made for channel 4 are ineffective (operation is automatically in accord with the settings of channel 3). No setting is made; the register is left at its initial value.</td>
</tr>
<tr>
<td>Timer output master enable register (TOER)</td>
<td>H'FFFFC20A</td>
<td>H'FF</td>
<td>Specifies enabling or disabling of output through the MTU2 output pins.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OE4D = B'1: MTU2 output on the TIOC4D pin is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OE4C = B'1: MTU2 output on the TIOC4C pin is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OE3D = B'1: MTU2 output on the TIOC3D pin is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OE4B = B'1: MTU2 output on the TIOC4B pin is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OE4A = B'1: MTU2 output on the TIOC4A pin is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• OE3B = B'1: MTU2 output on the TIOC3B pin is enabled.</td>
</tr>
<tr>
<td>Timer interrupt enable register_3 (TIER_3)</td>
<td>H'FFFFC208</td>
<td>H'01</td>
<td>Specifies enabling or disabling of interrupt requests.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• TGIEA = B'1: Interrupt requests (TGIA) corresponding to setting of the TGFA bit are enabled.</td>
</tr>
<tr>
<td>Timer start register (TSTR)</td>
<td>H'FFFFC280</td>
<td>H'C0</td>
<td>Selects operation or stoppage of TCNT for channels 0 to 4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• CST4 = B'1: TCNT_4 counts</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• CST3 = B'1: TCNT_3 counts</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Counting by TCNT_2 to TCNT_0 is stopped. Bit settings for counting by TCNT_4 and TCNT_3 should be made at the same time.</td>
</tr>
</tbody>
</table>
2.5.4 Interrupt Controller (INTC)

Table 10 gives a list of settings for registers of the interrupt controller (INTC).

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt priority register E</td>
<td>H'FFFFE984</td>
<td>H'00F0</td>
<td>Selects interrupt priority (level 0 to 15).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Bit 15 to 12 = B'0000: MTU2 (TGIA_2 and TGIB_2) interrupt level = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Bit 11 to 8 = B'0000: MTU2 (TCI2V and TCI2U) interrupt level = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Bit 7 to 4 = B'1111: MTU3 (TGIA to TGIB) interrupt level = 15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Bit 3 to 0 = B'0000: MTU3 (TCI_3) interrupt level = 0</td>
</tr>
<tr>
<td>In this sample program, TGI3A interrupt is used.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.5.5 Pin Function Controller (PFC)

Table 11 gives a list of settings for registers of the pin function controller (PFC).

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port E control register L4</td>
<td>H'FFFFD310</td>
<td>H'1111</td>
<td>Specifies functions of multiplexed pins on port E.</td>
</tr>
<tr>
<td>(PECRL4)</td>
<td></td>
<td></td>
<td>• PE15MD[2:0] = B'001: Specifies the TIOC4D I/O (MTU2) for PE15.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE14MD[2:0] = B'001: Specifies the TIOC4C I/O (MTU2) for PE14.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE13MD[2:0] = B'001: Specifies the TIOC4B I/O (MTU2) for PE13.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE12MD[2:0] = B'001: Specifies the TIOC4A I/O (MTU2) for PE12.</td>
</tr>
<tr>
<td>Port E control register L3</td>
<td>H'FFFFD312</td>
<td>H'1011</td>
<td>Specifies functions of multiplexed pins on port E.</td>
</tr>
<tr>
<td>(PECRL3)</td>
<td></td>
<td></td>
<td>• PE11MD[2:0] = B'001: Specifies the TIOC3D I/O (MTU2) for PE11.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE10MD[2:0] = B'000: Specifies the PE10 I/O (port) for PE10.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE9MD[2:0] = B'001: Specifies the TIOC3B I/O (MTU2) for PE9.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE8MD[2:0] = B'001: Specifies the TIOC3A I/O (MTU2) for PE8.</td>
</tr>
<tr>
<td>Port E I/O register L</td>
<td>H'FFFFD306</td>
<td>H'FB00</td>
<td>Specifies input and output directions for port E pins.</td>
</tr>
<tr>
<td>(PEIORL)</td>
<td></td>
<td></td>
<td>• PE15IOR = B'1: Specifies the TIOC4D pin (PE15) for output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE14IOR = B'1: Specifies the TIOC4C pin (PE14) for output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE13IOR = B'1: Specifies the TIOC4B pin (PE13) for output.</td>
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<tr>
<td></td>
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<td></td>
<td>• PE12IOR = B'1: Specifies the TIOC4A pin (PE12) for output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE11IOR = B'1: Specifies the TIOC3D pin (PE11) for output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE10IOR = B'0: Specifies the PE10 (port) for input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE9IOR = B'1: Specifies the TIOC3B pin (PE9) for output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE8IOR = B'1: Specifies the TIOC3A pin (PE8) for output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PE7IOR to PE0IOR all set to B'0: PE7 to PE0 are input pins.</td>
</tr>
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3. Documents for Reference

- Hardware Manual
  SH7137 Group Hardware Manual (REJ09B0402)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Software Manual
  SH-1/SH2/SH-DSP Software Manual (REJ09B0171)
  The most up-to-date version of this document is available on the Renesas Technology Website.
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http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

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