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SH7280 Group

MTU2: Input of Pulse Signals from a Two-Phase Encoder with “Z Phase” (Phase-Counting Mode)

Introduction

This application note describes an example of setting up multi-function timer pulse unit 2 (MTU2) in phase-counting mode for the input of pulse signals from a two-phase encoder (including input in "Z phase").

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

The sample program employs channel 1 of MTU2 in phase counting mode (phase counting mode 1) to count pulses from a two-phase (A and B) encoder with a counter reset function (Z phase). Channel 0 acts as a cycle timer, measuring a 1-ms period for the acquisition of values counted for the two-phase encoder. Figure 1 shows an overview.

1. The A- and B-phase signals from the two-phase encoder are connected to pins TCLKA and TCLKB for input to channel 1 of MTU2. Channel 1 is used to count the number of pulses from the two-phase encoder multiplied by four.
2. Z-phase signals of two-phase encoder are input on the TIOC1A pin of channel 1. The TIOC1A pin detects signals of rising edge (input capture) and clears a counter of channel 1 to 0.
3. Channel 0 of MTU2 is set up to operate as a compare-match timer with a 1-ms cycle. This compare-match signal acts as a source for activation of input capture on the channel-1 side, which obtains (captures) the values from counting at four times the frequency of signals from the encoder.
4. The intervals between edges of the A- and B-phase pulse signals (respectively) from the two-phase encoder are obtained (captured) by using the input capture function of MTU2 channel 0.

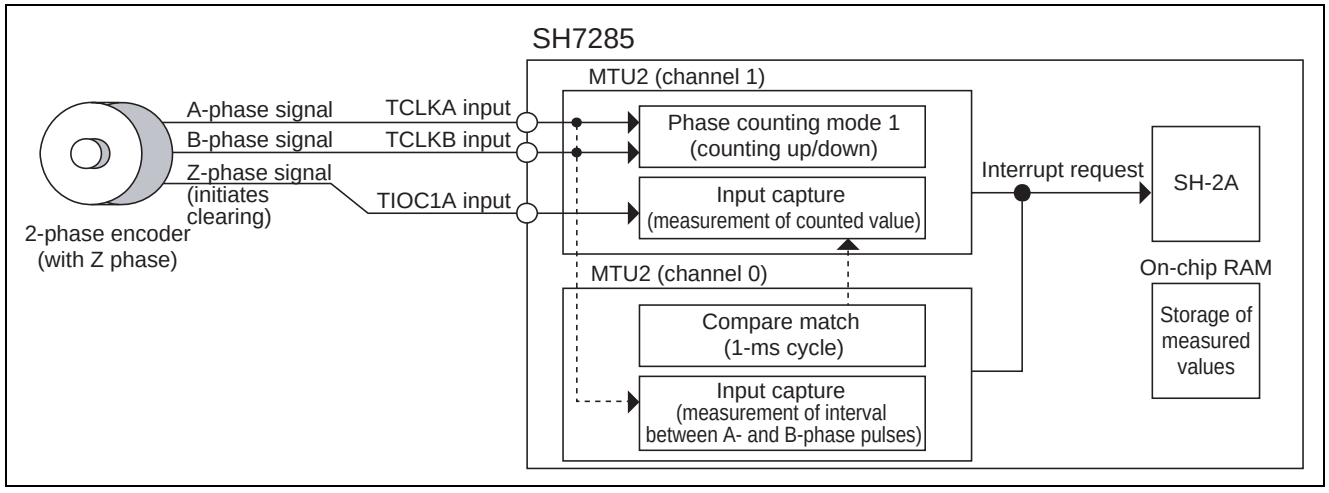


Figure 1 Detection of Pulses from the Two-Phase Encoder (Phase Counting Mode 1)

1.2 Module Used

Channels 0 and 1 of MTU2

1.3 Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
MCU	SH7285 [R5F72856]	
Operating frequency	Internal clock:	Iϕ = 100 MHz
	Bus clock:	Bϕ = 50 MHz
	Peripheral clock:	Pϕ = 50 MHz
	MTU2S clock:	Mϕ = 50 MHz
	AD clock:	Aϕ = 50 MHz
MCU operating mode	Single-chip	
C compiler	SuperH RISC engine C/C++ Compiler Ver.9.01.01 from Renesas Technology	
C compiler options	Default settings of the C compiler	

2. Description of the Sample Application

In this sample program, channel 1 of MTU2 is used in phase counting mode.

2.1 Operational Overview of Module Used

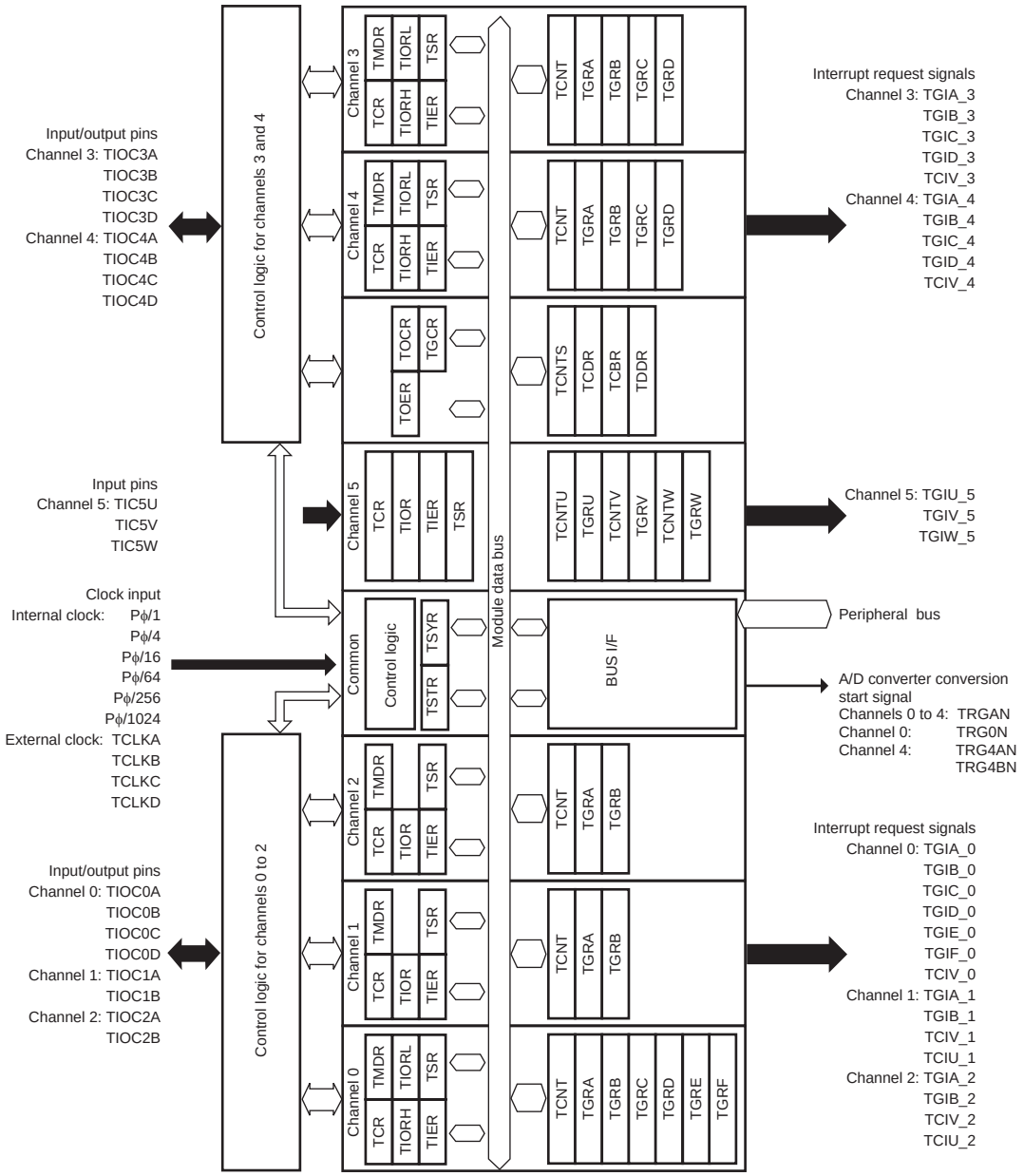
2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

MTU2 is a multi-functional timer unit that has six 16-bit timer channels. Settings for compare-match function, input-capture function, etc. can be made for each channel. Settings for phase counting mode are made for channels 1 and 2, thus enabling detection of the phase difference between two external clock inputs. Table 2 gives an overview of MTU2 and figure 2 is a block diagram of MTU2.

For details on MTU2, see the section on MTU2 in the *SH7280 Group Hardware Manual* (REJ09B0393).

Table 2 Overview of MTU2

Item	Description
Number of channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clock	The clock signal for counter input can be selected from among 8 different input clock signals (except for channel 5, with only 4 different clock signals available)
Operation of channels 0 to 5	• Waveform output on compare match • Input-capture function • Counter clearing • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Input to and output from registers are synchronized with counter operation • PWM output in up to 12 phases in combination with synchronous operation
Triggers for A/D converter	• A/D converter start trigger can be generated. • In complementary PWM mode, interrupts at the crest and trough of the counter value and A/D converter start triggers can be skipped.
Buffered operation	• Settings for buffered operation of registers can be made to channels 0, 3, and 4.
Operating modes	• Settings for PWM mode can be made on channels 0 to 4. • Settings for phase counting mode can be made for each of channels 1 and 2 individually. • In linked operation of channels 3 and 4, waveform output in a total of six phases, including the positive and inverse signals for three basic phases, is possible in reset-PWM mode or complementary PWM mode
Interrupt requests	• 28 different interrupt sources (interrupt generation by compare match, input capture, etc.)
Others	• Cascade-connection operation • High-speed access by internal 16-bit bus • Automatic transfer of register data is enabled. • Module standby mode can be set. • Dead time compensation counter is available in channel 5.



[Legend]

TSTR:	Timer start register	TCDR:	Timer cycle data register
TSYR:	Timer synchronous register	TCBR:	Timer cycle buffer register
TCR:	Timer control register	TDDR:	Timer dead time data register
TMDR:	Timer mode register	TGRA:	Timer general register A
TIOR:	Timer I/O control register	TGRB:	Timer general register B
TIORH:	Timer I/O control register H	TGRC:	Timer general register C
TIORL:	Timer I/O control register L	TGRD:	Timer general register D
TIER:	Timer interrupt enable register	TGRE:	Timer general register E
TGCR:	Timer gate control register	TGRF:	Timer general register F
TOER:	Timer output master enable register	TGRU:	Timer general register U
TOCR:	Timer output control register	TGRV:	Timer general register V
TSR:	Timer status register	TGRW:	Timer general register W
TCNT:	Timer counter		
TCNTS:	Timer subcounter		

Figure 2 Block Diagram of MTU2

2.1.2 Phase Counting Mode

In phase counting mode, the phase difference between two external clock inputs (on pins TCLKA and TCLKB, or pins TCLKC and TCLKD) is detected and TCNT is incremented/decremented accordingly.

The conditions for counting by the timer counter can set up phase counting mode in any of four operating modes (phase counting mode 1, phase counting mode 2, phase counting mode 3, and phase counting mode 4).

Figure 3 shows a sample operation in phase counting mode 1 and table 3 gives conditions for counting up and down by timer counter TCNT in phase counting mode 1.

For details on phase counting mode, see the section on MTU2 in the *SH7280 Group Hardware Manual* (REJ09B0393).

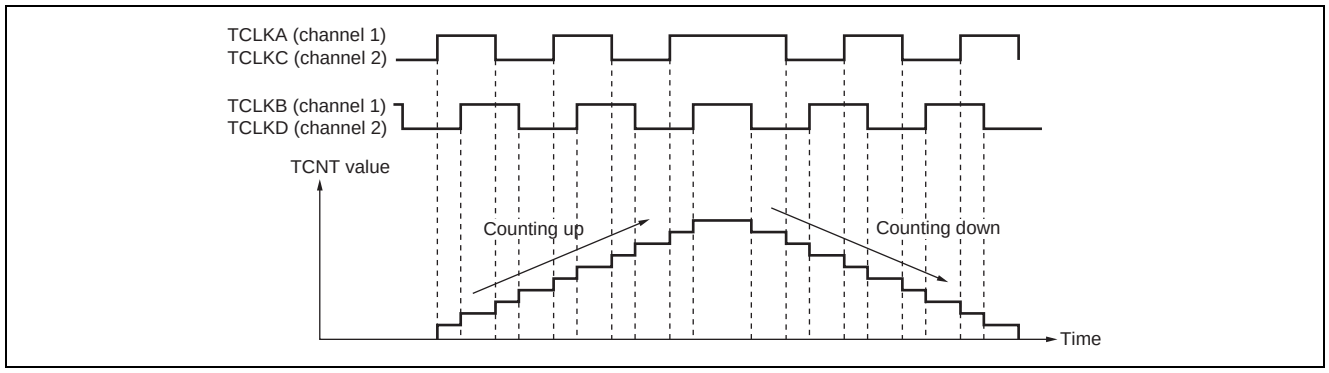


Figure 3 Example of Operation in Phase Counting Mode 1 (Channels 1 and 2)

Table 3 Conditions for Counting up and down in Phase Counting Mode 1

TCLKA Pin (Channel 1) TCLKC Pin (Channel 2)	TCLKA Pin (Channel 1) TCLKD Pin (Channel 2)	Operation
High level	↑: Rising edge	Counting up
Low level	↓: Falling edge	
↑: Rising edge	Low level	
↓: Falling edge	High level	
High level	↓: Rising edge	Counting down
Low level	↑: Falling edge	
↑: Rising edge	High level	
↓: Falling edge	Low level	

2.2 Operation of the Sample Program

2.2.1 Settings for Operation of the Sample Program

In the sample program, channels 1 and 0 of MTU2 operate in conjunction to count pulse signals from the two-phase encoder of a servomotor, etc., and to obtain the values counted every 1 ms. Information on the angular position and speed of a motor can thus be calculated.

Table 4 gives the setting conditions for MTU2 in this sample program and figure 4 shows the configuration of the multi-timer unit in the sample program.

Table 4 Setting for MTU2

Item	Description
Channels in use	0 and 1
Operating mode	(1) Channel 1: Phase counting mode 1 (2) Channel 0: Normal operation (compare-match timer with a 1-ms cycle)
Functions of pins	• TCLKA input pin: Input of A-phase pulses from the two-phase encoder (channel 1) • TCLKB input pin: Input of B-phase pulses from the two-phase encoder (channel 1) • TIOC1A input pin: Input of Z-phase signal that initiates clearing, from the encoder (channel 1)
Counter clock	(1) Channel 1: External clock pins (TCLKA and TCLKB) (2) Channel 0: Internal clock at 50 MHz (Pϕ/1, Pϕ = 50 MHz)
Interrupt	(1) Channel 1: • TGRA input-capture interrupt • TGRB input-capture interrupt • Interrupt by underflow/overflow of timer counter (2) Channel 0: • TGRB input-capture interrupt

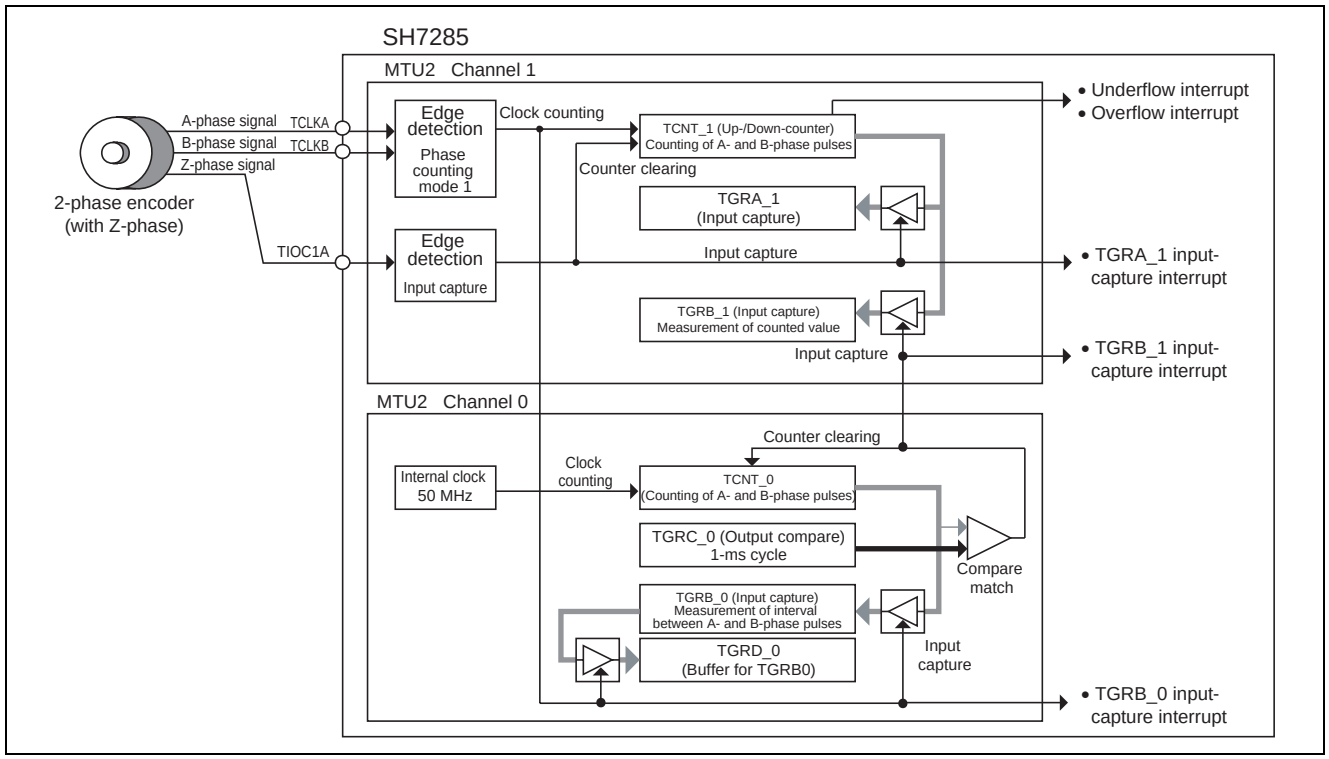


Figure 4 Configuration of Channels 0 and 1 of MTU2

2.2.2 Description of Operation by the Sample Program

Figure 5 shows operation timing of the sample program.

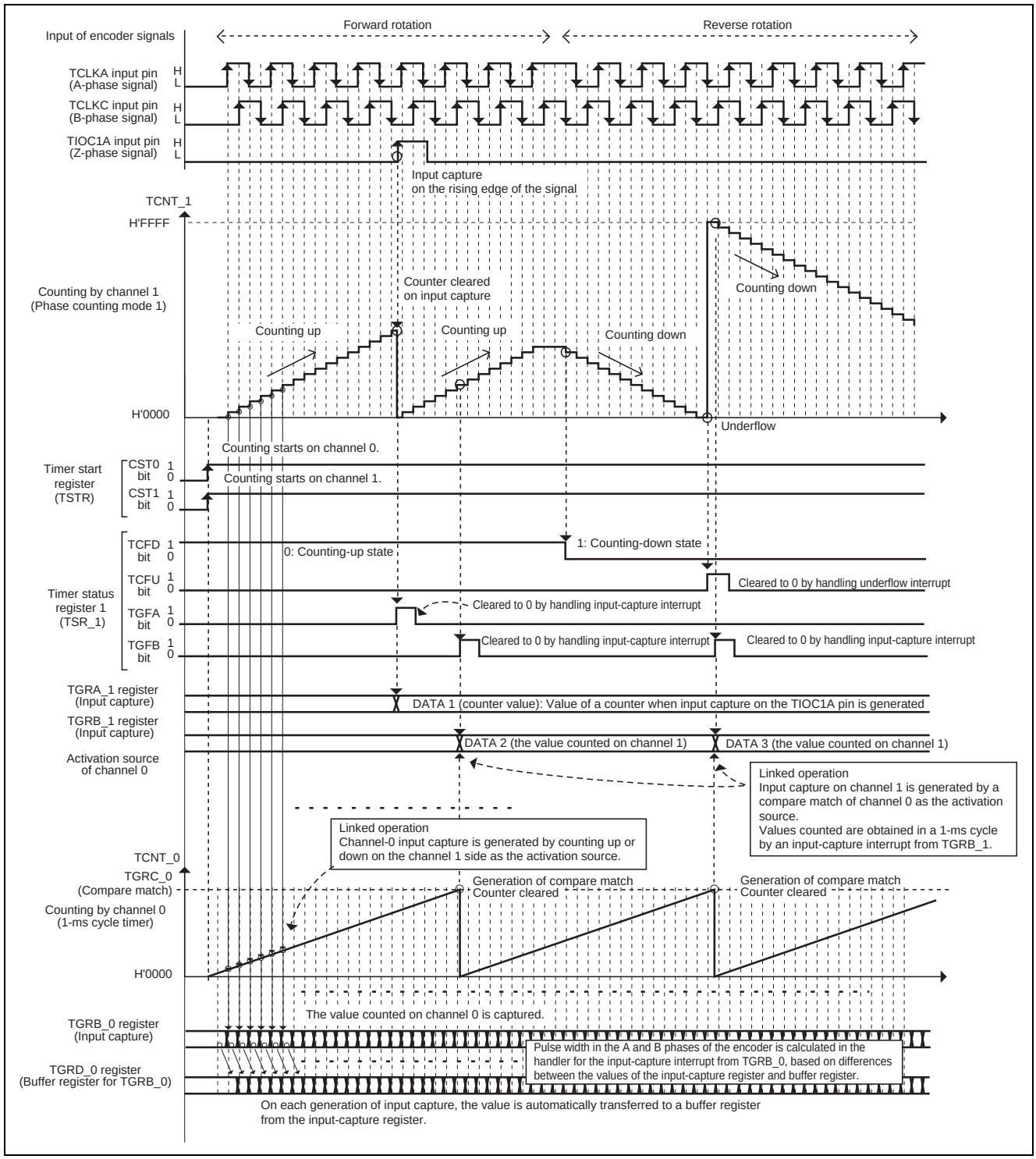


Figure 5 Operation Timing to Detect Signals of Two-Phase Encoder

Phase counting mode 1 (with frequency multiplication by four) is set up for channel 1 of MTU2 and the A- and B-phase signals from an external two-phase encoder are connected to pins TCLKA and TCLKB. The Z-phase signal from the two-phase encoder is connected to the TIOCIA pin of MTU2. Timer counter TCNT_1 detects the difference in phase between the A- and B-phase signals and counts up or down when either signal has a transition. The input-capture function is specified for registers TGRA_1 and TGRB_1 of channel 1.

- When the TGRA_1 register detects rising edges of the signal on the TIOC1A input pin, it captures the value of timer counter TCNT_1. At the same time, timer counter TCNT_1 is cleared and an input-capture interrupt is generated from TGRA.
- In a 1-ms cycle, the TGRB_1 register captures the values counted by timer counter TCNT_1. At the point of capture, an input-capture interrupt is generated from TGRB. The activation source for input capture is a compare match which is generated on the channel-0 side with a cycle of 1 ms. The values in register TGRB_1 provide information on the positions, in a 1-ms cycle, of the two-phase encoder.

On channel 0 of MTU2, the compare-match function is specified for the TGRC_0 register, which is used in the 1-ms cycle timer. The input-capture function is specified for the TGRB_0 register of channel 0. The TGRD_0 register is specified as the buffer register for register TGRB_0.

- Timer counter TCNT_0 is cleared on a compare match with the TGRC_0 register. The compare match is generated in a 1-ms cycle and is the activation source for input capture (the TGRB_1 register) on the channel-1 side.
- The input-capture function is specified for the TGRB_0 register, and this register obtains the value counted on channel 0 at four times the frequency of the pulses of the two-phase encoder. The activation source for input capture is the clock input to the counter on the channel 1 side. Every time the channel 1 counter is incremented or decremented, an input-capture interrupt is generated from TGRB.
- The TGRD_0 register is specified as the buffer for the TGRB_0 register. Each time an input capture from TGRB_0 is generated, the value of the TGRB_0 register is transferred to the TGRD_0 register. Differences between the values of registers TGRB_0 and TGRD_0 are obtained in the handler for the input-capture interrupt from TGRB, and the width of a signal at four-times the frequency of the two-phase encoder pulses is calculated from the results.

2.3 Configuration of the Sample Program

2.3.1 Description of Functions

Table 5 lists functions used in the sample program.

Table 5 Functions Used

Function Name	Label	Description
Main	main ()	Initializes other modules and makes settings to start the timers of MTU2
Standby setting	stbcr_init ()	Makes the setting to release MTU2 from standby
Initialization of MTU2	mtu2_init ()	Initializes MTU2 (channels 0 and 1) Places channel 1 in phase-counting mode 1 and sets up channel 0 as a 1-ms cycle timer
Initialization of PFC	pfc_init ()	Initializes the pin function controller (PFC) Selects the required MTU2-related pin functions, so that the pins function as timer pins
TGRA_1 interrupt	int_mtu2_tgia1 ()	Handles the TGRA_1 input-capture interrupt from MTU2 (channel 1) Processing initiated by rising edges of the Z-phase signal from the two-phase encoder Obtains the value counted at the time of counter clearing
TGRB_1 interupt	int_mtu2_tgib1 ()	Handles the TGRB_1 input-capture interrupt from MTU2 (channel 1) Generates an interrupt with a 1-ms cycle Obtains positional information (counted values) on the two-phase encoder
TCFV_1 interrupt	int_mtu2_tcfv1 ()	Handles a counter overflow interrupt from MTU2 (channel 1)
TCFU_1 interrupt	int_mtu2_tcfu1 ()	Handles a counter underflow interrupt from MTU2 (channel 1)
TGRB_0 interrupt	int_mtu2_tgib0 ()	Handles the TGRB_0 input-capture interrupt from MTU2 (channel 0) Calculates the interval between pulses in the A and B phases of the two-phase encoder

2.3.2 Variable Usage

Table 6 gives a list of variables used in the sample program.

Table 6 Variable Usage

Label Name	Description	Name of Employing Module
TGRA1_data	Input-capture value from the TGRA register of channel 1 of MTU2: the value captured is the value of the timer counter at the time of a rising edge in the Z-phase signal from the two-phase encoder	int_mtu2_tgia1 ()
TGRB1_data_old	Retains the previous input-capture value from the TGRB register of channel 1 of MTU2.	int_mtu2_tgib1 ()
TGRB1_data_diff	Difference between the input-capture value from the TGRB register of channel 1 of MTU2 and its previous value (TGRB1_data_old) The value represents the increase in the value counted for the two-phase encoder between 1-ms cycles.	int_mtu2_tgib1 ()
Under_over_flow_cnt	Counts the number of times the TCNT counter on channel 1 of MTU2 has overflowed or underflowed.	int_mtu2_tcfv1 () int_mtu2_tcfu1 ()
TGRD0_B0_data_diff	The interval between edges of the A- and B-phase signals from the two-phase encoder The value represents the difference between the value (input capture) in register TGRB of channel 0 of MTU2 and the value (previous value of the TGRB register) in the corresponding buffer register, TGRD.	int_mtu2_tgib0 ()

2.4 Procedure for Setting the Module Used

The following subsections describe the flow of processing by the sample program.

2.4.1 Main Function

Figure 6 shows the flow of processing by the main function.

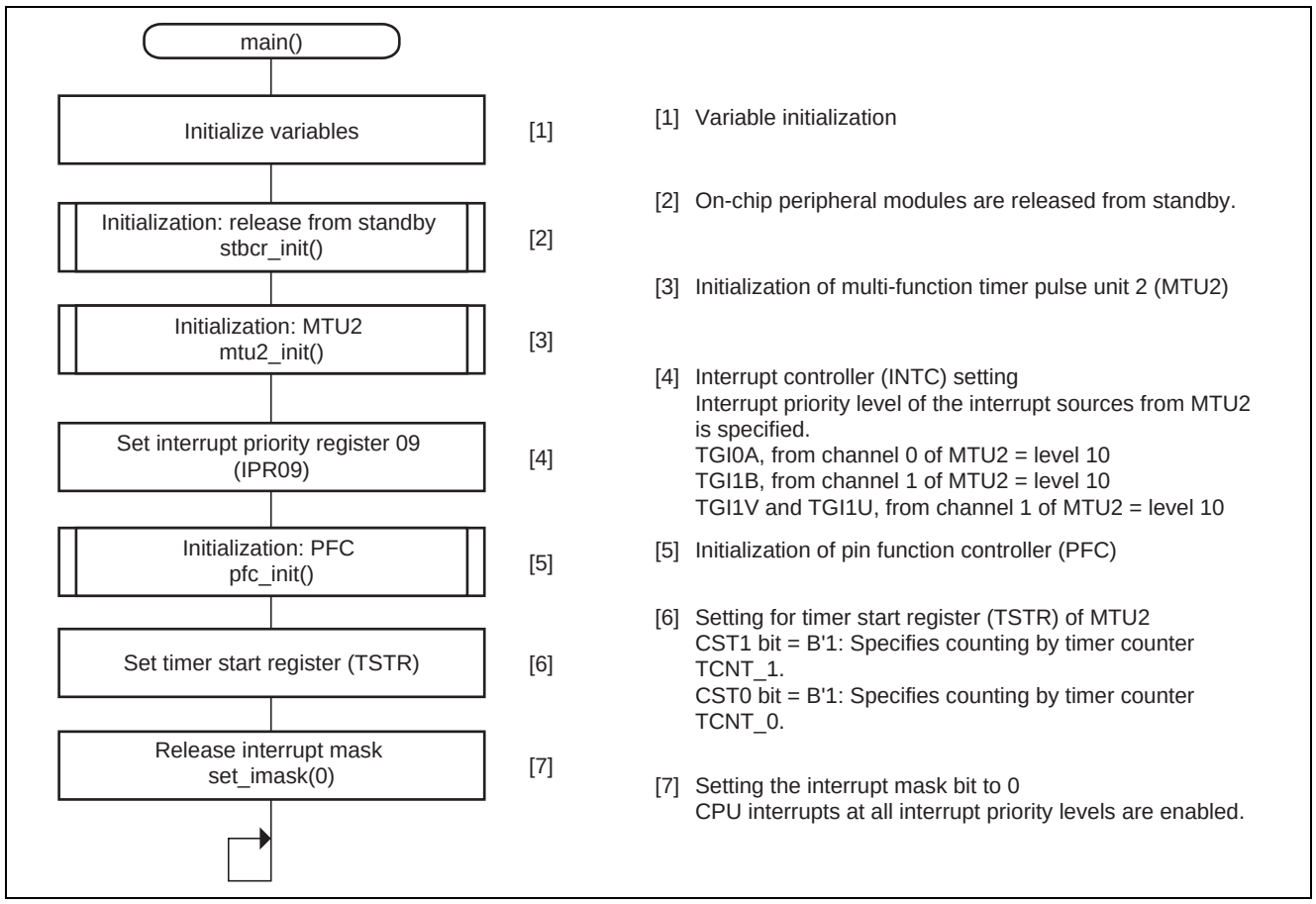


Figure 6 Processing by Function main

2.4.2 Setting to Release the Module from Standby

Figure 7 shows the flow of processing for release of the module from standby.

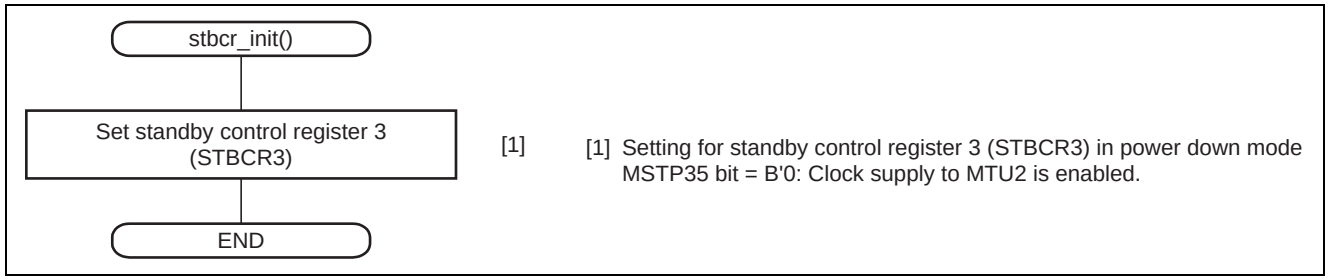
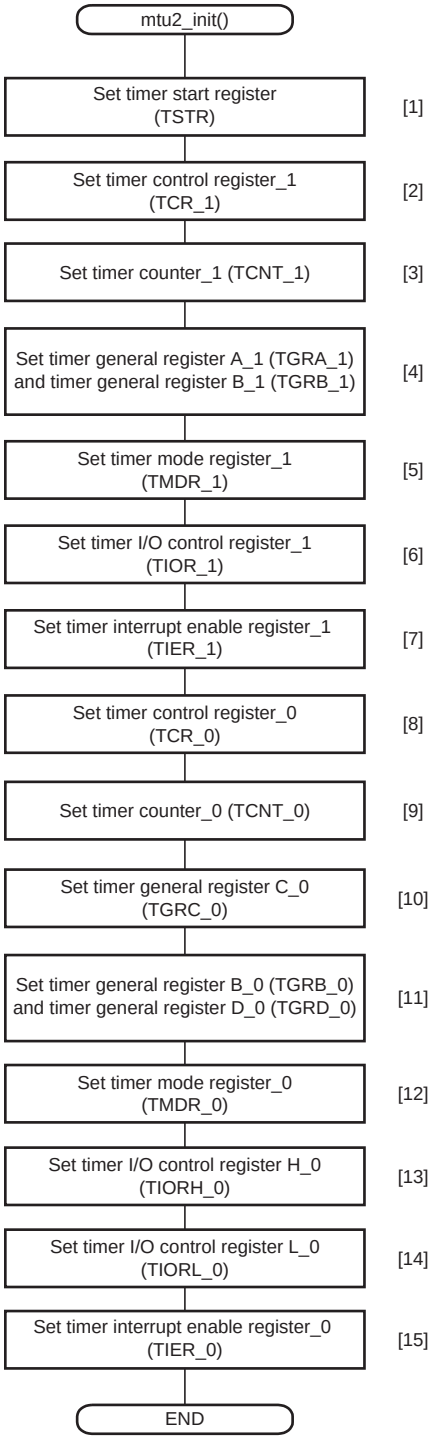


Figure 7 Setting for Release of the Module from Standby

2.4.3 Initialization of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 8 shows the flow for initialization of MTU2.



[1] Counting by channels 0 to 4 of MTU2 is halted.

[2] Specification of clock source and source for clearing of timer counters of channel 1
CCLR[2:0] bits = B'000: Disables clearing of TCNT
CKEG[1:0] bits = B'00: TCNT counts rising edges*1
TPSC[2:0] bits = B'000: TCNT counts cycles of internal clock Pϕ/1*1

[Note] 1. When phase-counting mode is in use, settings made with these bits are ineffective (operation is in accord with the settings made for phase-counting mode).
Regardless of any settings made in bits TPSC[2:0] and CKEG[1:0], the external clock is specified as the counter input clock, and TCNT functions as an up-/down-counter.

[3] Clearing timer counter TCNT_1 to 0

[4] Clearing registers TGRA_1 and TGRB_1 to 0
TGRA_1 and TGRB_1 function as input-capture register.

[5] Setting for operation mode of channel 1
MD[3:0] bits = B'0100: Phase counting mode 1

[6] Settings for operation of TGRA_1 and TGRB_1
IOB[3:0] bits = B'1100: TGRB_1 is specified as an input-capture register.
Input capture is initiated by a compare match signal from TGRC_0 of channel 0.
IOA[3:0] bits = B'1000: TGRA_1 is specified as input-capture register.
Input capture is generated at a rising edge of the TIOC1A input pin.

[7] Setting to enable or disable interrupt requests from channel 1
TGIEU bit = B'1: Interrupt requests on counter underflow are enabled.
TGIEV bit = B'1: Interrupt requests on counter overflow are enabled.
TGIEB bit = B'1: Interrupt requests (TGIB_1) by TGFB are enabled.
TGIEA bit = B'1: Interrupt requests (TGIA_1) by TGFA are enabled.

[8] Specification of clock source and source of clearing of timer counters of channel 0
CCLR[2:0] bits = B'101: TCNT is cleared on TGRC compare match.
CKEG[1:0] bits = B'00: TCNT counts rising edges.
TPSC[2:0] bits = B'000: TCNT counts cycles of internal clock Pϕ/1.

[9] Clearing timer counter TCNT_0 to 0

[10] Initialization of the TGRC_0 register
TGRC_0 is specified as a compare-match register and the cycle is set to 1 ms (the setting is D'49999 at 50 MHz).

[11] Clearing registers TGRB_0 and TGRD_0 to 0
TGRB_0 is used as an input-capture register.
TGRD_1 is used as a buffer register.

[12] Setting operation mode of channel 0
BFB = B'1: Register TGRD is used as a buffer register.
MD[3:0] bits = B'0000: Normal operation mode

[13] Setting operation of registers TGRA_0 and TGRB_0
IOB[3:0] bits = B'1100: TGRB_0 is specified as an input-capture register.
Source for input capture is the counter clock TCNT_1 of channel 1, and input capture is performed when it counts up or down.
IOA[3:0] bits = B'0000 (initial value): TGRA_0 is not in use.

[14] Setting operation of registers TGRC_0 and TGRD_0
IOD[3:0] bits = B'0000 (initial value): TGRD_0 is specified as a buffer register.
IOC[3:0] bits = B'0000: TGRC_0 is specified as a compare-match register.

[15] Setting to enable or disable interrupt request by channel 0
TGIEB bit = B'1: Interrupt requests (TGIB_1) by TGFB are enabled.

Figure 8 Initialization of MTU2

2.4.4 Setting for Pin Function Controller (PFC)

Figure 9 shows the flow for setting the PFC.

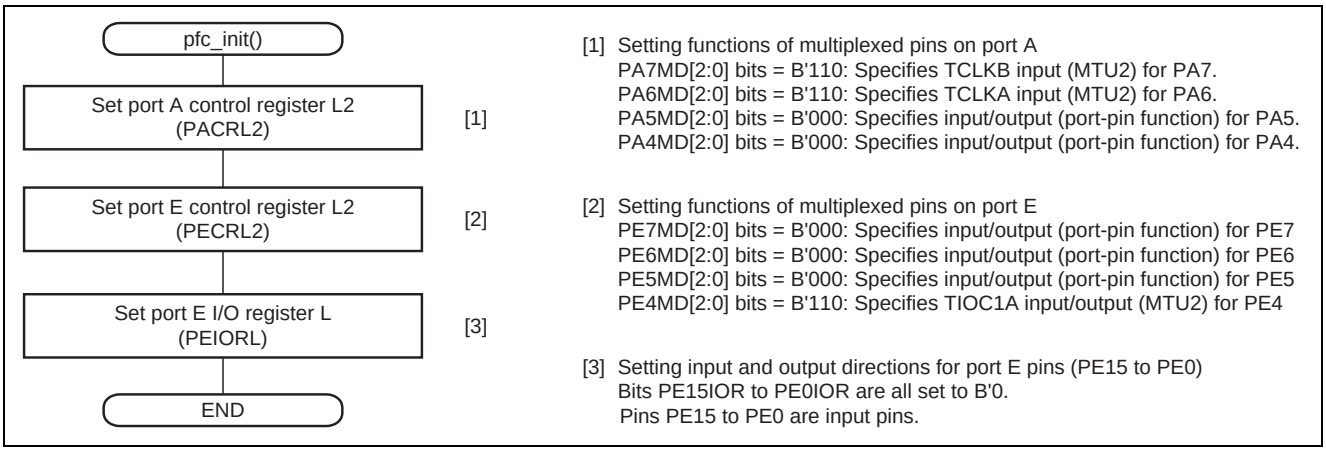


Figure 9 Flow for Setting PFC

2.4.5 Handling of the Input Capture (TGRA_1) Interrupt from Channel 1 of MTU2

Figure 10 shows the flow of handling for the input capture interrupt (TRRA_1) from channel 1 of MTU2. An interrupt is generated on a rising edge of the Z-phase signal of two-phase encoder.

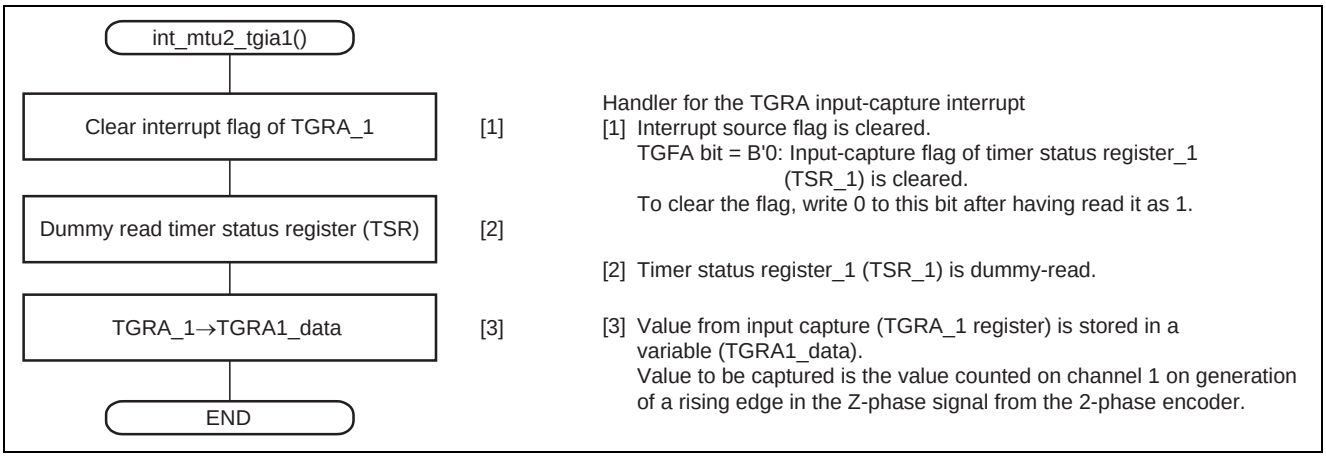


Figure 10 Handling of the Input Capture (TGRA_1) Interrupt from Channel 1 of MTU2

2.4.6 Handling of the Input Capture (TGRB_1) Interrupt from Channel 1 of MTU2

Figure 11 shows the flow of handling for the input capture interrupt (TRRB_1) from channel 1 of MTU2. An interrupt is generated in 1-ms cycles.

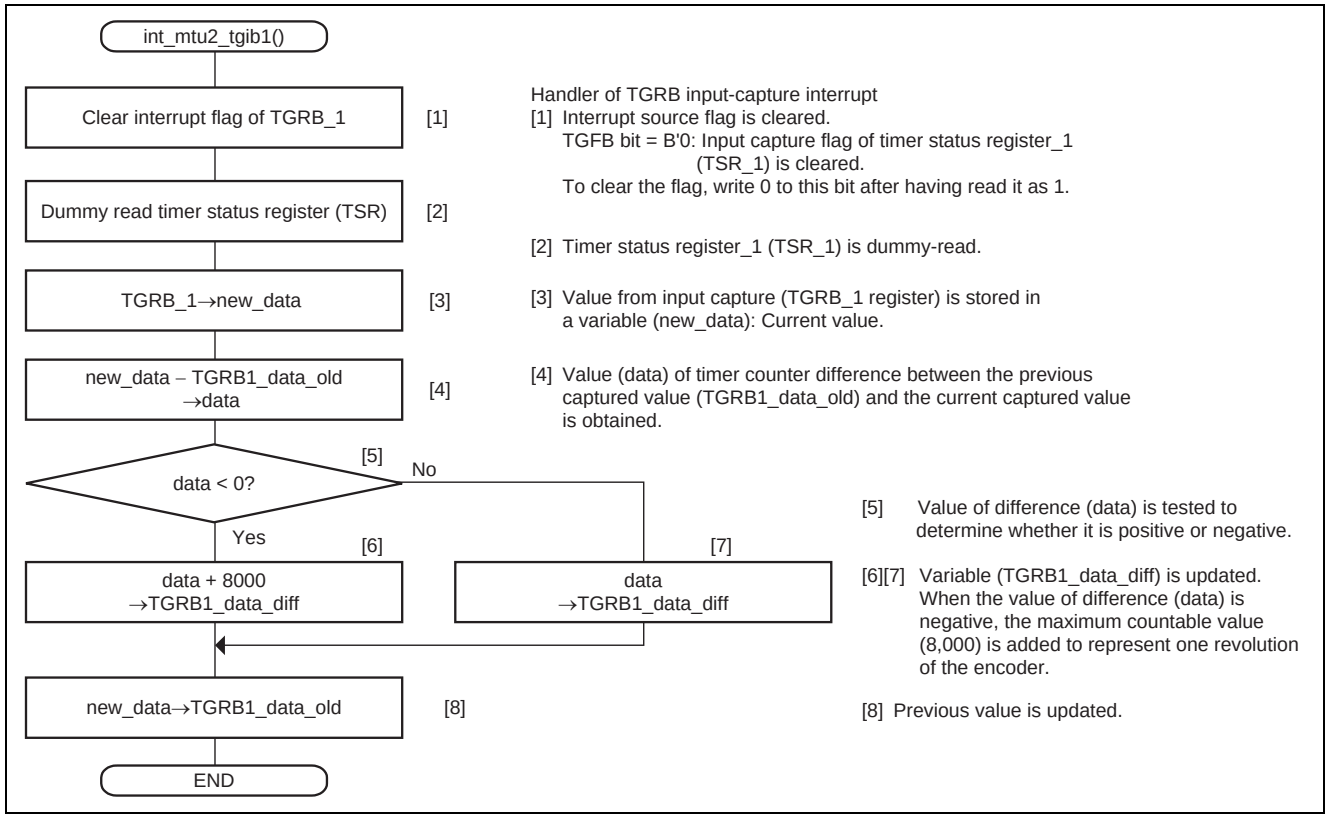


Figure 11 Handling of the Input Capture (TGRB_1) Interrupt from Channel 1 of MTU2

2.4.7 Handling of the Overflow Interrupt from Channel 1 of MTU2

Figure 12 shows the flow of handling for the overflow interrupt from channel 1 of MTU2.

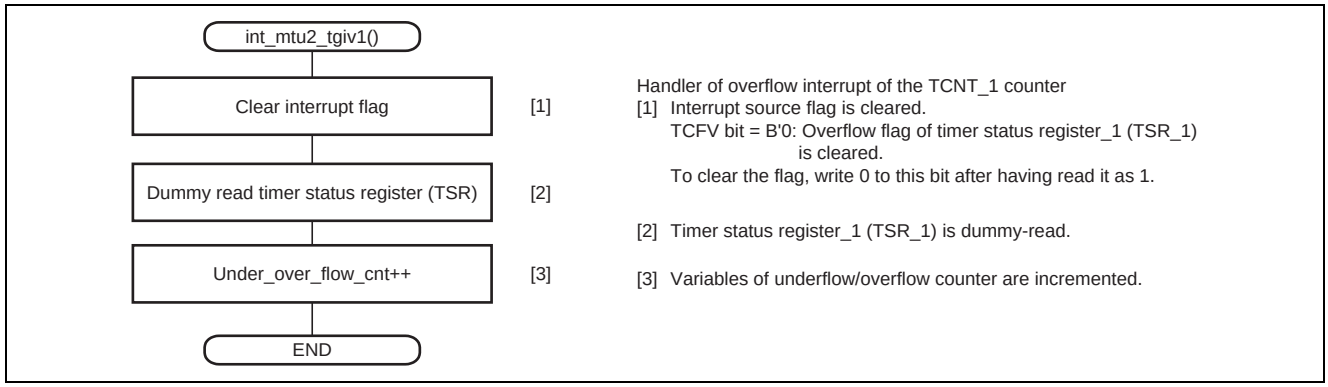


Figure 12 Handling of the Overflow Interrupt from Channel 1 of MTU2

2.4.8 Handling of the Underflow Interrupt from Channel 1 of MTU2

Figure 13 shows the flow of handling for the underflow interrupt from channel 1 of MTU2.

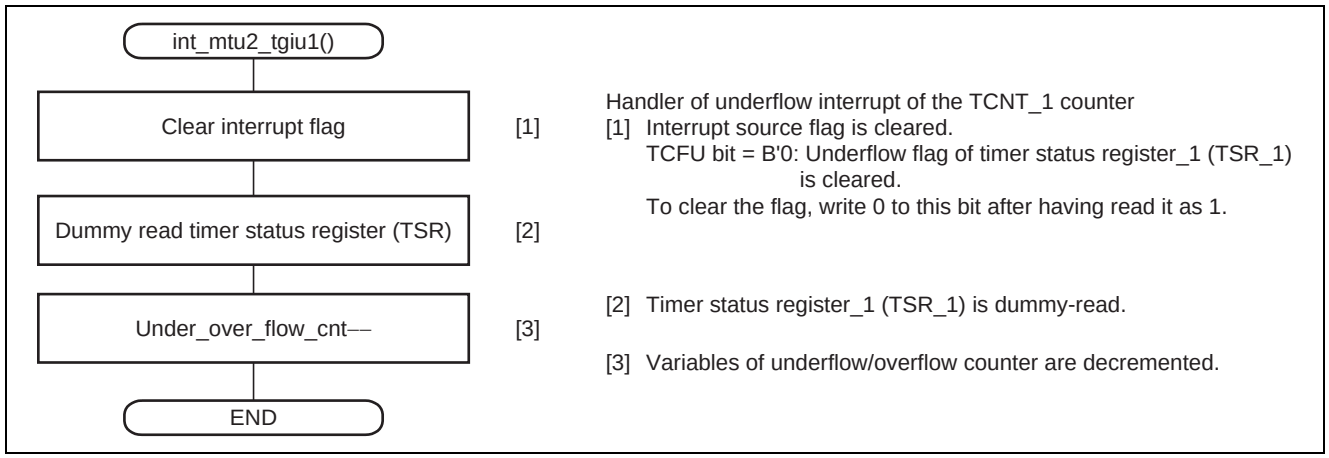


Figure 13 Handling of the Underflow Interrupt from Channel 1 of MTU2

2.4.9 Handling of the Input Capture (TGRB_0) Interrupt from Channel 0 of MTU2

Figure 14 shows the flow of handling for the input capture (TGRB_0) interrupt from channel 0 of MTU2. An interrupt is generated every time channel 1 counts up or down. This is used in calculating the intervals between edges of the A- and B-phase signals from the two-phase encoder.

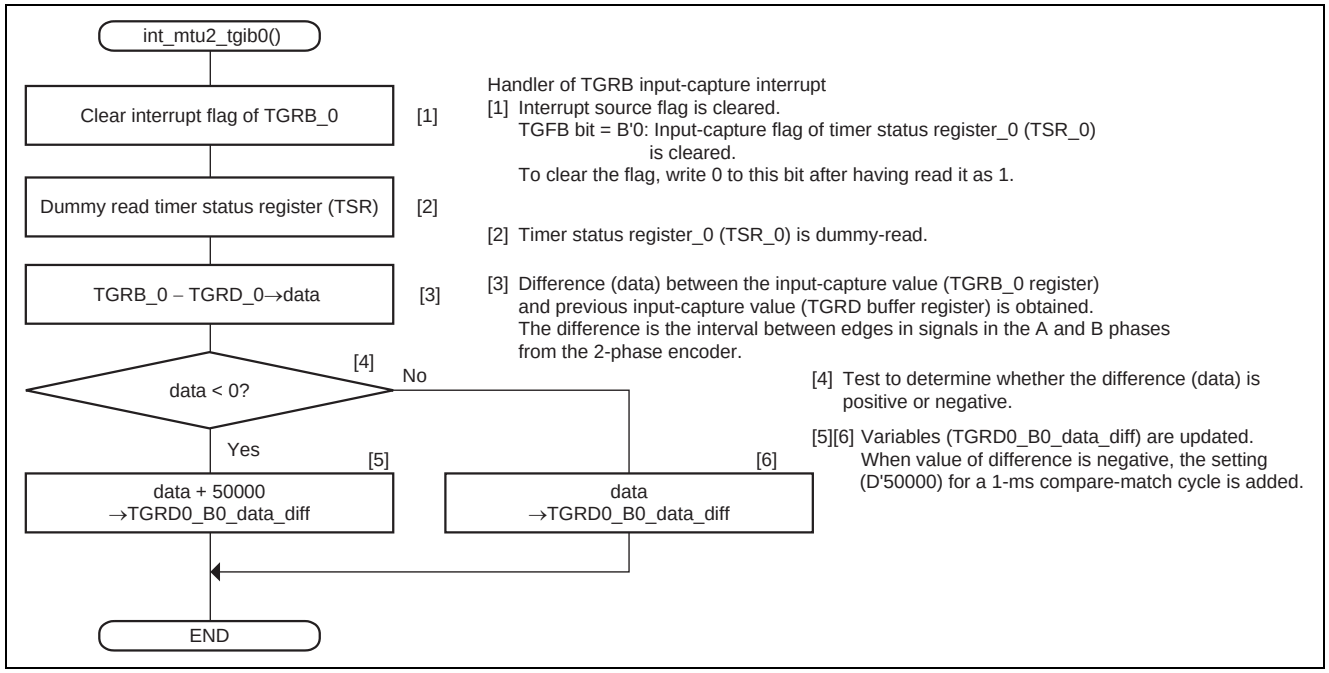


Figure 14 Handling of the Input Capture (TGRB_0) Interrupt from Channel 1 of MTU2

2.5 Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

2.5.1 Clock Pulse Generator (CPG)

Table 7 gives a list of settings for registers of the clock pulse generator (CPG).

Table 7 Clock Pulse Generator (CPG)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	Specifies division ratios for operating frequency • STC [2:0] = B'001: Bus clock (Bϕ) frequency division ratio, × 1/2 • IFC [2:0] = B'000: Internal clock (Iϕ) frequency division ratio, × 1 • PFC [2:0] = B'001: Peripheral clock (Pϕ) frequency division ratio, × 1/2
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	Specifies clock for MTU2S • MSSCS[1:0] = B'01: The PLL output clock is selected as the source clock. • MSDIVS[1:0] = B'01: Division ratio for the source clock = 1/2
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	Specifies clock for AD converter • ASSCS[1:0] = B'01: The PLL output clock is selected as the source clock. • ASDIVS[1:0] = B'01: Division ratio for the source clock = 1/2

2.5.2 Power-Down Modes

Table 8 gives register settings related to low-power modes.

Table 8 Power-Down Modes

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFE 0408	H'5E	Controls the operation of various modules in power-down modes • HIZ = B'0: Pin states are held in software standby mode. • MSTP36 = B'1: Clock supply to MTU2S halted. • MSTP35 = B'0: MTU2 runs. • MSTP34 = B'1: Clock supply to POE2 halted. • MSTP33 = B'1: Clock supply to IIC3 halted. • MSTP32 = B'1: Clock supply to ADC0 halted.

2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 9 gives a list of settings for registers of multi-function timer pulse unit 2 (MTU2).

Table 9 Multi-Function Timer Pulse Unit 2 (MTU2)

Register Name	Address	Setting	Description
Timer control register_1 (TCR_1)	H'FFFE 4380	H'20	Sets details of TCNT control of Channel 1 • CCLR[2:0] = B'001: TCNT cleared on input capture • CKEG[1:0] = B'00: TCNT counts rising edge. • TPSC[2:0] = B'000: TCNT counts cycles of internal clock Pφ/1. Note: When channel 1 is set to phase-counting mode, settings made with bits TPSC[2:0] and CKEG[1:0] are ineffective (operation is in accord with the settings made for phase-counting mode). Regardless of the settings of these bits, the external clock signal is specified as the counter input clock, and TCNT functions as an up-/down-counter.
Timer counter_1 (TCNT_1)	H'FFFE 4386	H'0000	16-bit counter Cleared to 0
Timer general register A_1 (TGRA_1)	H'FFFE 4388	H'0000	Used as input-capture register Cleared to 0
Timer general register B_1 (TGRB_1)	H'FFFE 438A	H'0000	Used as input-capture register Cleared to 0
Timer mode register_1 (TMDR_1)	H'FFFE 4381	H'04	Sets operation mode. • MD[3:0] = B'0100: Phase counting mode 1
Timer I/O control register_1 (TIOR_1)	H'FFFE 4382	H'C8	Sets TGR operation. • IOB[3:0] = B'1100: Input capture in the TGRB_1 register on a compare match with TGRC_0 in channel 0 • IOA[3:0] = B'1000: Input capture in the TGRA_1 register on a rising edge
Timer interrupt enable register_1 (TIER_1)	H'FFFE 4384	H'33	Controls enabling or disabling of interrupt requests. • TTGE = B'0: Generation of requests to start the A/D converter is disabled. • TCIEU = B'1: Underflow interrupt request (TCIU) by TCFU is enabled. • TCIEV = B'1: Overflow interrupt request (TCIV) by TCFV is enabled. • TGIEB = B'1: Interrupt request (TGIB) by TGFB is enabled. • TGIEA = B'1: Interrupt request (TGIA) by TGFA is enabled.
Timer control register_0 (TCR_0)	H'FFFE 4300	H'A0	Sets details of TCNT control of channel 0. • CCLR[2:0] = B'101: TCNT is cleared on compare match with TGRC. • CKEG[1:0] = B'00: TCNT counts rising edge. • TPSC[2:0] = B'000: TCNT counts cycles of internal clock Pφ/1.
Timer counter_0 (TCNT_0)	H'FFFE 4306	H'0000	16-bit counter Cleared to 0
Timer general register A_0 (TGRA_0)	H'FFFE 4308	—	Not used in the sample program

Register Name	Address	Setting	Description
Timer general register B_0 (TGRB_0)	H'FFFE 430A	H'0000	Used as input-capture register Cleared to 0
Timer general register C_0 (TGRC_0)	H'FFFE 430C	D'49999	Used as compare-match register Compare-match cycle is set to 1 ms (1 ms/20 ns (50 MHz)) – 1 = D'50000 – 1 = D'49999
Timer general register D_0 (TGRD_0)	H'FFFE 430E	H'0000	Used as a buffer register for TGRB_0 Cleared to 0
Timer mode register_0 (TMDR_0)	H'FFFE 4301	H'20	Sets operation mode. • BFE = B'0: Specifies normal operation of TGRE_0 and TGRF_0 • BFB = B'1: Specifies buffered operation of TGRB and TGRD • BFA = B'0: Specifies normal operation of TGRA and TGRC • MD[3:0] = B'0000: Operating mode is normal.
Timer I/O control register H_0 (TIORH_0)	H'FFFE 4302	H'C0	Sets TGR operation. • IOB[3:0] = B'1100: TGRB_1 is an input-capture register. The counter clock of channel 1 initiates input capture operation, and input capture is generated when TCNT_1 counts up or down. • IOA[3:0] = B'0000: TGRA_0 is output-compare register.
Timer I/O control register L_0 (TIORL_0)	H'FFFE 4303	H'00	Sets TGR operation. • IOD[3:0] = B'0000: TGRD_0 is output-compare register. • IOC[3:0] = B'0000: TGRC_0 is output-compare register.
Timer interrupt enable register_0 (TIER_0)	H'FFFE 4304	H'02	Specifies enabling or disabling of interrupt requests. • TTGE = B'0: Generation of request to start A/D converter is disabled. • TCIEV = B'0: Overflow interrupt request (TCIV) by the TCFV bit is disabled. • TGIED = B'0: Interrupt request (TGID) by TGFD is disabled. • TGIEC = B'0: Interrupt request (TGIC) by TGFC is disabled. • TGIEB = B'1: Interrupt request (TGIB) by TGFB is enabled. • TGIEA = B'0: Interrupt request (TGIA) by TGFA is disabled.
Timer start register (TSTR)	H'FFFF 4280	H'03	Selects operation or stoppage of TCNT for channels 0 to 4. • CST1 = B'1: TCNT_1 counts • CST0 = B'1: TCNT_0 counts

2.5.4 Interrupt Controller (INTC)

Table 10 gives a list of settings for registers of the interrupt controller (INTC).

Table 10 Interrupt Controller (INTC)

Register Name	Address	Setting	Description
Interrupt priority registers 09 (IPR09)	H'FFFE 0C06	H'A0AA	Selects interrupt priority (level 0 to 15). • Bits 15 to 12 = B'1010: MTU0 (TGI0A to TGI0D) interrupt level = 10 • Bits 11 to 8 = B'0000: MTU0 (TCI0V, TGI0E, TGI0F) interrupt level = 0 • Bits 7 to 4 = B'1010: MTU1 (TGI1A, TGI1B) interrupt level = 10 • Bits 3 to 0 = B'1010: MTU1 (TCI1V, TCI1U) interrupt level = 10

2.5.5 Pin Function Controller (PFC)

Table 11 gives a list of settings for registers of the pin function controller (PFC).

Table 11 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port A control register L2 (PACRL2)	H'FFFE 3814	H'6600	Specifies functions of multiplexed pins on port A. PA7MD[2:0] = B'110: Specifies the TCLKB input (MTU2) for PA7. PA6MD[2:0] = B'110: Specifies the TCLKA input (MTU2) for PA6. PA5MD[2:0] = B'000: Specifies the PA5 I/O (port) for PA5. PA4MD[2:0] = B'000: Specifies the PA4 I/O (port) for PA4.
Port E control register L2 (PECRL2)	H'FFFE 3A14	H'0006	Specifies functions of multiplexed pins on port E. PE7MD[2:0] = B'000: Specifies the PE7 I/O (port) for PE7. PE6MD[2:0] = B'000: Specifies the PE6 I/O (port) for PE6. PE5MD[2:0] = B'000: Specifies the PE5 I/O (port) for PE5. PE4MD[2:0] = B'110: Specifies the TIOC1A I/O (MTU2) for PE4.
Port E I/O register L (PEIORL)	H'FFFE 3A06	H'0000	Specifies input and output directions for port E pins. PE15IOR to PE0IOR all set to B'0: PE15 to PE0 are input pins.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7280 Group Hardware Manual (REJ09B0393)
  The most up-to-date version of this document is available on the Renesas Technology Website.

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