

Renesas Synergy<sup>™</sup> Platform

R01AN3042EU0092 Rev.0.92

Migrating S7G2 MCUs Early Application Projects Nov 18, 2016

#### Introduction

This Application Note describes various options for migrating projects created in the development environment for S7G2 Early Samples to the development environment for S7G2 Mass Production devices.

Please note that as the complexity of the project to be migrated increases, the migration success rate will decrease. In addition, the more components of the S7G2 Early Sample development environment being migrated to the Mass Production development environment, the more difficult the migration process will be.

If you are having trouble migrating your project, it is suggested to re-create your project in the development environment for Mass Production devices by creating a new project and bringing in your application-specific code.

#### Target Devices

R7F5A00Z03CBG:S7G2 224-pin BGA Early SampleR7FS7G27H2A01CBD:S7G2 224-pin BGA Mass Production device

Note: If you are using a different S7G2 device (e.g. the S7G2 176-pin LQFP device, part number R7FS7G27H2A01CFC), you can still follow this Application Note. Substitute references to part number R7FS7G27H2A01CBD in this document for the part number of the device you're using.

#### **Intended Audience**

The intended audience for this Application Note are developers who have created projects in the Renesas Synergy Development Environment supporting S7G2 Early Samples and would like to migrate those projects to the Renesas Synergy Development Environment supporting S7G2 Mass Production devices. It is also intended for developers who want to continue using their existing Synergy Development Environment supporting S7G2 Early Samples but upgrade the SSP to Revision v1.0.0 or later.



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#### 1. S7G2 Development Environments

#### 1.1 S7G2 Early Sample Development Environment

Until Q3 of 2015, the Renesas Synergy Development Environment supported the S7G2 224-pin BGA Early Samples with the following part marking:

## SYNERGY R7F5A00Z03CBG

The development environment components were as follows:

Environment component	Version(s)	Comment
SSP	0.91.0x	Synergy Software Package
e <sup>2</sup> studio	4.0.1.015	Integrated Solutions Development Environment (ISDE)
PE-HMI1 Product Example (Early Sample)	1.x	See sticker on the board for identification
DK-S7G2 Development Kit (Early Sample)	1.x; 2.x	See sticker on the board for identification

#### **1.2 S7G2 Mass Production Development Environment**

From October 2015 onwards, the Renesas Synergy Development Environment supports the S7G2 224-pin BGA Mass Production devices with the following part marking:

## SYNERGY R7FS7G27H2A01CBD

The development environment components are as follows:

Environment component	Version(s)	Comment
SSP	1.0.0	Synergy Software Package
e <sup>2</sup> studio	4.2.0.012 and later	Integrated Solutions Development Environment
PE-HMI1 Product Example (Mass Production)	2.0	See sticker on the board for identification
DK-S7G2 Development Kit (Mass Production)	3.0	See sticker on the board for identification

NOTE: Please make sure you are NOT installing  $e^2$  studio version 4.2.0.012 over an existing installation of version 4.0.1.015. Install the 4.2.0.012 to a different directory.



#### 2. Migration Option Overview

Migration Option	Renesas Synergy Environment before migration			<b>→</b>	Renesas Synergy Environment after migration		
	SSP	e <sup>2</sup> studio	Boards		SSP	e <sup>2</sup> studio	Boards
Option 1	v0.91.0x	v4.0.1.015	Early Sample	<b>&gt;</b>	v0.91.0x	v4.2.0.012 and later	Early Sample
Option 2	v0.91.0x	v4.0.1.015	Early Sample	<b>&gt;</b>	v1.0.0	v4.2.0.012 and later	Early Sample
Option 3	v0.91.0x	v4.0.1.015	Early Sample	<b>&gt;</b>	v0.91.0x	v4.2.0.012 and later	Mass Production
Option 4	v0.91.0x	v4.0.1.015	Early Sample	<b>→</b>	v1.0.0	v4.2.0.012 and later	Mass Production

This application note covers the following migration options.

# 3. Migration Option 1: Migrate to e<sup>2</sup> studio v4.2.0.012, but keep using SSP v0.91.0x and S7G2 Early Sample boards

Use Migration Option 1 if you would like to keep using SSP v0.91.0x and your existing Early Sample boards (PE-HMI1 v1.x / DK-S7G2 v1.x / 2.x), but you would like to upgrade to the latest  $e^2$  studio ISDE version.

The migration is accomplished by exporting the project you created from your current S7G2 Early Sample environment and importing it into e<sup>2</sup> studio v4.2.0.012.

Current Renesas Synergy Environment	<b>→</b>	Renesas Synergy Environment after migration
SSP v0.91.0x		SSP v0.91.0x (no change)
e <sup>2</sup> studio v4.0.1.015	<b>→</b>	e <sup>2</sup> studio v4.2.0.012 and later
PE-HMI1 Product Example v1.x		PE-HMI1 Product Example v1.x (no change)
DK-S7G2 Development Kit v1.x / 2.x		DK-S7G2 Development Kit v1.x / 2.x (no change)

In order to implement this migration option, please follow the following steps.

#### 3.1 Step 1: Export your project from the S7G2 Early Sample Software Development Environment

- a) Open your project in  $e^2$  studio v4.0.1.015.
- b) Right-click in the Project Explorer area and select "Export".
- c) Select "General  $\rightarrow$  Archive File" as the export destination
- d) Click "Next"
- e) Click "Browse" and navigate to the location of your choice.
- f) Enter a file name and click "Save".
- g) Click "Finish".
- h) Close  $e^2$  studio v4.0.1.015.

#### 3.2 Step 2: Install the S7G2 Mass Production Software Development Environment

- a) Download and install e<sup>2</sup> studio v4.2.0.012 from the Renesas Synergy Gallery (<u>https://synergygallery.renesas.com</u>). Registration is required.
- b) Download and install SSP v1.0.0 from the Renesas Synergy Gallery into the e<sup>2</sup> studio v4.2.0.012 installation folder. (Even though you will not be using SSP v1.0.0 in your migrated project.)



#### 3.3 Step 3: Switch the S7G2 224-pin BGA Pin Configurator in the Mass Production Environment to support S7G2 Early Samples

- a) Make sure  $e^2$  studio v4.2.0.012 is closed.
- b) Navigate to the following folder:  $\langle ISDE\_base\_dir \rangle \langle internal \rangle projectgen \rangle arm \rangle pinmapping \rangle$
- c) Rename file 'PinCfgS7G27BD.xml' to 'PinCfgS7G27BD\_WS2.xml'
- d) Rename file 'PinCfgS7G27BD\_WS1.xml' to 'PinCfgS7G27BD.xml'
- e) Do not restart  $e^2$  studio v4.2.0.012 just yet.

#### 3.4 Step 4: Transfer SSP v0.91.0x into e<sup>2</sup> studio v4.2.0.012

- a) Navigate to the following folder: <e2\_studio\_v4.0.1.015\_base\_dir>/internal/projectgen/arm/Packs/
- b) Select all files in the folder referenced above, and copy & paste them into the following folder: <e2\_studio\_v4.2.0.012\_base\_dir>/internal/projectgen/arm/Packs/

#### 3.5 Step 5: Import your project into the S7G2 Mass Production Software Development Environment

- a) Start  $e^2$  studio v4.2.0.012.
- b) Select a suitable workspace.
- c) Right-click in the Project Explorer area and select "Import".
- d) Select "General  $\rightarrow$  Existing Projects into Workspace" as the import source.

e <sup>2</sup> Import	
Select Create new projects from an archive file or directory.	Ľ
Select an import source:	
type hiter text	
(?)	Cancel

- e) Click "Next"
- f) Click "Select Archive File"
- g) Click "Browse" and navigate to the location of the project you exported earlier.



h) Select the project to be imported and click "Open".

6² Import	_ 🗆 🗙
Import Projects Select a directory to search for existing Edipse projects.	
Select root directory:     Select archive file:     C:\workspace\WeatherPanel.zip  Projects:	Browse Browse
- 🗹 WeatherPanel (WeatherPanel)	Select All Deselect All Refresh
Options         Search for nested projects         Copy projects into workspace         Hjde projects that already exist in the workspace         Working sets         Add project to working sets         Working sets:	Sglet
C      Eack Mext > Einish	Cancel

i) Click "Finish" and wait for e<sup>2</sup> studio to finish importing your project.

#### 3.6 Step 6: Open the project in the Synergy Project Editor

- a) Expand the imported project in the Project Explorer view.
- b) Double-click on the configuration.xml file to invoke the Renesas Synergy Project Editor.



- c) If you see a window asking whether you would like to switch to the latest available SSP version (1.0.0), click "**No**". (If you would like to switch, use Migration Option 2 in this document.)
- d) If you see the window below, click "Yes".





e) In the Synergy Project Editor, click the Components tab. Make sure there are no 🙆 marks anywhere.

mponents		
		1
ponent	Version	Description
🖉 BSP		
🖃 🧼 BSP		
s3a7_dk	0.91.02	Board Support Package for S3A7_DK
s3a7_dk	0.91.01	Board Support Package for S3A7_DK
s3a7_dk	0.91.00	Board Support Package for S3A7_DK
s3a7_user	0.91.02	Board Support Package for S3A7_USER
s3a7_user	0.91.01	Board Support Package for S3A7_USER
s7g2_dk	0.91.02	Board Support Package for S7G2_DK
s7g2_dk	0.91.01	Board Support Package for S7G2_DK
s7g2_dk	0.91.00	Board Support Package for S7G2_DK
<pre>s7g2_pe_hmi1</pre>	0.91.02	Board Support Package for S7G2_PE_HMI1
s7g2_pe_hmi1	0.91.01	Board Support Package for S7G2_PE_HMI1
s7g2_pe_hmi1	0.91.00	Board Support Package for S7G2_PE_HMI1
s7g2_user	0.91.02	Board Support Package for S7G2_USER
s7g2_user	0.91.01	Board Support Package for S7G2_USER
Documentation		
Express Logic		
) 🧼 all		
🔲 fx	0.91.00	Express Logic FileX: Provides=[FileX] , Requires=[FileX I/O ,ThreadX]
m fx	0.91.01	Express Logic FileX: Provides=[FileX] , Requires=[FileX I/O ,ThreadX]
V gx	0.91.02	Express Logic GUIX: Provides=[GUIX] , Requires=[ThreadX]
gx gx	0.91.00	Express Logic GUIX: Provides=[GUIX] , Requires=[ThreadX]
nx	0.91.00	Express Logic NetX: Provides=[NetX] , Requires=[ThreadX ,NetX Driver]
nx_dhcp	0.91.00	Express Logic NetX DHCP: Provides=[NetX DHCP], Requires=[NetX]
nx_dhcp_server	0.91.00	Express Logic NetX DHCP Server: Provides=[NetX DHCP Server], Requi
nx_dns	0.91.00	Express Logic NetX DNS: Provides=[NetX DNS] , Requires=[NetX]
nx_ftp_dient	0.91.00	Express Logic NetX FTP Client: Provides=[NetX FTP Client] , Requires=[I
nx_ftp_server	0.91.00	Express Logic NetX FTP Server: Provides=[NetX FTP Server] , Requires=
nx_http_client	0.91.00	Express Logic NetX HTTP Client: Provides=[NetX HTTP Client] , Requires
nx_http_server	0.91.00	Express Logic NetX HTTP Server: Provides=[NetX HTTP Server] , Requin
nx_telnet_client	0.91.00	Express Logic NetX Telnet Client: Provides=[NetX Telnet Client] , Requin
nx telnet server	0.91.00	Express Logic NetX Telnet Server: Provides=[NetX Telnet Server] . Regu

Note: If you see  $\triangle$  marks anywhere in the Components tab, you may not have copied over all SSP v0.91.0x packs from your e<sup>2</sup> studio v4.0.1.015 ISDE.

#### 3.7 Step 7: Verify the Threads tab

- a) Click on the Threads tab in the Synergy Project Editor.
- b) Open your original project in  $e^2$  studio v4.0.1.015.
- c) Make sure that your project in  $e^2$  studio v4.0.1.015 and your project in  $e^2$  studio v4.2.0.012 have:
  - i. Exactly the same components list
  - ii. Exactly the same properties for each module

Since the SSP version is the same, there should be no difference.

🔅 Synergy Configuration [WeatherPanel] 🛛		
Threads	(	Senerate Project Content
Threads         Image: Sec CGC Driver on CGC         g_cgc CGC Driver on ELC         g_oport IOPORT Driver on IOPORT         Image: HMIT Thread         g_dsplay DISPLAY Module on GLCD         g_nymm_baddight PWM Driver on GPT11         g_12c12C Driver on RIIC1	HMI Thread Modules	Remove
	HMI Thread Objects <ul> <li>g_hmi_queue Queue</li> </ul>	New >
The contents in the Threads tab sh e <sup>2</sup> studio v4.0.1.015 (see above) ar	ould be same between your project in d e <sup>2</sup> studio v4.2.0.012 (see below).	

🔅 Synergy Configuration [WeatherPanel] 🔀			
Threads		Q Generate Project	t Content
Threads		HMI Thread Modules	
<pre>% HAL/Common g_cgc CGC Driver on ELC g_loport IOPORT Driver on IOPORT % HML Thread g_display DISPLAY Module on GLCD g_pwm_baddight PVM Driver on GPT11 g_12c 12C Driver on RIIC1</pre>	New           Remove		w >

#### 3.8 Step 8: Check ICU settings

- a) Click on the ICU tab in the Synergy Project Editor.
- b) Make sure that your project in e<sup>2</sup> studio v4.0.1.015 and your project in e<sup>2</sup> studio v4.2.0.012 have exactly same IRQ settings.

#### 3.9 Step 9: Point your project to a valid Synergy License file

- a) In e<sup>2</sup> studio v4.2.0.012, right-click on your project in the Project Explorer view and select "Properties" from the menu.
- b) Expand the "C/C++ General" section and click on "Synergy License"
- c) Browse to a valid Synergy License file, e.g. to the Evaluation License here: <e2\_studio\_v4\_2\_0\_012\_base\_dir>\internal\projectgen\arm\Licenses\
- d) Click "OK".

#### 3.10 Step 10: Build your project in e<sup>2</sup> studio v4.2.0.012

- a) Select "Project  $\rightarrow$  Clean" from the menu
- b) Check "Clean projects selected below", "Start a build immediately", and "Build only the selected projects".
- c) Click OK to clean your project and build it.
- d) Confirm there are no compilation errors.

#### 3.11 Step 11: Download and run your project

- a) Connect your target hardware to your PC via a Segger J-Link, J-Link-Lite, or J-Link On-Board.
- b) Select "Run  $\rightarrow$  Debug Connections" from the menu
- c) Select your project's debug configuration under "Renesas GDB Hardware Debugging".
- d) After the debug configuration has loaded, click "Debug".
- e) Run your project to confirm proper operation.

**Note:** To switch the Pin Configurator support back to S7G2 224-pin BGA Mass Production devices, revert the changes you made in Step 3 above:

- a) Close down  $e^2$  studio v4.2.0.012.
- c) Rename file 'PinCfgS7G27BD.xml' back to 'PinCfgS7G27BD\_WS1.xml'



- d) Rename file 'PinCfgS7G27BD\_WS2.xml' back to 'PinCfgS7G27BD.xml'
- e) Restart  $e^2$  studio v4.2.0.012.

Now you can create a new Synergy Project for an S7G2 224-pin BGA Mass Production device again.

# 4. Migration Option 2: Migrate to SSP v1.0.0 and e<sup>2</sup> studio v4.2.0.012, but keep using S7G2 Early Sample boards

Use Migration Option 2 if you would like to keep using your existing Early Sample boards (PE-HMI1 v1.x / DK-S7G2 v1.x / 2.x), but you would like to upgrade to the latest SSP and  $e^2$  studio ISDE versions.

The migration is accomplished by exporting the project you created from your current S7G2 Early Sample environment, importing it into e<sup>2</sup> studio v4.2.0.012, and migrating it to SSP v1.0.0.

Current Renesas Synergy Environment	<b>→</b>	Renesas Synergy Environment after migration
SSP v0.91.0x	<b>→</b>	SSP v1.0.0
e <sup>2</sup> studio v4.0.1.015	<b>→</b>	e <sup>2</sup> studio v4.2.0.012 and later
PE-HMI1 Product Example v1.x		PE-HMI1 Product Example v1.x (no change)
DK-S7G2 Development Kit v1.x / 2.x		DK-S7G2 Development Kit v1.x / 2.x (no change)

In order to implement this migration option, please follow the following steps.

#### 4.1 Step 1: Export your project from the S7G2 Early Sample Software Development Environment

- a) Open your project in  $e^2$  studio v4.0.1.015.
- b) Right-click in the Project Explorer area and select "Export".
- c) Select "General  $\rightarrow$  Archive File" as the export destination
- d) Click "Next"
- e) Click "Browse" and navigate to the location of your choice.
- f) Enter a file name and click "Save".
- g) Click "Finish".
- h) Close  $e^2$  studio v4.0.1.015.

#### 4.2 Step 2: Install the S7G2 Mass Production Software Development Environment

- a) Download and install e<sup>2</sup> studio v4.2.0.012 from the Renesas Synergy Gallery (<u>https://synergygallery.renesas.com</u>). Registration is required.
- b) Download and install SSP v1.0.0 from the Renesas Synergy Gallery into the e<sup>2</sup> studio v4.2.0.012 installation folder.

#### 4.3 Step 3: Switch the S7G2 224-pin BGA Pin Configurator in the Mass Production Environment to support S7G2 Early Samples

- a) Make sure  $e^2$  studio v4.2.0.012 is closed.
- b) Navigate to the following folder:  $\langle ISDE\_base\_dir \rangle \langle internal \rangle projectgen \rangle arm \rangle pinmapping \rangle$
- c) Rename file 'PinCfgS7G27BD.xml' to 'PinCfgS7G27BD\_WS2.xml'
- d) Rename file 'PinCfgS7G27BD\_WS1.xml' to 'PinCfgS7G27BD.xml'

#### 4.4 Step 4: Import your project into the S7G2 Mass Production Software Development Environment

- a) Start  $e^2$  studio v4.2.0.012.
- b) Select a suitable workspace.

- c) Right-click in the Project Explorer area and select "Import".
- d) Select "General  $\rightarrow$  Existing Projects into Workspace" as the import source.

e <sup>2</sup> Import	<u>- 🗆 ×</u>
Select Create new projects from an archive file or directory.	Ľ
Select an import source: type filter text General CMSIS Pack CMSIS Pack CMSIS Pack CMSIS Pack CMSIS Pack CMSIS Projects into Workspace File System CMSIS Project Site File System CHE Project Preferences CPC++ CCS CPC++ CCS CPC++ COS Distall CPC Team	
? < Back Next > Einish	Cancel

- e) Click "Next"
- f) Click "Select Archive File"
- g) Click "Browse" and navigate to the location of the project you exported earlier.
- h) Select the project to be imported and click "Open".

1 0					<u> </u>
e <sup>2</sup> Import					_ 🗆 🗙
Import Projects Select a directory to search	ch for existing Ec	lipse projects.			
C Select root directory:				7	Browse
Select archive file:	C:\workspace\	WeatherPanel.	zip	•	Browse
Projects:					
WeatherPanel (W	(eatherPanel)				Select All
					Deselect All
					Refresh
Options	- / h -				
Copy projects into w	ojects orkspace				
Hide projects that alr	eady exist in the	e workspace			
Working sets					
Add project to work	ing sets				
Working sets:				~	Select
(?)		< <u>B</u> ack	Next >	Einish	Cancel

i) Click "Finish" and wait for e<sup>2</sup> studio to finish importing your project.

#### 4.5 Step 5: Open the project in the Synergy Project Editor

a) Expand the imported project in the Project Explorer view.

b) Double-click on the configuration.xml file to invoke the Renesas Synergy Project Editor.



c) If you see a window asking whether you would like to switch to the latest available SSP version (1.0.0), click "**Yes**". (If you would like to stay with the older SSP version, use Migration Option 1 in this document.)

e <sup>2</sup> e2 st	tudio X
	Warning: Pack missing for project's current selected SSP version of 0.91.03.
	If you remain with this SSP version you will not be able to add further SSP components or re-extract SSP source files.
	Would you like to switch to latest available SSP version? (1.0.0)
Ren	nember my decision
	Yes No Cancel

d) In the Synergy Project Editor, click the Components tab. Make sure there are no 🙆 marks anywhere.

#### 4.6 Step 6: Verify / Update the Threads tab

- a) Click on the Threads tab in the Synergy Project Editor.
- b) Open your original project in  $e^2$  studio v4.0.1.015.
- c) Compare the modules in the Thread Modules panes between your original project in e<sup>2</sup> studio v4.0.1.015 / SSP v0.91.0x and your imported project in e<sup>2</sup> studio v4.2.0.012 / SSP v1.0.0. You will notice that the Module names in SSP v1.0.0 have changed somewhat compared to v0.91.0x, but you will still be able to identify which v0.91.0x module corresponds to which v1.0.0 module.



SSP v0.91.0x Modules

SSP v1.0.0 Modules

d) Compare all the SSP Module property settings in the Properties View between your original project in e<sup>2</sup> studio v4.0.1.015 / SSP v0.91.0x and your imported project in e<sup>2</sup> studio v4.2.0.012 / SSP v1.0.0. (When you updated your SSP version to v1.0.0, the module settings were reset to their default values. Therefore you need to edit any modified module properties manually. Be sure not to miss any properties).



e) You may see some missing modules that were present in your SSP v0.91.0x project but are not present in your SSP v1.0.0 project. For instance, you may notice that the PWM Driver on GPTxx, which was present in your SSP v0.91.0x project, is missing for SSP v1.0.0 (see picture in Step 6c). This is because SSP v1.0.0 no longer supports a stand-alone PWM Driver on GPT module. Instead, PWM is supported by the Timer Driver on r\_gpt (see picture below).

You may also see additional modules. For instance, the D/AVE 2D Driver on dave 2d was not present in your SSP v0.91.0x project but is present now in your SSP v1.0.0 project (see picture in Step 6c). This is because SSP v1.0.0 now allows to select the SSP component in the Modules selection pane on the Synergy Project Editor Threads tab. In SSP v0.91.0x, you could only select the D/AVE 2D Driver from the Components tab.

It is possible to swap a module between SSP versions or use an alternative module or new module from the new SSP pack. Please refer to the SSP Pack Release Notes for the differences between such modules, or contact Renesas for more information.

HMI Thread Modules		B P109	P108	¥9301	vcc	vcc	P312	P912	P200	VLO	VSS
g_display Display Driver on r_glcd     g_ize_zze_zze_zie_zie_zie_zie_zie_zie_zie	New : Driver		Ana	log	✓   · ►	09	P310	P311	P201	P904	VSS
g_lzc 12C Driver on r_nic g_external_irq External IRQ Driver on r_icu	Remov Frame	work 🕨	Con	nectivi	ity 🕨	06	¥9307	¥308	P910	P903	vcc
g_sf_external_irq External IRQ Framework on sf_external_irq     a of managed Magazing Framework on of magazing		E P61	Inpu	it		14	¥915	¥908	¥909	¥900	P313
<ul> <li>g_s1_message Messaging Framework on s1_message</li> <li>g_sf_touch_panel_i2c Touch Panel Framework on sf_touch_panel_i2c</li> </ul>		F P61	Mon	itoring		00	¥906	¥907	RES	¥314	P710
g_sf_el_gx GUIX Port on sf_el_gx     Ave a start of the address     Ave address     Ave a start of the address     A		G 981	Stor	er age		12	PA11	PAOS	P615	¥206	P713
<ul> <li>g_sf_jpeg_decode JPEG Decode Framework on sf_jpeg_decode</li> </ul>		H VCL	Time	rs	•		RTC D	river	on r_r	tc	
g_jpeg_decode JPEG Decode Driver on r_jpeg		3 PA0	7 PAO6	PA05	PA04		Timer	Driver	r on r	_agt _gpt	
W GUIX on gx		~	<b>v</b>	<b>~</b>	<b>~</b>	-	<ul> <li></li> </ul>				

f) If you added new SSP v1.0.0 modules to your project as alternatives for SSP v0.91.0x modules that are no longer supported in v1.0.0, configure the module properties in the Properties View.

		🔲 Properties 🔀 🚼 Problems	
		Property	Value
Properties 🔀 🚼 Problems		Common	
Property	Value	Parameter Checking	Enabled
Common		⊟ ICU	
Param Checking Enable	Enabled	GPT11 COUNTER OVERFLOW	Disabled
Module		Module	
Name	g_pwm_backlight	Name	g_pwm_backlight
Period	10	Channel	11
Period Unit	Unit Period Msec	Mode	PWM
Duty Cyde	50	Period Value	10
Duty Cyde Unit	Unit Percent	Period Unit	Milliseconds
Channel	11	Duty Cyde Value	50
Autostart	True	Duty Cycle Unit	Unit Percent
Gtioca Output Enabled	True	Auto Start	True
Gtioca Stop Level	Pin Level Low	GTIOCA Output Enabled	True
Gtiocb Output Enabled	False	GTIOCA Stop Level	Pin Level Low
Gtiocb Stop Level	Pin Level Low	GTIOCB Output Enabled	False
Callback	NULL	GTIOCB Stop Level	Pin Level Low
		Callback	NULL

V0.91.03 (PWM Driver on GPTnn)

v1.0.0 (Timer Driver on r\_gpt)

#### 4.7 Step 7: Enable FPU support

SSP v1.0.0 now supports FPU. This is one of the major differences between SSP v0.91.0x and v1.0.0.

- a) Go to Project  $\rightarrow$  Properties
- b) Go to C/C++ Build  $\rightarrow$  Settings
- c) On the Tool Settings tab, click on Target Processor

d) Change the Float ABI setting to 'FP instructions (hard)' since SSP v1.0.0 does support FPU (VFPv4).

e <sup>2</sup> Properties for WeatherPanel				JN
type filter text	Settings		← → →	-
Builders				-41
⊡ C/C++ Build	Configuration: Debug [Active]		Manage Configurations	
Build Variables				
Environment				- 11
Settings	🛞 Tool Settings 🎤 Build Steps 🖳 😤 Build Artifa	ict 🛞 Toolchain	🗟 Binary Parsers 🛛 📀 Error Parsers	
Tool Chain Editor				
□ C/C++ General	Target Processor	ARM family	cortex-m4	
Code Analysis	Optimization	Architecture	Toolchain default	
Documentation	Warnings			
File Types	Debugging	Instruction set	Thumb (-mthumb)	
Formatter	Cross ARM GNU Assembler	Thumb interwor	rk (-mthumb-interwork)	
Indexer	Preprocessor	Endianness	Toolchain default	
Language Mappings	Includes	chuidhineaa		
Preprocessor Include Path	Wissellangeus	Float ABI	FP instructions (hard)	
- Synergy Builder	E R Cross ARM C Compiler	FPU Type	fpv4-sp-d16	
Synergy License				
···· Project References		Unaligned access	Toolchain default	
···· Refactoring History	Optimization	AArch64 Family	Generic (-mcpu=generic)	
Run/Debug Settings		Easterna and	Tradichasia da fault	
		reature crc		
	E Cross ARM C Linker	Feature crypto	Toolchain default	
	- Ceneral	Feature fo	Toolchain default	
	Libraries	i oacaro ip		
	Miscellaneous	Feature simd	Enabled (+simd)	
	Cross ARM GNU Create Flash Image	Code model	Small (-mcmodel=small)	
		Strict align (-ms	trict-align'	
	General	- Serve angri ( ins	since any i	
	General	Other target flags		
				١Ŀ
<b>√</b>	<u> </u>			-
?			OK Cancel	

#### 4.8 Step 8: Check ICU settings

- a) Click on the ICU tab in the Synergy Project Editor.
- b) Make sure that your project in e<sup>2</sup> studio v4.0.1.015 and your project in e<sup>2</sup> studio v4.2.0.012 have exactly the same IRQ settings. This task is a bit tedious because the structure and the naming of the ICU settings has changed. See the Appendix for a list of old names vs. new names.

#### 4.9 Step 9: Point your project to a valid Synergy License file

- a) In e<sup>2</sup> studio v4.2.0.012, right-click on your project in the Project Explorer view and select "Properties" from the menu.
- b) Expand the "C/C++ General" section and click on "Synergy License"
- c) Browse to a valid Synergy License file, e.g. to the Evaluation License here: <e2\_studio\_v4\_2\_0\_012\_base\_dir>\internal\projectgen\arm\Licenses\
- d) Click "OK".

#### 4.10 Step 10: Build your project in e<sup>2</sup> studio v4.2.0.012

- a) Select "Project  $\rightarrow$  Clean" from the menu
- b) Check "Clean projects selected below", "Start a build immediately", and "Build only the selected projects".
- c) Click OK to clean your project and build it.
- d) Confirm there are no compilation errors.

#### 4.11 Step 11: Download and run your project

- a) Connect your target hardware to your PC via a Segger J-Link, J-Link-Lite, or J-Link On-Board.
- b) Select "Run  $\rightarrow$  Debug Connections" from the menu



- c) Select your project's debug configuration under "Renesas GDB Hardware Debugging".
- d) After the debug configuration has loaded, click "Debug".
- e) Run your project to confirm proper operation.

**Note:** To switch the Pin Configurator support back to S7G2 224-pin BGA Mass Production devices, revert the changes you made in Step 3 above:

- a) Close down  $e^2$  studio v4.2.0.012.
- b) Navigate to the following folder: <ISDE\_base\_dir>\internal\projectgen\arm\pinmapping\
- c) Rename file 'PinCfgS7G27BD.xml' back to 'PinCfgS7G27BD\_WS1.xml'
- d) Rename file 'PinCfgS7G27BD\_WS2.xml' back to 'PinCfgS7G27BD.xml'
- e) Restart  $e^2$  studio v4.2.0.012.

Now you can create a new Synergy Project for an S7G2 224-pin BGA Mass Production device again.

# 5. Migration Option 3: Migrate to e<sup>2</sup> studio v4.2.0.012 and Mass Production boards, but keep using SSP v0.91.0x

Use this Migration Option if you have updated hardware populated with Mass Production devices (PE-HMI1 v2.0 / DK-S7G2 v3.0) and you would like to upgrade to the latest  $e^2$  studio ISDE version.

The migration is accomplished by exporting the project you created from your current S7G2 Early Sample environment, importing it into e<sup>2</sup> studio v4.2.0.012, and running it on a Mass Production board.

Current Renesas Synergy Environment	→	Renesas Synergy Environment after migration
SSP v0.91.0x		SSP v0.91.0x (no change)
e <sup>2</sup> studio v4.0.1.015	<b>→</b>	e <sup>2</sup> studio v4.2.0.012 and later
PE-HMI1 Product Example v1.x	<b>→</b>	PE-HMI1 Product Example v2.0
DK-S7G2 Development Kit v1.x / 2.x	→	DK-S7G2 Development Kit v3.0

In order to implement this migration option, please follow these steps:

#### 5.1 Step 1: Export your project from the S7G2 Early Sample Software Development Environment

- a) Open your project in  $e^2$  studio v4.0.1.015.
- b) Right-click in the Project Explorer area and select "Export".
- c) Select "General  $\rightarrow$  Archive File" as the export destination
- d) Click "Next"
- e) Click "Browse" and navigate to the location of your choice.
- f) Enter a file name and click "Save".
- g) Click "Finish".
- h) Close  $e^2$  studio v4.0.1.015.

#### 5.2 Step 2: Install the S7G2 Mass Production Software Development Environment

- a) Download and install e<sup>2</sup> studio v4.2.0.012 from the Renesas Synergy Gallery (<u>https://synergygallery.renesas.com</u>). Registration is required.
- b) Download and install SSP v1.0.0 from the Renesas Synergy Gallery into the e<sup>2</sup> studio v4.2.0.012 installation folder. (Even though you will not be using SSP v1.0.0 in your migrated project.)



#### 5.3 Step 3: Transfer SSP v0.91.0x into e<sup>2</sup> studio v4.2.0.012

- a) If  $e^2$  studio v4.2.0.012 is running, close it down.
- b) Navigate to the following folder: <e2\_studio\_v4.0.1.015\_base\_dir>/internal/projectgen/arm/Packs/
- c) Copy all files in the folder referenced above, and paste them into the following folder: <e2\_studio\_v4.2.0.012\_base\_dir>/internal/projectgen/arm/Packs/

#### 5.4 Step 4: Import your project into the S7G2 Mass Production Software Development Environment

- a) Start  $e^2$  studio v4.2.0.012.
- b) Select a suitable workspace.
- c) Right-click in the Project Explorer area and select "Import".
- d) <u>Select "General → Existing Projects into Workspace" as the import source</u>.

Select Create new projects from an archive file or directory.  Select an import source:  type filter text  General  General  Given Size Spack  File System  File System File System  File System  File System  File System  File System  File System  File System  File System  File System  File System  File S	<u>2</u>
Select an import source: type filter text CMSIS Pack File System File System Proferences Free System Proferences	_
type filter text	
General     G	
C/C++     Fename & Import Existing C/C++ Project into Workspace     Fenesas Common Project File     C/C++     CVS     C/S     For Install     CRun/Debug     For Team	
2 Clark Next > Einich	Cancel

- e) Click "Next"
- f) Click "Select Archive File"
- g) Click "Browse" and navigate to the location of the project you exported earlier.



h) Select the project to be imported and click "Open".

e <sup>2</sup> Import	
Import Projects Select a directory to search for existing Edipse projects.	
Select root directory:     Select archive file:     C:\workspace\WeatherPanel.zp	Browse
Projects:	
WeatherPanel (WeatherPanel)	Select All
	Deselect All
	Refresh
Options     Search_for nested projects     Gopy projects into workspace     Hide projects that already exist in the workspace	
Working sets	
Add project to working sets       Wgrking sets:	Sglect
< Back         Mext >         Einish	Cancel

i) Click "Finish" and wait for e<sup>2</sup> studio to finish importing your project.

#### 5.5 Step 5: Open the project in the Synergy Project Editor

- a) Expand the imported project in the Project Explorer view.
- b) Double-click on the configuration.xml file to invoke the Renesas Synergy Project Editor.



- c) If you see a window asking whether you would like to switch to the latest available SSP version (1.0.0), click "**No**". (If you would like to switch, use Migration Option 4 in this document.)
- d) If you see the window below, click "Yes".





e) In the Synergy Project Editor, click the Components tab. Make sure there are no 🤼 marks anywhere.

🌼 Synergy Configuration [WeatherPanel] 🔀		
Components		
Component	Version	Description
😑 🌧 BSP		
🖃 🥥 BSP		
s3a7_dk	0.91.02	Board Support Package for S3A7_DK
s3a7_dk	0.91.01	Board Support Package for S3A7_DK
s3a7_dk	0.91.00	Board Support Package for S3A7_DK
s3a7_user	0.91.02	Board Support Package for S3A7_USER
s3a7_user	0.91.01	Board Support Package for S3A7_USER
s7g2_dk	0.91.02	Board Support Package for S7G2_DK
s7g2_dk	0.91.01	Board Support Package for S7G2_DK
s7g2_dk	0.91.00	Board Support Package for S7G2_DK
s7g2_pe_hmi1	0.91.02	Board Support Package for S7G2_PE_HMI1
s7g2_pe_hmi1	0.91.01	Board Support Package for S7G2_PE_HMI1
s7g2_pe_hmi1	0.91.00	Board Support Package for S7G2_PE_HMI1
s7g2_user	0.91.02	Board Support Package for S7G2_USER
s7g2_user	0.91.01	Board Support Package for S7G2_USER
🖃 👧 Express Logic		
🖃 🥥 all		
fx fx	0.91.00	Express Logic FileX: Provides=[FileX], Requires=[FileX I/O, ThreadX]
m fx	0.91.01	Express Logic FileX: Provides=[FileX] , Requires=[FileX I/O ,ThreadX]
🔽 gx	0.91.02	Express Logic GUIX: Provides=[GUIX] , Requires=[ThreadX]
m gx	0.91.00	Express Logic GUIX: Provides=[GUIX] , Requires=[ThreadX]
nx	0.91.00	Express Logic NetX: Provides=[NetX] , Requires=[ThreadX ,NetX Driver]
nx_dhcp	0.91.00	Express Logic NetX DHCP: Provides=[NetX DHCP], Requires=[NetX]
nx_dhcp_server	0.91.00	Express Logic NetX DHCP Server: Provides=[NetX DHCP Server] , Requires
nx_dns	0.91.00	Express Logic NetX DNS: Provides=[NetX DNS] , Requires=[NetX]
nx_ftp_dient	0.91.00	Express Logic NetX FTP Client: Provides=[NetX FTP Client] , Requires=[NetX]
nx_ftp_server	0.91.00	Express Logic NetX FTP Server: Provides=[NetX FTP Server] , Requires=[
nx_http_dient	0.91.00	Express Logic NetX HTTP Client: Provides=[NetX HTTP Client] , Requires=[
nx_http_server	0.91.00	Express Logic NetX HTTP Server: Provides=[NetX HTTP Server] , Requires
nx_telnet_client	0.91.00	Express Logic NetX Telnet Client: Provides=[NetX Telnet Client] , Requires
nx_telnet_server	0.91.00	Express Logic NetX Telnet Server: Provides=[NetX Telnet Server] , Requir
Summary 这 BSP Clocks Pins Threads ICU Components		

Note: If you see  $\triangle$  marks anywhere in the Components tab, you may not have copied over all SSP v0.91.0x packs from your e<sup>2</sup> studio v4.0.1.015 ISDE.

#### 5.6 Step 6: Update the Pin Configuration file

In this step you need to either update or recreate your existing .pincfg file (your Pin Configuration file) in your  $e^2$  studio project. This file is no longer valid for the Mass Production board, since the pinout of the MCU is different between the Early Samples and the Mass Production devices.

a) Rename the .pincfg file in your e<sup>2</sup> studio project to R7FS7G27H2A01CBD\_old.pincfg.



- b) If your project was originally **based on a Renesas Project Template** and you are using a Renesas DK-S7G2 or PE-HMI1 board (i.e. not a custom board):
  - i. Download and install the X-Ware Template Pack from the Synergy Gallery (Demos & Applications section) into your e<sup>2</sup> studio v4.2.0.012 installation.
  - Using Windows Explorer, navigate to the following folder: <e2\_studio\_4.2.0.012\_base\_dir>/internal/projectgen/arm/Templates/synergy/<project\_template\_dir>, where <project\_template\_dir> is the directory of the project template you selected when you originally created you project in e<sup>2</sup> studio v4.0.1.015.



iii. Copy file R7FS7G27H2A01CBD.pincfg from <project\_template\_dir> and paste it into your project in the e<sup>2</sup> studio Project Explorer.



- iv. In order for the pin configuration file change to take effect, restart  $e^2$  studio (File  $\rightarrow$  Restart).
- v. If you made any modifications to the pin configuration file from the Project Template in your original project, make the same modifications again to the new pin configuration file using the Pin Configurator (on the Pins tab in the Synergy Project Editor).
- vi. Proceed to Step 7.
- c) If your Project was originally **NOT based on a Renesas Project Template** (i.e. you have a completely custom pin configuration file):
  - i. Using Windows Explorer, navigate to the following folder: <e2\_studio\_4.2.0.012\_base\_dir>/internal/projectgen/arm/pinconfig.
  - ii. Copy file R7FS7G27H2A01CBD.pincfg (which is an "empty" default pin configuration file) and paste it into your project in the e<sup>2</sup> studio Project Explorer.



- iii. In order for the pin configuration file change to take effect, restart  $e^2$  studio (File  $\rightarrow$  Restart)
- iv. Manually configure all the required pins using the Pin Configurator (on the Pins tab in the Synergy Project Editor). (You may want to compare e<sup>2</sup> studio v4.0.1.015 and e<sup>2</sup> studio v4.2.0.012.)
- v. Be aware that some pin names have changed in the Pin Configurator for the Mass Production devices.



vi. Be aware that some pins on the Mass Production devices are different from the Early Samples:

Pin	Early Samples	Mass Production devices
P600	CKE (SDRAM)	- (no longer used for SDRAM)
P601	WE (SDRAM)	DQM0 (External Bus)
P608	A0 (SDRAM)	A0/DQM1 (External Bus)
P609	DQM1 (SDRAM)	CKE (External Bus)
P610	DQM0 (SDRAM)	WE (External Bus)

#### 5.7 Step 7: Verify the Threads tab

- a) Click on the Threads tab in the Synergy Project Editor.
- b) Make sure that your project in  $e^2$  studio v4.0.1.015 and your project in  $e^2$  studio v4.2.0.012 have:
  - iii. Exactly the same components list
  - iv. Exactly the same properties for each module

Since the SSP version is the same, there should be no difference.

🔅 Synergy Configuration [WeatherPanel] 🔀	
Threads	Generate Project Content
Threads	HMI Thread Modules
<pre>MAL g_cgc CGC Driver on CGC g_clc ELC Driver on ELC g_joport IOPORT Driver on IOPORT MHUT Tread g_display DISPLAY Module on GLCD g_pwm_baddight PWM Driver on GPT11 g_12c T2C Driver on RTIC1</pre>	New
	HMI Thread Objects
	a hmi queue Queue New >
	Remove
Synergy Configurate Synergy Configurate Threads	ubove) and e <sup>2</sup> studio v4.2.0.012 (see below).
Threads	HMI Thread Modules
WHAL/Common         g_cc CGC Driver on CGC         g_loport IOPORT Driver on IOPORT         ● HMI Thread         g_display DISPLAY Module on GLCD         g_joyne baddight PWM Driver on GPT11         g_j2c I2C Driver on RIIC1	New



#### 5.8 Step 8: Updating the Panel Clock Ratio

If your application uses the SSP Module "DISPLAY Module on GLCD", the Panel Clock Division Ratio has to be changed, since there is a hardware specification change from the Early Samples to the Mass Production devices.

For instance, if the Panel Clock Division Ratio (in the TCON register) for the Early Sample is set to ½, you need to change it to 1/8, since the pixel clock source for the Mass Production devices is 4 times faster than the pixel clock source for the Early Samples.

- a) On the Threads tab, in the RTOS thread that uses "DISPLAY Module on GLCD", click on that module to bring it into scope.
- b) In the Properties View, change the TCON Panel clock division ratio to <sup>1</sup>/<sub>4</sub> of the current setting.

#### 5.9 Step 9: Check ICU settings

- a) Click on the ICU tab in the Synergy Project Editor.
- b) Make sure that your project in e<sup>2</sup> studio v4.0.1.015 and your project in e<sup>2</sup> studio v4.2.0.012 have exactly same IRQ settings.

#### 5.10 Step 10: Point your project to a valid Synergy License file

- a) In e<sup>2</sup> studio v4.2.0.012, right-click on your project in the Project Explorer view and select "Properties" from the menu.
- b) Expand the "C/C++ General" section and click on "Synergy License".
- c) Browse to a valid Synergy License file, e.g. to the Evaluation License here:  $<\!e2\_studio\_v4\_2\_0\_012\_base\_dir>\internal\projectgen\arm\Licenses\$
- d) Click "OK".

#### 5.11 Step 11: Build your project in e<sup>2</sup> studio v4.2.0.012

- a) Select "Project  $\rightarrow$  Clean" from the menu
- b) Check "Clean projects selected below", "Start a build immediately", and "Build only the selected projects".
- c) Click OK to clean your project and build it.
- d) Confirm there are no compilation errors.

#### 5.12 Step 12: Download and run your project

- a) Connect your target hardware to your PC via a Segger J-Link, J-Link-Lite, or J-Link On-Board.
- b) Select "Run  $\rightarrow$  Debug Connections" from the menu
- c) Select your project's debug configuration under "Renesas GDB Hardware Debugging".
- d) After the debug configuration has loaded, click "Debug".
- e) Run your project to confirm proper operation.

# 6. Migration Option 4: Migrate to SSP v1.0.0, e<sup>2</sup> studio v4.2.0.012, and Mass Production boards

Use this Migration Option if you have updated hardware populated with Mass Production devices (PE-HMI1 v2.0 / DK-S7G2 v3.0) and you would like to upgrade to the latest SSP and  $e^2$  studio ISDE versions.



The migration is accomplished by exporting the project you created from your current S7G2 Early Sample environment, importing it into e<sup>2</sup> studio v4.2.0.012, migrating it to SSP v1.0.0, and running it on a Mass Production board.

Current Renesas Synergy Environment	<b>→</b>	Renesas Synergy Environment after migration
SSP v0.91.0x	<b>→</b>	SSP v1.0.0
e² studio v4.0.1.015	<b>→</b>	e <sup>2</sup> studio v4.2.0.012 and later
PE-HMI1 Product Example v1.x	<b>→</b>	PE-HMI1 Product Example v2.0
DK-S7G2 Development Kit v1.x / 2.x	<b>→</b>	DK-S7G2 Development Kit v3.0

In order to implement this migration option, please follow the following steps.

#### 6.1 Step 1: Export your project from the S7G2 Early Sample Software Development Environment

- a) Open your project in  $e^2$  studio v4.0.1.015.
- b) Right-click in the Project Explorer area and select "Export".
- c) Select "General  $\rightarrow$  Archive File" as the export destination
- d) Click "Next"
- e) Click "Browse" and navigate to the location of your choice.
- f) Enter a file name and click "Save".
- g) Click "Finish".
- h) Close  $e^2$  studio v4.0.1.015.

#### 6.2 Step 2: Install the S7G2 Mass Production Software Development Environment

- a) Download and install e<sup>2</sup> studio v4.2.0.012 from the Renesas Synergy Gallery (<u>https://synergygallery.renesas.com</u>). Registration is required.
- b) Download and install SSP v1.0.0 from the Renesas Synergy Gallery into the e<sup>2</sup> studio v4.2.0.012 installation folder.

#### 6.3 Step 3: Import your project into the S7G2 Mass Production Software Development Environment

- a) Start  $e^2$  studio v4.2.0.012.
- b) Select a suitable workspace.
- c) Right-click in the Project Explorer area and select "Import".



d) Select "General → Existing Projects into Workspace" as the import source.

e <sup>2</sup> Import	
Select Create new projects from an archive file or directory.	Ľ
Select an import source: type filter text	
General Archive File CMSIS Pack Existing Projects into Workspace File System HEW Project Preferences Rename & Import Existing C/C++ Project into Workspace Rename & Import Existing C/C++ Project into Workspace C/C++ Rename & Import Existing C/C++ Project into Workspace C/C++ C/C++ C/C++ C/C ++ C/C ++ File System C/C ++ File System Rename & Import Existing C/C++ Project into Workspace File System File System File System Rename & Import Existing C/C++ Project into Workspace File System File System Fi	
?	Cancel

- e) Click "Next"
- f) Click "Select Archive File"
- g) Click "Browse" and navigate to the location of the project you exported earlier.
- h) Select the project to be imported and click "Open".

1 0		-			·
e <sup>2</sup> Import					_ 🗆 🗙
Import Projects					
Select a directory to search	ch for existing E	Eclipse projects.			
					~
○ Select root directory:				7	Browse
Select <u>archive</u> file:	C:\workspace	WeatherPanel.	ip	•	Browse
Projects:					
WeatherPanel (W	eatherPanel)				Select All
					Deselect All
					Refresh
					ngnean
Options					
Search for nested pro	ojects				
☑ ⊆opy projects into we	orkspace				
Hide projects that alr	eady exist in th	ne workspace			
Working sets					
Add project to work	ing sets				
Working sets:				<b>v</b>	Select
?		< <u>B</u> ack	$\underline{N}ext >$	Einish	Cancel

i) Click "Finish" and wait for e<sup>2</sup> studio to finish importing your project.

#### 6.4 Step 4: Open the project in the Synergy Project Editor

a) Expand the imported project in the Project Explorer view.

b) Double-click on the configuration.xml file to invoke the Renesas Synergy Project Editor.



c) You should see a window asking whether you would like to switch to the latest available SSP version (1.0.0), click "**Yes**". (If you would like to stay with the older SSP version, use Migration Option 3 in this document.)

e <sup>2</sup> e2 st	tudio
$\bigcirc$	Warning: Pack missing for project's current selected SSP version of 0.91.03.
	If you remain with this SSP version you will not be able to add further SSP components or re-extract SSP source files.
	Would you like to switch to latest available SSP version? (1.0.0)
Ren	nember my decision
	Yes No Cancel

d) In the Synergy Project Editor, click the Components tab. Make sure there are no 🕰 marks anywhere.

#### 6.5 Step 5: Update the Pin Configuration file

In this step you need to either update or recreate your existing .pincfg file (your Pin Configuration file) in your  $e^2$  studio project. This file is no longer valid for the Mass Production board, since the pinout of the MCU is different between the Early Samples and the Mass Production devices.

a) Rename the .pincfg file in your e<sup>2</sup> studio project to R7FS7G27H2A01CBD\_old.pincfg.



- b) If your project was originally **based on a Renesas Project Template** and you are using a Renesas DK-S7G2 or PE-HMI1 board (i.e. not a custom board):
  - vii. Download and install the X-Ware Template Pack from the Synergy Gallery (Demos & Applications section) into your e<sup>2</sup> studio v4.2.0.012 installation.
  - viii. Using Windows Explorer, navigate to the following folder: <e2\_studio\_4.2.0.012\_base\_dir>/internal/projectgen/arm/Templates/synergy/<project\_template\_dir>,



where <project\_template\_dir> is the directory of the project template you selected when you originally created you project in e<sup>2</sup> studio v4.0.1.015.

ix. Copy the file R7FS7G27H2A01CBD.pincfg from <project\_template\_dir> and paste it into your project in the e<sup>2</sup> studio Project Explorer.

🎦 Project Explorer 🛛	⊡ 🔄 ▽
🗆 💕 WeatherPanel	[Debug]
🗄 🐝 Binaries	
🗄 👘 Includes	
🗄 🟸 src	
🗄 🗁 ssp	
🗄 🗁 Debug	
🗄 🗁 guix_studio	
🗄 🗁 script	
🗄 🗁 ssp_cfg	
💮 configuration	.xml
🔤 📄 hmi_app_solu	ition_chapter10 Debug.jlink
hmi_app_solu	ition_chapter 10 Debug.launch
R7FS7G27G2	A01CBD.pincfg
📄 R7FS7G27H2	A01CBD_old.pincfg

- x. In order for the pin configuration file change to take effect, restart  $e^2$  studio (File  $\rightarrow$  Restart).
- xi. If you made any modifications to the pin configuration file from the Project Template in your original project, make the same modifications again to the new pin configuration file using the Pin Configurator (on the Pins tab in the Synergy Project Editor).
- xii. Proceed to Step 6.
- c) If your Project was originally **NOT based on a Renesas Project Template** (i.e. you have a completely custom pin configuration file):
  - vii. Using Windows Explorer, navigate to the following folder:
     <e2\_studio\_4.2.0.012\_base\_dir>/internal/projectgen/arm/pinconfig.
  - viii. Copy the file R7FS7G27H2A01CBD.pincfg (which is an "empty" default pin configuration file) and paste it into your project in the e<sup>2</sup> studio Project Explorer.



- ix. In order for the pin configuration file change to take effect, restart  $e^2$  studio (File  $\rightarrow$  Restart)
- x. Manually configure all the required pins using the Pin Configurator (on the Pins tab in the Synergy Project Editor). (You may want to compare e<sup>2</sup> studio v4.0.1.015 and e<sup>2</sup> studio v4.2.0.012.)
- xi. Be aware that some pin names have changed in the Pin Configurator for the Mass Production devices.



xii. Be aware that some pins on the Mass Production devices are different from the Early Samples:

Pin	Early Samples	Mass Production devices
P600	CKE (SDRAM)	- (no longer used for SDRAM)
P601	WE (SDRAM)	DQM0 (External Bus)
P608	A0 (SDRAM)	A0/DQM1 (External Bus)
P609	DQM1 (SDRAM)	CKE (External Bus)
P610	DQM0 (SDRAM)	WE (External Bus)

#### 6.6 Step 6: Verify / Update the Threads tab

- a) Click on the Threads tab in the Synergy Project Editor.
- b) Open your original project in  $e^2$  studio v4.0.1.015.
- c) Compare the modules in the Thread Modules panes between your original project in e<sup>2</sup> studio v4.0.1.015 / SSP v0.91.0x and your imported project in e<sup>2</sup> studio v4.2.0.012 / SSP v1.0.0. You will notice that the Module names in SSP v1.0.0 have changed somewhat compared to v0.91.0x, but you will still be able to identify which v0.91.0x module corresponds to which v1.0.0 module.

	HMI Thread Modules
HMI Thread Modules	🕀 g display Display Driver on r glcd
<ul> <li>         ⊕ g_display DISPLAY Module on GLCD         ⊕ g_owm_backlight PWM Driver on GPT11         ⊕ g_l2c I2C Driver on RIIC1         ⊕ g_l2c I2C Driver on RIIC1         ⊕ g_sternal_irq EXTERNAL_IRQ Module on ICU12         ⊕ g_sf_external_irq SF_EXTERNAL_IRQ Module on SF_EXTERNAL_IRQ         ⊕ g_sf_external_irq SF_EXTERNAL_RQ Module on SF_EXTERNAL_IRQ         ⊕ g_sf_external_irq ST_EXTERNAL_RQ Module on SF_TOUCH_PANEL_I         ⊕ g_sf_el gx GUIX Adaptation Framework         </li> </ul>	<ul> <li>         ⊕ g_display Display Driver on r_glcd         ⊕ g_l2 I2C Driver on r_ricc         ⊕ g_l2 I2C Driver on r_ricc         ⊕ g_setternal_irq External IRQ Driver on r_icu         ⊕ g_sf_external_irq External IRQ Framework on sf_external_irq         ⊕ g_sf_message Messaging Framework on sf_message         ⊕ g_sf_touch_panel_i2C Touch Panel Framework on sf_touch_panel_i2C         ⊕ g_sf_el_ax GUIX Port on sf_el_ax         ⊕ D/AVE 2D Port on sf_el_ax         ⊕ D/AVE 2D Port on sf_els_2d_drw         ⊕ g_sf_pieg_decode         </li> </ul>
<ul> <li>➡ SF_TES_2D_DRW Module on Dave/2d</li> <li>➡ g_sf_jpeg_decode SF_JPEG_Decode Module on JPEG Decode</li> <li>➡ g_jpeg_decode JPEG Decode Driver on JPEG</li> <li>➡ GUIX</li> </ul>	<ul> <li> <b>g</b>_jpeg_decode JPEG Decode Driver on r_jpeg          </li> <li>             GUIX on gx         </li> <li> <b>g</b>_pwm_backlight Timer Driver on r_gpt         </li> <li> <b>D</b>/AVE 2D Driver on dave2d         </li> </ul>

SSP v0.91.0x Modules

#### SSP v1.0.0 Modules

- d) Compare all the SSP Module property settings in the Properties View between your original project in e<sup>2</sup> studio v4.0.1.015 / SSP v0.91.0x and your imported project in e<sup>2</sup> studio v4.2.0.012 / SSP v1.0.0.
   (When you updated your SSP version to v1.0.0, the module settings were reset to their default values. Therefore you need to edit any modified module properties manually. Be sure not to miss any properties).
- e) You may see some missing modules that were present in your SSP v0.91.0x project but are not present in your SSP v1.0.0 project. For instance, you may notice that the PWM Driver on GPTxx, which was present in your SSP v0.91.0x project, is missing for SSP v1.0.0 (see picture in Step 6c). This is because SSP v1.0.0 no longer supports a stand-alone PWM Driver on GPT module. Instead, PWM is supported by the Timer Driver on r\_gpt (see picture below).

You may also see additional modules. For instance, the D/AVE 2D Driver on dave 2d was not present in your SSP v0.91.0x project but is present now in your SSP v1.0.0 project (see picture in Step 6c). This is because SSP v1.0.0 now allows to select the SSP component in the Modules selection pane on the Synergy Project Editor Threads tab. In SSP v0.91.0x, you could only select the D/AVE 2D Driver from the Components tab..

It is possible to swap a module between SSP versions or use an alternative module or new module from the new SSP pack. Please refer to the SSP Pack Release Notes for the differences between such modules, or contact Renesas for more information.



HMI Thread Modules		в	P109	P108	P301	vcc	vcc	P312	P912	P200	VLO	VSS
g_display Display Driver on r_glcd	New Drive	er		Ana	l√ log		<b>(</b> 109	¥310	P311	P201	P904	vss
g_ize ize briver on r_nic     g_external_irq External IRQ Driver on r_icu	Remov Fran	nework	•	Con	nectiv	vity I	06	P307	<b>P308</b>	P910	P903	vcc
g_sf_external_irq External IRQ Framework on sf_external_irq		E	¥61	Inp	ut	,	14	¥915	<b>7908</b>	<b>6064</b>	¥900	P313
<ul> <li>g_st_message messaging ranework on st_message</li> <li>g_st_touch_panel_i2c Touch Panel Framework on st_touch_panel_i2c</li> </ul>		F	<b>P</b> 61	Mor	nitorin	g l	00	¥906	<b>P907</b>	RES	P314	P710
g_sf_el_gx GUIX Port on sf_el_gx     D/AVE 2D Port on sf_tes_2d_drw		G	P81	Sto	rage	j	112	PA11	PAOS	P615	¥206	P713
g_sf_jpeg_decode JPEG Decode Framework on sf_jpeg_decode		н	VCL	Tim	ers osfer	)		RTC E	)river Drive	on r_	rtc agt	4
g_jpeg_decode JPEG Decode Driver on r_jpeg     GUIX on gx		3	PA07	PA06	PA05	PA04		Timer	Drive	r on r	_gpt	
- sourcer gr			×	<b>~</b>	×	<b>~</b>	~	×				~

f) If you added new SSP v1.0.0 modules to your project as alternatives for SSP v0.91.0x modules that are no longer supported in v1.0.0, configure the module properties in the Properties View.

		Properties 🖾 👫 Problems	
		Property	Value
Properties 🔀 🚰 Problems		Common	
Property	Value	Parameter Checking	Enabled
Common		⊡ ICU	
Param Checking Enable	Enabled	GPT11 COUNTER OVERFLOW	Disabled
Module		Module	
Name	g_pwm_backlight	Name	g_pwm_backlight
Period	10	Channel	11
Period Unit	Unit Period Msec	Mode	PWM
Duty Cyde	50	Period Value	10
Duty Cycle Unit	Unit Percent	Period Unit	Milliseconds
Channel	11	Duty Cycle Value	50
Autostart	True	Duty Cyde Unit	Unit Percent
Gtioca Output Enabled	True	Auto Start	True
Gtioca Stop Level	Pin Level Low	GTIOCA Output Enabled	True
Gtiocb Output Enabled	False	GTIOCA Stop Level	Pin Level Low
Gtiocb Stop Level	Pin Level Low	GTIOCB Output Enabled	False
Callback	NULL	GTIOCB Stop Level	Pin Level Low
		Callback	NULL

V0.91.03 (PWM Driver on GPTnn)

v1.0.0 (Timer Driver on r gpt)

### 6.7 Step 7: Enable FPU support

SSP v1.0.0 now supports FPU. This is one of the major differences between SSP v0.91.0x and v1.0.0.

- a) Go to Project  $\rightarrow$  Properties
- b) Go to C/C++ Build  $\rightarrow$  Settings
- c) On the Tool Settings tab, click on Target Processor



d) Change the Float ABI setting to 'FP instructions (hard)' since SSP v1.0.0 does support FPU (VFPv4).

e <sup>2</sup> Properties for WeatherPanel				×
type filter text	Settings		← → →	•
<ul> <li>B: Resource</li> <li>Builders</li> <li>C/C++ Build</li> <li>Build Variables</li> <li>Environment</li> <li>Logging</li> <li>Settingsi</li> <li>Tool Chain Editor</li> <li>C/C++ General</li> <li>B: Code Analysis</li> <li>Documentation</li> <li>File Types</li> <li>Formatter</li> <li>Indexer</li> <li>Language Mappings</li> <li>Paths and Symbols</li> <li>Preprocessor Include Path</li> <li>Synergy Builder</li> <li>Synergy License</li> <li>Project References</li> <li>Refactoring History</li> <li>Run/Debug Settings</li> </ul>	Configuration: Debug [Active]	tifact 🛛 😵 Toolchain ARM family Architecture Instruction set Instruction set Inthumb interwo Endianness Float ABI FPU Type Unaligned access AArch64 family Feature cric Feature crypto Feature fp Feature fp Feature fp Feature simd Code model I Strict align (am	Manage Configurations Manage Configurations Toolchain default Thumb (mthumb) rk (mthumb-interwork) Toolchain default FP instructions (hard) FP instructions (hard) FD instruct	
				-1
	<u>•</u>		•	1
?			OK Cancel	

#### 6.8 Step 8: Updating the Panel Clock Ratio

If your application uses the SSP Module "DISPLAY Module on GLCD", the Panel Clock Division Ratio has to be changed, since there is a hardware specification change from the Early Samples to the Mass Production devices.

For instance, if the Panel Clock Division Ratio (in the TCON register) for the Early Sample is set to ½, you need to change it to 1/8, since the pixel clock source for the Mass Production devices is 4 times faster than the pixel clock source for the Early Samples.

- a) On the Threads tab, in the RTOS thread that uses "DISPLAY Module on GLCD", click on that module to bring it into scope.
- b) In the Properties View, change the TCON Panel clock division ratio to <sup>1</sup>/<sub>4</sub> of the current setting.

Value
LCD_TCON1
LCD_TCON2
1/2
Off
512
512

#### 6.9 Step 9: Check ICU settings

- a) Click on the ICU tab in the Synergy Project Editor.
- b) Make sure that your project in e<sup>2</sup> studio v4.0.1.015 and your project in e<sup>2</sup> studio v4.2.0.012 have exactly same IRQ settings. This task is a bit tedious because the structure and the naming of the ICU settings has changed. See the Appendix for a list of old names vs. new names.

#### 6.10 Step 10: Point your project to a valid Synergy License file

- a) In e<sup>2</sup> studio v4.2.0.012, right-click on your project in the Project Explorer view and select "Properties" from the menu.
- b) Expand the "C/C++ General" section and click on "Synergy License"
- c) Browse to a valid Synergy License file, e.g. to the Evaluation License here:  $<\!e2\_studio\_v4\_2\_0\_012\_base\_dir>\!internal\projectgen\arm\Licenses\$
- d) Click "OK".

### 6.11 Step 11: Build your project in e<sup>2</sup> studio v4.2.0.012

- a) Select "Project  $\rightarrow$  Clean" from the menu
- b) Check "Clean projects selected below", "Start a build immediately", and "Build only the selected projects".
- c) Click OK to clean your project and build it.
- d) Confirm there are no compilation errors.

#### 6.12 Step 12: Download and run your project

- a) Connect your target hardware to your PC via a Segger J-Link, J-Link-Lite, or J-Link On-Board.
- b) Select "Run  $\rightarrow$  Debug Connections" from the menu
- c) Select your project's debug configuration under "Renesas GDB Hardware Debugging".
- d) After the debug configuration has loaded, click "Debug".
- e) Run your project to confirm proper operation.



### 7. Appendix

### 7.1 ELC Event list (on the ICU tab)

Old Name	New Name
ELC_PERIPHERAL_GPT_A	ELC_PERIPHERAL_GPT_A
ELC_PERIPHERAL_GPT_B	ELC_PERIPHERAL_GPT_B
ELC_PERIPHERAL_GPT_C	ELC_PERIPHERAL_GPT_C
ELC_PERIPHERAL_GPT_D	ELC_PERIPHERAL_GPT_D
ELC_PERIPHERAL_GPT_E	ELC_PERIPHERAL_GPT_E
ELC_PERIPHERAL_GPT_F	ELC_PERIPHERAL_GPT_F
ELC_PERIPHERAL_GPT_G	ELC_PERIPHERAL_GPT_G
ELC_PERIPHERAL_GPT_H	ELC_PERIPHERAL_GPT_H
ELC_PERIPHERAL_S12ADA0	ELC_PERIPHERAL_ADC0
ELC_PERIPHERAL_S12ADB0	ELC_PERIPHERAL_ADC0_B
ELC_PERIPHERAL_S12ADA1	ELC_PERIPHERAL_ADC1
ELC_PERIPHERAL_S12ADB1	ELC_PERIPHERAL_ADC1_B
ELC_PERIPHERAL_DA0	ELC_PERIPHERAL_DAC0
ELC_PERIPHERAL_DA1	ELC_PERIPHERAL_DAC1
ELC_PERIPHERAL_PORT_GROUP_A	ELC_PERIPHERAL_IOPORT1
ELC_PERIPHERAL_PORT_GROUP_B	ELC_PERIPHERAL_IOPORT2
ELC_PERIPHERAL_PORT_GROUP_C	ELC_PERIPHERAL_IOPORT3
ELC_PERIPHERAL_PORT_GROUP_D	ELC_PERIPHERAL_IOPORT4
ELC_PERIPHERAL_CTSU	ELC_PERIPHERAL_CTSU
PORTO_IRQ	ICU_IRQ0
PORT1_IRQ	ICU_IRQ1
PORT2_IRQ	ICU_IRQ2
PORT3_IRQ	ICU_IRQ3
PORT4_IRQ	ICU_IRQ4
PORT5_IRQ	ICU_IRQ5
PORT6_IRQ	ICU_IRQ6
PORT7_IRQ	ICU_IRQ7
PORT8_IRQ	ICU_IRQ8
PORT9_IRQ	ICU_IRQ9
PORT10_IRQ	ICU_IRQ10
PORT11_IRQ	ICU_IRQ11
PORT12_IRQ	ICU_IRQ12
PORT13_IRQ	ICU_IRQ13
PORT14_IRQ	ICU_IRQ14
PORT15_IRQ	ICU_IRQ15
DMAC0_DMAC	DMAC0_INT
DMAC1_DMAC	DMAC1_INT
DMAC2_DMAC	DMAC2_INT
DMAC3_DMAC	DMAC3_INT
DMAC4_DMAC	DMAC4_INT
DMAC5_DMAC	DMAC5_INT



DMAC6_DMAC	DMAC6_INT	
DMAC7_DMAC	DMAC7_INT	
DTC_TRANSFER	REMOVE	
DTC_COMPLETE	DTC_COMPLETE	
DTC_DTC_END	DTC_END	
EXDMAC0_EXDMAC	REMOVE	
EXDMAC1_EXDMAC	REMOVE	
ICU_CANCELING_SNOOZE_MODE	ICU_SNOOZE_CANCEL	
FCU_FIFERR	FCU_FIFERR	
FCU_FRDYI	FCU_FRDYI	
FCU_ECCERR	REMOVE	
LVD1_LVD1	LVD LVD1	
LVD2_LVD2	LVD_LVD2	
VBATT_VBAT	VBATT_LVD	
MOSC_OSC_STOP	CGC_MOSC_STOP	
CPUSYS_SNOOZE_MODE_ENTRY_FLAG	LPM_SNOOZE_REQUEST	
	AGT0_INT	
AGT0_AGTCMAI	AGT0_COMPARE_A	
AGT0_AGTCMBI	AGT0_COMPARE_B	
AGT1_AGTI	AGT1_INT	
AGT1_AGTCMAI	AGT1_COMPARE_A	
AGT1_AGTCMBI	AGT1_COMPARE_B	
IWDT_NMIUNDF_N	IWDT UNDERFLOW	
CWDT_NMIUNDF_N	WDT_UNDERFLOW	
RTC_ALM	 RTC_ALARM	
RTC_PRD	RTC_PERIOD	
RTC_CUP	RTC_CARRY	
S12AD0_ADI	ADC0_SCAN_END	
S12AD0_GBADI	ADC0_SCAN_END_B	
S12AD0_CMPAI	ADC0_WINDOW_A	
S12AD0_CMPBI	ADC0_WINDOW_B	
S12AD0_COMPARE_MATCH	ADC0_COMPARE_MATCH	
S12AD0_COMPARE_MISMATCH	ADC0_COMPARE_MISMATCH	
S12AD1_ADI	ADC1_SCAN_END	
S12AD1_GBADI	ADC1_SCAN_END_B	
S12AD1_CMPAI	ADC1_WINDOW_A	
S12AD1_CMPBI	ADC1_WINDOW_B	
S12AD1_COMPARE_MATCH	ADC1_COMPARE_MATCH	
S12AD1_COMPARE_MISMATCH	ADC1_COMPARE_MISMATCH	
COMP_OC0_COMP_IRQ	COMP_HS_0	
COMP_RD1_COMP_IRQ	COMP_HS_1	
COMP_RD2_COMP_IRQ	COMP_HS_2	
COMP_RD3_COMP_IRQ	COMP_HS_3	
COMP_RD4_COMP_IRQ	 COMP_HS_4	
COMP_RD5_COMP_IRQ	COMP_HS_5	



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Migrating S7G2 MCUs Early Application Projects

COMP_LP_COMP_COIRQ	COMP_LP_0	
COMP_LP_COMP_C1IRQ	COMP_LP_1	
USBFS_D0FIFO	USBFS_FIFO_0	
USBFS_D1FIFO	USBFS_FIFO_1	
USBFS_USBI	USBFS_INT	
USBFS_USBR	USBFS_RESUME	
RIICO_RXI	IIC0_RXI	
RIICO_TXI	IIC0_TXI	
RIICO_TEI	IIC0_TEI	
RIICO_EEI	IICO_ERI	
RIICO_WUI	IIC0_WUI	
RIIC1_RXI	IIC1_RXI	
RIIC1_TXI		
RIIC1_TEI	IIC1_TEI	
RIIC1_EEI	IIC1_ERI	
RIIC2_RXI	IIC2_RXI	
RIIC2_TXI	IIC2_TXI	
RIIC2_TEI	IIC2_TEI	
RIIC2_EEI	IIC2_ERI	
SSI0_SSITXI	SSI0_TXI	
SSI0_SSIRXI	SSIO_RXI	
SSI0_SSIRT	REMOVE	
SSI0_SSIF	SSIO_INT	
SSI0_SSIF SSI1_SSITXI	REMOVE	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRXI	REMOVE REMOVE	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT	SSI0_INI       REMOVE       SSI1_TXI_RXI	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF	SSI0_INI       REMOVE       SSI1_TXI_RXI       SSI1_INT	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI	SSI0_INI         REMOVE         REMOVE         SSI1_TXI_RXI         SSI1_INT         SRC_INPUT_FIFO_EMPTY	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI	SSI0_INI         REMOVE         SSI1_TXI_RXI         SSI1_INT         SRC_INPUT_FIFO_EMPTY         SRC_OUTPUT_FIFO_FULL	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOW	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOW	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_OVF SRC_UDF SRC_CEF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_END	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_OVF SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READY	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_END	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SRC_IDEI SRC_ODFI SRC_OVF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INT	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCERI CTSU_CTSUWR	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITE	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_OVF SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_READ	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN	SSI0_IN1REMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_ENDCTSU_END	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN KEY_INTKR	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_EADKEY_INT	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN KEY_INTKR DOC_DOPCF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_EADCTSU_ENDKEY_INTDOC_INT	
SSIO_SSIF SSI1_SSITXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN KEY_INTKR DOC_DOPCF CAC_FERRF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_ENDKEY_INTDOC_INTCAC_FREQUENCY_ERROR	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN KEY_INTKR DOC_DOPCF CAC_FERRF CAC_MENDF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_ENDKEY_INTDOC_INTCAC_FREQUENCY_ERRORCAC_MEASUREMENT_END	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN KEY_INTKR DOC_DOPCF CAC_FERRF CAC_MENDF CAC_OVFF	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_ENDKEY_INTDOC_INTCAC_FREQUENCY_ERRORCAC_OVERFLOW	
SSI0_SSIF SSI1_SSITXI SSI1_SSIRT SSI1_SSIF SRC_IDEI SRC_ODFI SRC_OVF SRC_UDF SRC_CEF PDC_PCDFI PDC_PCFEI PDC_PCERI CTSU_CTSUWR CTSU_CTSURD CTSU_CTSUFN KEY_INTKR DOC_DOPCF CAC_FERRF CAC_MENDF CAC_OVFF RCAN20_ERS	SSI0_INIREMOVEREMOVESSI1_TXI_RXISSI1_INTSRC_INPUT_FIFO_EMPTYSRC_OUTPUT_FIFO_FULLSRC_OUTPUT_FIFO_OVERFLOWSRC_OUTPUT_FIFO_UNDERFLOWSRC_CONVERSION_ENDPDC_RECEIVE_DATA_READYPDC_FRAME_ENDPDC_INTCTSU_WRITECTSU_ENDKEY_INTDOC_INTCAC_FREQUENCY_ERRORCAC_OVERFLOWCANO_ERROR	



RCAN20_TXF	CAN0_FIFO_TX	
RCAN20_RXM	CAN0_MAILBOX_RX	
RCAN20_TXM	CAN0_MAILBOX_TX	
RCAN21_ERS	CAN1_ERROR	
RCAN21_RXF	CAN1_FIFO_RX	
RCAN21_TXF	CAN1_FIFO_TX	
RCAN21_RXM	CAN1_MAILBOX_RX	
RCAN21_TXM	CAN1_MAILBOX_TX	
GPIO_PORT_GROUP_A	IOPORT_EVENT_1	
GPIO_PORT_GROUP_B	IOPORT_EVENT_2	
GPIO_PORT_GROUP_C	IOPORT_EVENT_3	
GPIO_PORT_GROUP_D	IOPORT_EVENT_4	
ELC0_SOFTWARE_EVENT	ELC_SOFTWARE_EVENT_0	
ELC1_SOFTWARE_EVENT	ELC_SOFTWARE_EVENT_1	
POEG_GROUP_EVENT0	POEG0_EVENT	
POEG_GROUP_EVENT1	POEG1_EVENT	
POEG_GROUP_EVENT2	POEG2_EVENT	
POEG_GROUP_EVENT3	POEG3_EVENT	
GPT0_CAPTURE_COMPARE_INT_A	GPT0_CAPTURE_COMPARE_A	
GPT0 CAPTURE COMPARE INT B	GPT0 CAPTURE COMPARE B	
GPT0 COMPARE INT C	GPT0 COMPARE C	
 GPT0_COMPARE_INT_D	 GPT0_COMPARE_D	
GPT0_COMPARE_INT_E	GPT0 COMPARE E	
	GPT0 COMPARE F	
GPT0_COUNTER_OVERFLOW	 GPT0_COUNTER_OVERFLOW	
GPT0_COUNTER_UNDERFLOW		
GPT0_AD_TRIG_A	 GPT0_AD_TRIG_A	
GPT0_AD_TRIG_B	GPTO AD TRIG B	
GPT1_CAPTURE_COMPARE_INT_A	GPT1 CAPTURE COMPARE A	
GPT1_CAPTURE_COMPARE_INT_B	GPT1_CAPTURE_COMPARE_B	
GPT1_COMPARE_INT_C	GPT1_COMPARE_C	
GPT1_COMPARE_INT_D	GPT1_COMPARE_D	
GPT1_COMPARE_INT_E	GPT1_COMPARE_E	
GPT1_COMPARE_INT_F	GPT1_COMPARE_F	
GPT1_COUNTER_OVERFLOW	GPT1_COUNTER_OVERFLOW	
GPT1_COUNTER_UNDERFLOW	GPT1_COUNTER_UNDERFLOW	
GPT1_AD_TRIG_A	GPT1_AD_TRIG_A	
GPT1_AD_TRIG_B	GPT1_AD_TRIG_B	
GPT2_CAPTURE_COMPARE_INT_A	GPT2_CAPTURE_COMPARE_A	
GPT2_CAPTURE_COMPARE_INT_B	GPT2_CAPTURE_COMPARE_B	
GPT2_COMPARE_INT_C	GPT2_COMPARE_C	
GPT2_COMPARE_INT_D	GPT2 COMPARE D	
GPT2_COMPARE_INT_E	GPT2 COMPARE E	
GPT2_COMPARE_INT_F	GPT2_COMPARE_F	
GPT2_COUNTER_OVERFLOW	GPT2_COUNTER_OVERFLOW	



GPT2_COUNTER_UNDERFLOW	GPT2_COUNTER_UNDERFLOW		
GPT2_AD_TRIG_A	GPT2 AD TRIG A		
GPT2_AD_TRIG_B	GPT2 AD TRIG B		
GPT3_CAPTURE_COMPARE_INT_A	GPT3 CAPTURE COMPARE A		
GPT3_CAPTURE_COMPARE_INT_B	GPT3 CAPTURE COMPARE B		
GPT3_COMPARE_INT_C	GPT3_COMPARE_C		
GPT3 COMPARE INT D	GPT3 COMPARE D		
 GPT3_COMPARE_INT_E	 GPT3_COMPARE_E		
GPT3 COMPARE INT F	GPT3_COMPARE_F		
GPT3 COUNTER OVERFLOW	GPT3_COUNTER_OVERFLOW		
GPT3 COUNTER UNDERFLOW	GPT3_COUNTER_UNDERFLOW		
 GPT3_AD_TRIG_A	GPT3 AD TRIG A		
GPT3_AD_TRIG_B	GPT3_AD_TRIG_B		
GPT4_CAPTURE_COMPARE_INT_A	GPT4_CAPTURE_COMPARE_A		
GPT4_CAPTURE_COMPARE_INT_B	GPT4_CAPTURE_COMPARE_B		
GPT4_COMPARE_INT_C	GPT4_COMPARE_C		
GPT4_COMPARE_INT_D	GPT4_COMPARE_D		
GPT4_COMPARE_INT_E	GPT4_COMPARE_E		
GPT4_COMPARE_INT_F	GPT4_COMPARE_F		
GPT4_COUNTER_OVERFLOW	GPT4_COUNTER_OVERFLOW		
GPT4_COUNTER_UNDERFLOW	GPT4_COUNTER_UNDERFLOW		
GPT4_AD_TRIG_A	GPT4_AD_TRIG_A		
GPT4_AD_TRIG_B	GPT4_AD_TRIG_B		
GPT5_CAPTURE_COMPARE_INT_A	GPT5_CAPTURE_COMPARE_A		
GPT5_CAPTURE_COMPARE_INT_B	GPT5_CAPTURE_COMPARE_B		
GPT5_COMPARE_INT_C	GPT5_COMPARE_C		
GPT5_COMPARE_INT_D	GPT5_COMPARE_D		
GPT5_COMPARE_INT_E	GPT5_COMPARE_E		
GPT5_COMPARE_INT_F	GPT5_COMPARE_F		
GPT5_COUNTER_OVERFLOW	GPT5_COUNTER_OVERFLOW		
GPT5_COUNTER_UNDERFLOW	GPT5_COUNTER_UNDERFLOW		
GPT5_AD_TRIG_A	GPT5_AD_TRIG_A		
GPT5_AD_TRIG_B	GPT5_AD_TRIG_B		
GPT6_CAPTURE_COMPARE_INT_A	GPT6_CAPTURE_COMPARE_A		
GPT6_CAPTURE_COMPARE_INT_B	GPT6_CAPTURE_COMPARE_B		
GPT6_COMPARE_INT_C	GPT6_COMPARE_C		
GPT6_COMPARE_INT_D	GPT6_COMPARE_D		
GPT6_COMPARE_INT_E	GPT6_COMPARE_E		
GPT6_COMPARE_INT_F	GPT6_COMPARE_F		
GPT6_COUNTER_OVERFLOW	GPT6_COUNTER_OVERFLOW		
GPT6_COUNTER_UNDERFLOW	GPT6_COUNTER_UNDERFLOW		
GPT6_AD_TRIG_A	GPT6_AD_TRIG_A		
GPT6_AD_TRIG_B	GPT6_AD_TRIG_B		
GPT7_CAPTURE_COMPARE_INT_A	GPT7_CAPTURE_COMPARE_A		
GPT7_CAPTURE_COMPARE_INT_B	GPT7_CAPTURE_COMPARE_B		



GPT7_COMPARE_INT_C	GPT7_COMPARE_C		
GPT7_COMPARE_INT_D	GPT7_COMPARE_D		
GPT7_COMPARE_INT_E	 GPT7_COMPARE_E		
GPT7_COMPARE_INT_F			
GPT7_COUNTER_OVERFLOW	GPT7_COUNTER_OVERFLOW		
GPT7_COUNTER_UNDERFLOW	GPT7_COUNTER_UNDERFLOW		
GPT7_AD_TRIG_A	GPT7_AD_TRIG_A		
GPT7_AD_TRIG_B	GPT7_AD_TRIG_B		
GPT8_CAPTURE_COMPARE_INT_A	GPT8_CAPTURE_COMPARE_A		
GPT8_CAPTURE_COMPARE_INT_B	GPT8_CAPTURE_COMPARE_B		
GPT8_COMPARE_INT_C	GPT8_COMPARE_C		
GPT8_COMPARE_INT_D	GPT8_COMPARE_D		
GPT8_COMPARE_INT_E	GPT8 COMPARE E		
GPT8_COMPARE_INT_F	GPT8_COMPARE_F		
GPT8_COUNTER_OVERFLOW	GPT8_COUNTER_OVERFLOW		
GPT8_COUNTER_UNDERFLOW	GPT8_COUNTER_UNDERFLOW		
GPT8_AD_TRIG_A	GPT8_AD_TRIG_A		
GPT8_AD_TRIG_B	GPT8_AD_TRIG_B		
GPT9_CAPTURE_COMPARE_INT_A	GPT9_CAPTURE_COMPARE_A		
GPT9_CAPTURE_COMPARE_INT_B	GPT9_CAPTURE_COMPARE_B		
GPT9_COMPARE_INT_C	GPT9_COMPARE_C		
GPT9_COMPARE_INT_D	GPT9_COMPARE_D		
GPT9_COMPARE_INT_E	GPT9_COMPARE_E		
GPT9_COMPARE_INT_F	GPT9_COMPARE_F		
GPT9_COUNTER_OVERFLOW	GPT9_COUNTER_OVERFLOW		
GPT9_COUNTER_UNDERFLOW	GPT9_COUNTER_UNDERFLOW		
GPT9_AD_TRIG_A	GPT9_AD_TRIG_A		
GPT9_AD_TRIG_B	GPT9_AD_TRIG_B		
GPT10_CAPTURE_COMPARE_INT_A	GPT10_CAPTURE_COMPARE_A		
GPT10_CAPTURE_COMPARE_INT_B	GPT10_CAPTURE_COMPARE_B		
GPT10_COMPARE_INT_C	GPT10_COMPARE_C		
GPT10_COMPARE_INT_D	GPT10_COMPARE_D		
GPT10_COMPARE_INT_E	GPT10_COMPARE_E		
GPT10_COMPARE_INT_F	GPT10_COMPARE_F		
GPT10_COUNTER_OVERFLOW	GPT10_COUNTER_OVERFLOW		
GPT10_COUNTER_UNDERFLOW	GPT10_COUNTER_UNDERFLOW		
GPT10_AD_TRIG_A	GPT10_AD_TRIG_A		
GPT10_AD_TRIG_B	GPT10_AD_TRIG_B		
GPT11_CAPTURE_COMPARE_INT_A	GPT11_CAPTURE_COMPARE_A		
GPT11_CAPTURE_COMPARE_INT_B	GPT11_CAPTURE_COMPARE_B		
GPT11_COMPARE_INT_C	GPT11_COMPARE_C		
GPT11_COMPARE_INT_D	GPT11_COMPARE_D		
GPT11_COMPARE_INT_E	GPT11_COMPARE_E		
GPT11_COMPARE_INT_F	GPT11_COMPARE_F		
GPT11 COUNTER OVERFLOW	GPT11 COUNTER OVERFLOW		



GPT11 COUNTER UNDERFLOW	GPT11 COUNTER UNDERFLOW		
GPT11 AD TRIG A	GPT11 AD TRIG A		
GPT11 AD TRIG B	GPT11 AD TRIG B		
GPT12 CAPTURE COMPARE INT A	GPT12 CAPTURE COMPARE A		
GPT12 CAPTURE COMPARE INT B	GPT12 CAPTURE COMPARE B		
GPT12 COMPARE INT C	GPT12 COMPARE C		
GPT12 COMPARE INT D	GPT12_COMPARE_D		
GPT12 COMPARE INT E	GPT12_COMPARE_E		
GPT12 COMPARE INT F	GPT12_COMPARE_F		
GPT12 COUNTER OVERFLOW	 GPT12_COUNTER_OVERFLOW		
GPT12 COUNTER UNDERFLOW	GPT12_COUNTER_UNDERFLOW		
GPT12 AD TRIG A	GPT12 AD TRIG A		
GPT12 AD TRIG B	GPT12 AD TRIG B		
GPT13 CAPTURE COMPARE INT A	GPT13 CAPTURE COMPARE A		
	 GPT13_COMPARE_C		
GPT13 COMPARE INT D	GPT13 COMPARE D		
 GPT13_COMPARE_INT_F	 GPT13_COMPARE_F		
GPT13_COUNTER_OVERFLOW	GPT13_COUNTER_OVERFLOW		
GPT13_COUNTER_UNDERFLOW	GPT13_COUNTER_UNDERFLOW		
GPT13_AD_TRIG_A	GPT13_AD_TRIG_A		
GPT13_AD_TRIG_B	GPT13_AD_TRIG_B		
GPT14_CAPTURE_COMPARE_INT_A	GPT14_CAPTURE_COMPARE_A		
GPT14_CAPTURE_COMPARE_INT_B	GPT14_CAPTURE_COMPARE_B		
GPT14_COMPARE_INT_C	GPT14_COMPARE_C		
GPT14_COMPARE_INT_D	GPT14_COMPARE_D		
GPT14_COMPARE_INT_E	GPT14_COMPARE_E		
GPT14_COMPARE_INT_F	GPT14_COMPARE_F		
GPT14_COUNTER_OVERFLOW	GPT14_COUNTER_OVERFLOW		
GPT14_COUNTER_UNDERFLOW	GPT14_COUNTER_UNDERFLOW		
GPT14_AD_TRIG_A	GPT14_AD_TRIG_A		
GPT14_AD_TRIG_B	GPT14_AD_TRIG_B		
GPT15_CAPTURE_COMPARE_INT_A	GPT15_CAPTURE_COMPARE_A		
GPT15_CAPTURE_COMPARE_INT_B	GPT15_CAPTURE_COMPARE_B		
GPT15_COMPARE_INT_C	GPT15_COMPARE_C		
GPT15_COMPARE_INT_D	GPT15_COMPARE_D		
GPT15_COMPARE_INT_E	GPT15_COMPARE_E		
GPT15_COMPARE_INT_F	GPT15_COMPARE_F		
GPT15_COUNTER_OVERFLOW	GPT15_COUNTER_OVERFLOW		
GPT15_COUNTER_UNDERFLOW	GPT15_COUNTER_UNDERFLOW		
GPT15_AD_TRIG_A	GPT15_AD_TRIG_A		
GPT15_AD_TRIG_B	GPT15_AD_TRIG_B		
GPT_UVW_EDGE	OPS_UVW_EDGE		
ETHER_IPLS	EPTPC_IPLS		



ETHER_MINT	EPTPC_MINT
ETHER_PINT	EPTPC_PINT
ETHER_EINTO	EDMAC0_EINT
ETHER_EINT1	EDMAC1_EINT
ETHER_ETHERO_RISE	EPTPC_TIMER0_RISE
ETHER_ETHER1_RISE	EPTPC_TIMER1_RISE
ETHER_ETHER2_RISE	EPTPC_TIMER2_RISE
ETHER_ETHER3_RISE	EPTPC_TIMER3_RISE
ETHER_ETHER4_RISE	EPTPC_TIMER4_RISE
ETHER_ETHER5_RISE	EPTPC_TIMER5_RISE
ETHER_ETHER0_FALL	EPTPC_TIMER0_FALL
ETHER_ETHER1_FALL	EPTPC_TIMER1_FALL
ETHER_ETHER2_FALL	EPTPC_TIMER2_FALL
ETHER_ETHER3_FALL	EPTPC_TIMER3_FALL
ETHER_ETHER4_FALL	EPTPC_TIMER4_FALL
ETHER_ETHER5_FALL	EPTPC_TIMER5_FALL
USBHS_DOFIFO	USBHS_FIFO_0
USBHS_D1FIFO	USBHS_FIFO_1
USBHS_USBIR	USBHS_USB_INT_RESUME
SCI0_RXI	SCI0_RXI
SCI0_TXI	SCI0_TXI
SCI0_TEI	SCI0_TEI
SCI0_ERI	SCI0_ERI
SCI0_AM	SCI0_AM
SCI0_RXI_OR_ERI	SCI0_RXI_OR_ERI
SCI1_RXI	SCI1_RXI
SCI1_TXI	SCI1_TXI
SCI1_TEI	SCI1_TEI
SCI1_ERI	SCI1_ERI
SCI1_AM	SCI1_AM
SCI2_RXI	SCI2_RXI
SCI2_TXI	SCI2_TXI
SCI2_TEI	SCI2_TEI
SCI2_ERI	SCI2_ERI
SCI2_AM	SCI2_AM
SCI3_RXI	SCI3_RXI
SCI3_TXI	SCI3_TXI
SCI3_TEI	SCI3_TEI
SCI3_ERI	SCI3_ERI
SCI3_AM	SCI3_AM
SCI4_RXI	SCI4_RXI
SCI4_TXI	SCI4_TXI
SCI4_TEI	SCI4_TEI
SCI4_ERI	SCI4_ERI
SCI4 AM	SCI4 AM



SCI5_RXI	SCI5_RXI	
SCI5_TXI	SCI5 TXI	
SCI5_TEI	SCI5_TEI	
SCI5_ERI	SCI5_ERI	
SCI5_AM	SCI5 AM	
SCI6_RXI	SCI6 RXI	
SCI6_TXI	SCI6 TXI	
SCI6_TEI	SCI6_TEI	
SCI6_ERI	SCI6_ERI	
SCI6_AM	SCI6_AM	
SCI7_RXI	SCI7_RXI	
SCI7_TXI	SCI7_TXI	
SCI7_TEI	SCI7_TEI	
SCI7_ERI	SCI7_ERI	
SCI7_AM	SCI7_AM	
SCI8_RXI	SCI8_RXI	
SCI8_TXI	SCI8_TXI	
SCI8_TEI	SCI8_TEI	
SCI8_ERI	SCI8_ERI	
SCI8_AM	SCI8_AM	
SCI9_RXI	SCI9_RXI	
SCI9_TXI	SCI9_TXI	
SCI9_TEI	SCI9_TEI	
SCI9_ERI	SCI9_ERI	
SCI9_AM	SCI9_AM	
RSPI0_SPRI	SPIO_RXI	
RSPI0_SPTI	SPI0_TXI	
RSPI0_SPII	SPI0_IDLE	
RSPI0_SPEI	SPIO_ERI	
RSPI0_SP_ELCTEND	SPI0_TEI	
RSPI1_SPRI	SPI1_RXI	
RSPI1_SPTI	SPI1_TXI	
RSPI1_SPII	SPI1_IDLE	
RSPI1_SPEI	SPI1_ERI	
RSPI1_SP_ELCTEND	SPI1_TEI	
QSPI_INTR	QSPI_INT	
SDHI_MMC0_ACCS	SDHIMMC0_ACCS	
SDHI_MMC0_SDIO	SDHIMMC0_SDIO	
SDHI_MMC0_CARD	SDHIMMC0_CARD	
SDHI_MMC0_ODMSDBREQ	SDHIMMC0_DMA_REQ	
SDHI_MMC1_ACCS	SDHIMMC1_ACCS	
SDHI_MMC1_SDIO	SDHIMMC1_SDIO	
SDHI_MMC1_CARD	SDHIMMC1_CARD	
SDHI_MMC1_ODMSDBREQ	SDHIMMC1_DMA_REQ	
EXT_DIVIDER_INTMD	DIVIDER_INT	



Renesas Synergy™ Platform

Migrating S7G2 MCUs Early Application Projects

TSIP_PROC_BUSY_N	SCE_PROC_BUSY	
TSIP_ROMOK_N	SCE_ROMOK	
TSIP_LONG_PLG_N	SCE_LONG_PLG	
TSIP_TEST_BUSY_N	SCE_TEST_BUSY	
TSIP_WRRDY_0_N	SCE_WRRDY_0	
TSIP_WRRDY_1_N	SCE_WRRDY_1	
TSIP_WRRDY_4_N	SCE_WRRDY_4	
TSIP_RDRDY_0_N	SCE_RDRDY_0	
TSIP_RDRDY_1_N	SCE_RDRDY_1	
TSIP_INTEGRATE_WRRDY_N	SCE_INTEGRATE_WRRDY	
TSIP_INTEGRATE_RDRDY_N	SCE_INTEGRATE_RDRDY	
LCDC_LCDC_LEVEL_0	GLCDC_LINE_DETECT	
LCDC_LCDC_LEVEL_1	GLCDC_UNDERFLOW_1	
LCDC_LCDC_LEVEL_2	GLCDC_UNDERFLOW_2	
TWOD_ENGINE_IRQ	DRW_INT	
JPEG_JEDI	JPEG_JEDI	
JPEG_JDTI	JPEG_JDTI]	



#### Website and Support

Support: https://synergygallery.renesas.com/support

Technical Contact Details:

- America: <u>https://renesas.zendesk.com/anonymous\_requests/new</u>
- Europe: <u>https://www.renesas.com/en-eu/support/contact.html</u>
- Japan: <u>https://www.renesas.com/ja-jp/support/contact.html</u>

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### **Revision History**

		Descript	on	
Rev.	Date	Page	Summary	
0.90	Oct 9, 2015	-	Initial release	
0.91	Jan 12, 2016	40	Support URL updated.	
			Update document to describe migration to SSP v.1.0.0 instead of SSP v 1.0.0 beta 1 and $e^2$ studio versions 4.2.0.012 and	
			later instead of 4.1.0.017.	
0.92	Nov 18, 2016	-	Minor format changes.	

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