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M16C/62A Group

Method of A-D Conversion and Accuracy

1. Abstract

The following article introduces method of A-D conversion and accuracy.

2. Introduction

The explanation of this issue is M16C/62A Group.

3. Contents

3.1 Method of A-D Conversion (10-bit mode)

(1) The A-D converter compares the reference voltage (Vref) generated internally based on the contents of the successive comparison register with the analog input voltage (V_{IN}) input from the analog input pin. Each bit of the comparison result is stored in the successive comparison register until analog-to-digital conversion (successive comparison method) is complete. If a trigger occurs, the A-D converter carries out the following:

1. Fixes bit 9 of the successive comparison register.
   Compares Vref with V_{IN}: [In this instance, the contents of the successive comparison register are "1000000000_2" (default).]
   Bit 9 of the successive comparison register varies depending on the comparison result as follows.
   If Vref < V_{IN}, then "1" is assigned to bit 9.
   If Vref > V_{IN}, then "0" is assigned to bit 9.

2. Fixes bit 8 of the successive comparison register.
   Sets bit 8 of the successive comparison register to "1", then compares Vref with V_{IN}.
   Bit 8 of the successive comparison register varies depending on the comparison result as follows:
   If Vref < V_{IN}, then "1" is assigned to bit 8.
   If Vref > V_{IN}, then "0" is assigned to bit 8.

3. Fixes bit 7 through bit 0 of the successive comparison register.
   Carries out step 2 above on bit 7 through bit 0.
   After bit 0 is fixed, the contents of the successive comparison register (conversion result) are transmitted to A-D register i.

Vref is generated based on the latest content of the successive comparison register. Table 1 shows the relationship of the successive comparison register contents and Vref. Table 2 shows how the successive comparison register and Vref vary while A-D conversion is in progress. Figure 1 shows theoretical A-D conversion characteristics.

Table 1. Relationship of the successive comparison register contents and Vref

Successive approximation register : n	Vref (V)
0	0
1 to1023	$\frac{V_{REF}}{1024} \times n - \frac{V_{REF}}{2048}$

Table 2. Variation of the successive comparison register and Vref while A-D conversion is in progress (10-bit mode)

	Successive approximation register	Vref change
A-D converter stopped	b9 … b0 1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$ [V]
1st comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} - \frac{V_{REF}}{2048}$ [V]
2nd comparison	n9 1 0 0 0 0 0 0 0 0 ↑ 1st comparison result	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{2048}$ [V] $\left(\begin{array}{ll} n_9 = 1 & +\frac{V_{REF}}{4} \\ n_9 = 0 & -\frac{V_{REF}}{4} \end{array} \right)$
3rd comparison	n9 n8 1 0 0 0 0 0 0 0 ↑ 2nd comparison result	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{2048}$ [V] $\left(\begin{array}{ll} n_8 = 1 & +\frac{V_{REF}}{8} \\ n_8 = 0 & -\frac{V_{REF}}{8} \end{array} \right)$
⋮	⋮	⋮
10th comparison	n9 n8 n7 n6 n5 n4 n3 n2 n1 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} \pm ...... \pm \frac{V_{REF}}{1024} - \frac{V_{REF}}{2048}$ [V]
Conversion complete	n9 n8 n7 n6 n5 n4 n3 n2 n1 n0 This data transfers to the bit 0 to bit 9 of A-D register i.	

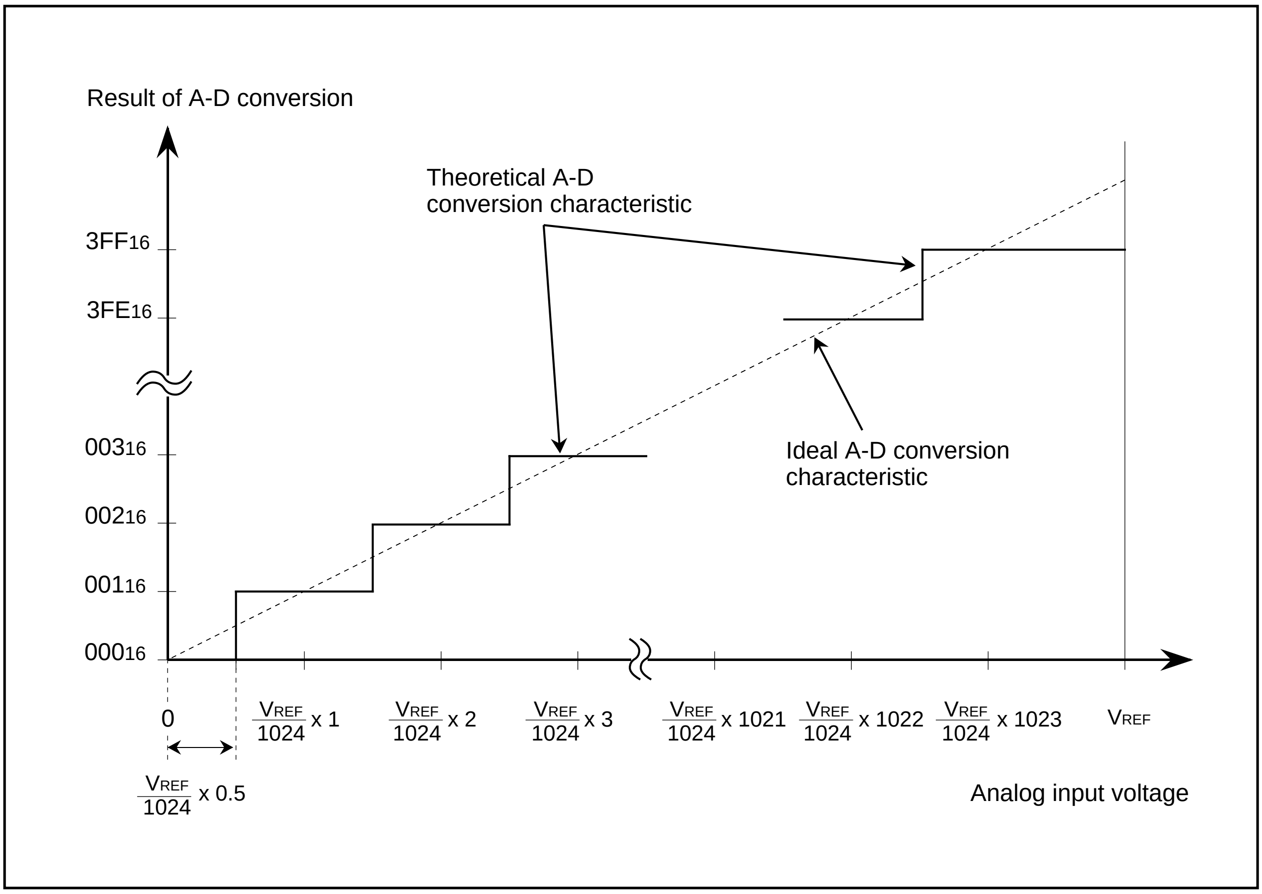

Figure 1. Theoretical A-D conversion characteristics (10-bit mode)

3.2 Method of A-D Conversion (8-bit mode)

(1) In 8-bit mode, 8 higher-order bits of the 10-bit successive comparison register becomes A-D conversion result. Hence, if compared to a result obtained by using an 8-bit A-D converter, the voltage compared is different by 3 VREF/2048 (see what are underscored in Table 3), and differences in stepping points of output codes occur as shown in Figure 2.

Table 3. The comparison voltage in 8-bit mode compared to 8-bit A-D converter

		8-bit mode	8-bit A-D converter
Comparison voltage Vref	n = 0	0	0
	n = 1 to 255	$\frac{V_{REF}}{2^8} \times n - \underline{\frac{V_{REF}}{2^{10}} \times 0.5}$	$\frac{V_{REF}}{2^8} \times n - \underline{\frac{V_{REF}}{2^8} \times 0.5}$

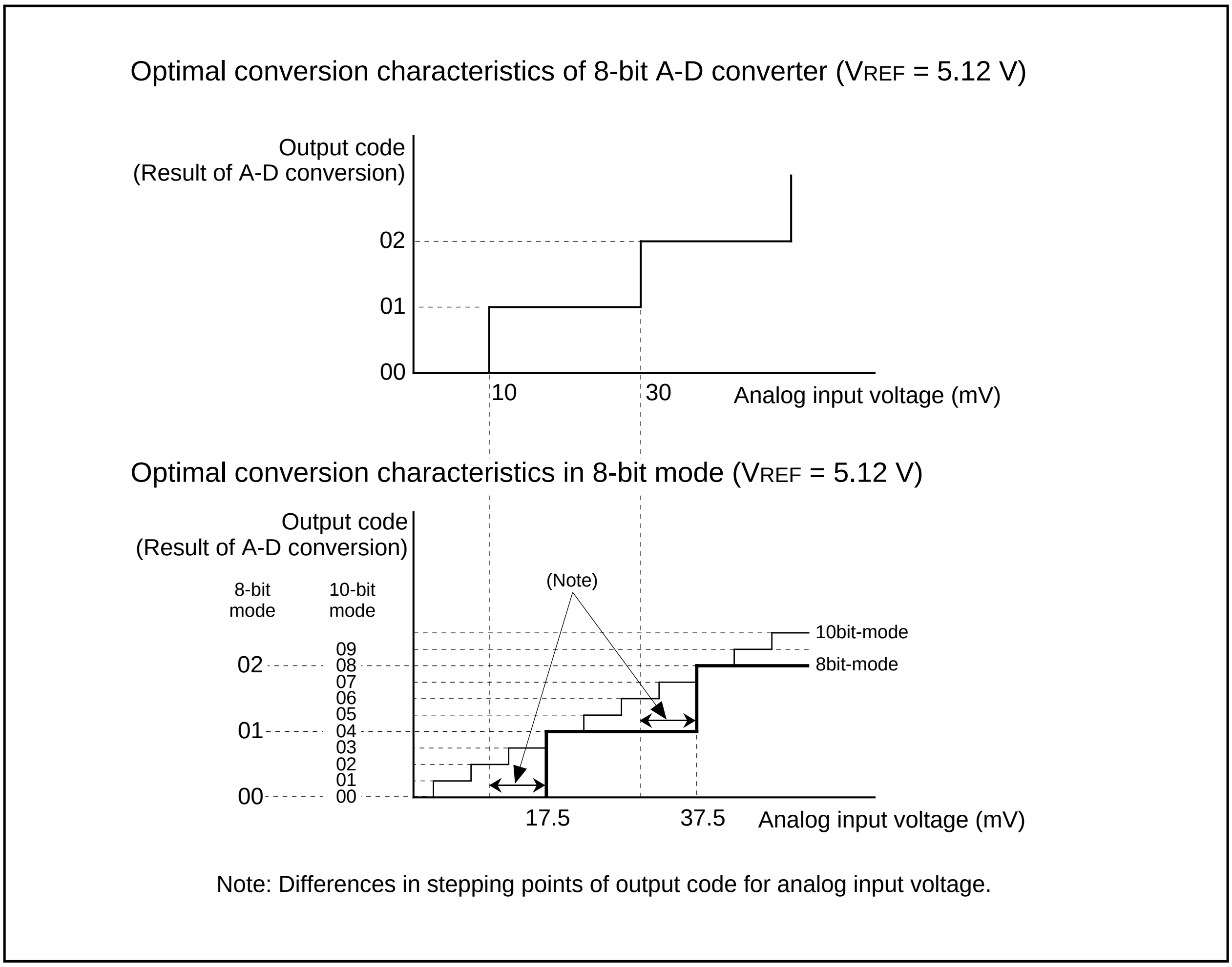

Figure 2. The level conversion characteristics of 8-bit mode and 8-bit A-D converter

Table 4. Variation of the successive comparison register and Vref while A-D conversion is in progress (8-bit mode)

	Successive approximation register	Vref change
A-D converter stopped	b9 … b0: 1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$ [V]
1st comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} - \frac{V_{REF}}{2048}$ [V]
2nd comparison	n9 1 0 0 0 0 0 0 0 0 (↑ 1st comparison result)	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{2048}$ [V] (n9 = 1: $+\frac{V_{REF}}{4}$; n9 = 0: $-\frac{V_{REF}}{4}$)
3rd comparison	n9 n8 1 0 0 0 0 0 0 0 (↑ 2nd comparison result)	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{2048}$ [V] (n8 = 1: $+\frac{V_{REF}}{8}$; n8 = 0: $-\frac{V_{REF}}{8}$)
⋮	⋮	⋮
8th comparison	n9 n8 n7 n6 n5 n4 n3 1 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} \pm \ldots\ldots \pm \frac{V_{REF}}{256} - \frac{V_{REF}}{2048}$ [V]
Conversion complete	n9 n8 n7 n6 n5 n4 n3 n2 0 0 — This data transfers to bit 0 to bit 7 of A-D register i.	

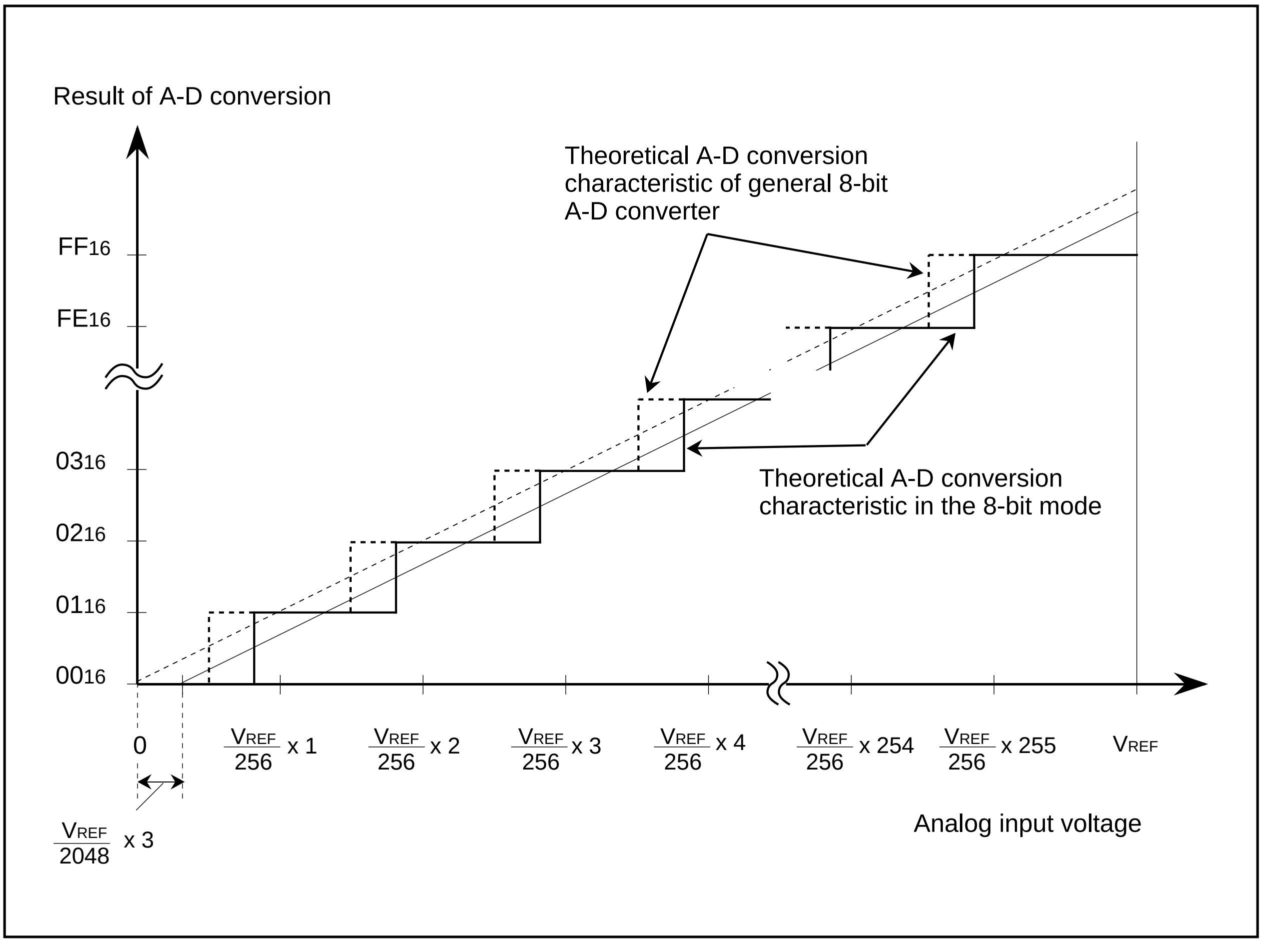

Figure 3. Theoretical A-D conversion characteristics (8-bit mode)

3.3 Absolute Accuracy and Differential Non-Linearity Error

3.3.1 Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A-D conversion characteristics, and actual A-D conversion result. When measuring absolute accuracy, the voltage at the middle point of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A-D conversion characteristics, is used as an analog input voltage. For example, if 10-bit resolution is used and if VREF (reference voltage) = 5.12 V, then 1-LSB width becomes 5 mV, and 0 mV, 5 mV, 10 mV, 15 mV, 20 mV, ····are used as analog input voltages. If analog input voltage is 25 mV, “absolute accuracy = ± 3LSB” refers to the fact that actual A-D conversion falls on a range from “002_{16}” to ”008_{16}” though an output code, “005_{16}”, can be expected from the theoretical A-D conversion characteristics. Zero error and full-scale error are included in absolute accuracy.

Also, all the output codes for analog input voltage between VREF and AVcc becomes “$3FF_{16}$”.

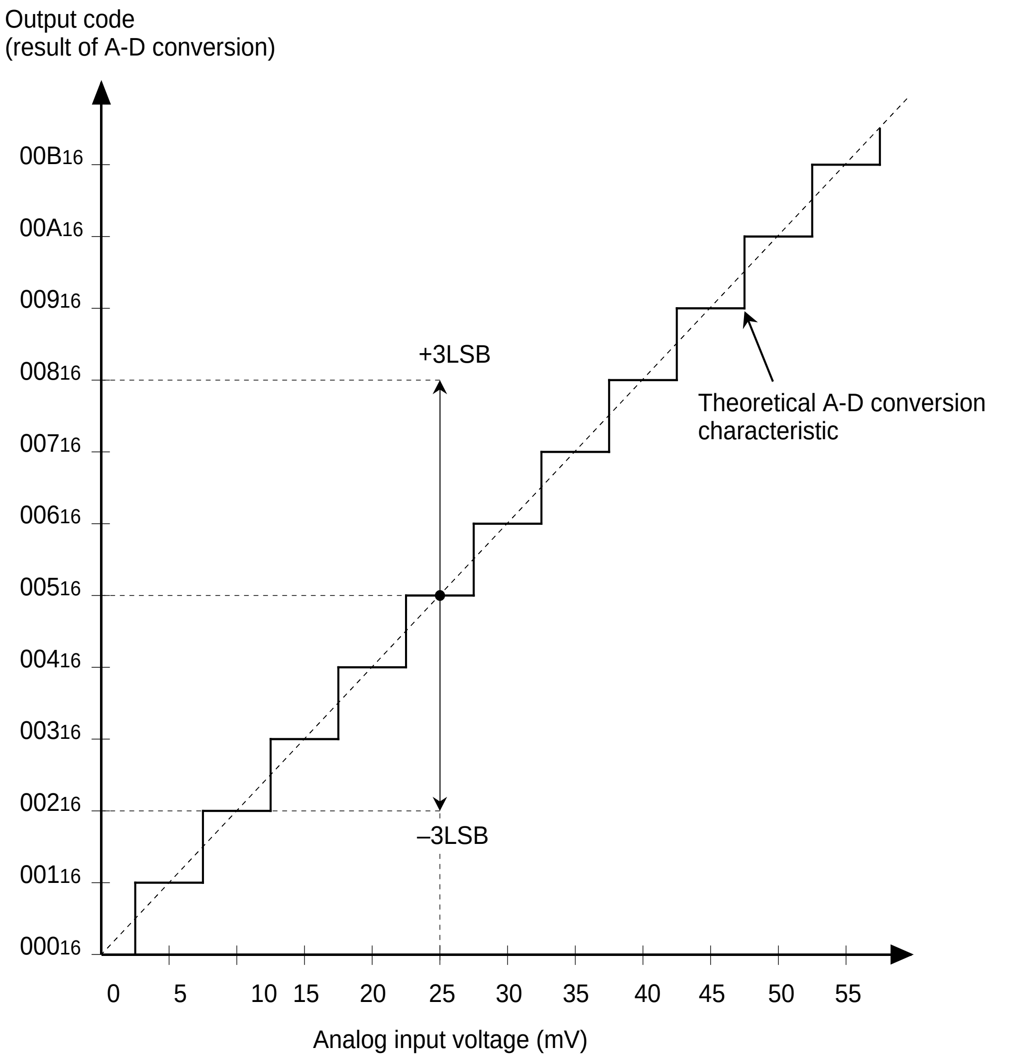

Figure 4. Absolute accuracy (10-bit resolution)

3.3.2 Differential non-linearity error

Differential non-linearity error refers to the difference between 1-LSB width based on the theoretical A-D conversion characteristics (an analog input width that can meet the expectation of outputting an equal code) and an actually measured 1-LSB width (analog input voltage width that outputs an equal code). If 10-bit resolution is used and if V_{REF} (reference voltage) = 5.12 V, "differential non-linearity error = ± 1LSB" refers to the fact that 1-LSB width actually measured falls on a range from 0 mV to 10 mV though 1-LSB width based on the theoretical A-D conversion characteristics is 5 mV.

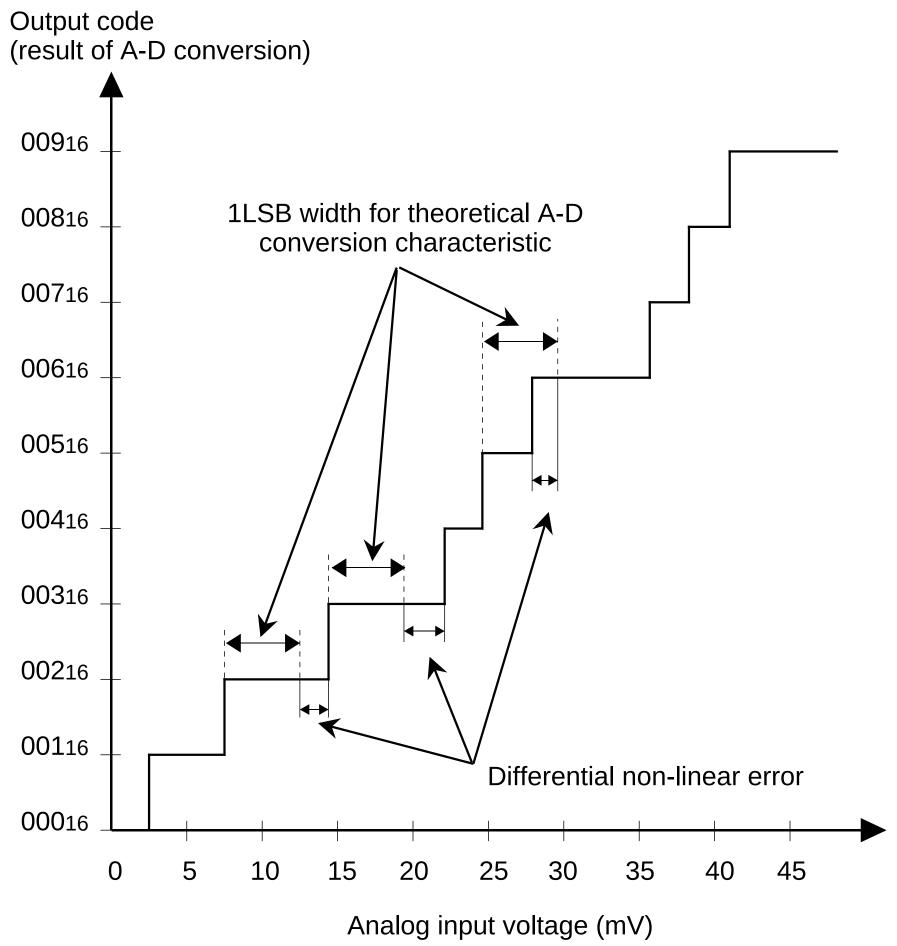

Figure 5. Differential non-linearity error (10-bit resolution)

REVISION HISTORY	M16C/62A Group Application Note Method of A-D Conversion and Accuracy

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		Page	Summary
1.00	Sep, 30, 2003	-	First edition issued