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Renesas Electronics Corporation

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# M66591

## Guidelines for board design (Preliminary)

**Notice : This is not a final specification. Some parametric items are subject to change.**

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## 1. Summary

This document states the guidelines for USB2.0 Hi-Speed board design.

## 2. Introduction

The examples of application explained in this document apply to the following ASSP.

- USB device: M66591

### 3. Cautions in designing the board

#### 3.1 USB transmission line

The USB transmission line indicates the pattern that connects the USB connector and the M66591. The USB2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission line must be designed as a high-frequency circuit. Impedance control is required for the USB transmission line.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance  $90 \Omega (\pm 15\%)$ .
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. As for the details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB receptacle to the M66591. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 100 mm and the difference between the pattern lengths for D+ and D- is less than 2.5 mm for generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more.
- Do not allocate other signal lines near the USB transmission line. Particularly lines of heavily fluctuating signals, such as clock and data bus lines, must be allocated far from the USB transmission line.
- Allocate the USB transmission line on the same layer without passing it through a through hole.
- Do not bend the USB transmission line at acute angles (right angles). Bend it gently.
- If a terminal resistance pattern is provided on the USB transmission line, the characteristic impedance of the transmission line is disturbed. Do not set the terminal resistance pattern of the M66591 on the USB transmission line. Allocate a signal line having the same width as that of the transmission line outside the transmission line, and provide the resistance pattern on the signal line.



- It is recommended to girdle the clock, reset, read, write and chip select signals at grounds.
- When a resistance is connected to the USB transmission line, allocate the part near the USB transmission line. The connecting wire must be as short as possible.

### 3.2 Power supply and ground pattern

- It is recommended to separate power supplies and ground patterns into digital and analog. When the voltage of the control MCU is 1.8 V, it is necessary to separately apply 1.8 V to VIF of the M66591. When the voltage of the control MCU is 3.3 V, VDD and VIF must be powered from the same power supply.
- Connect the power supplies and grounds firmly on wide areas. Connect PLLGND, BIASGND and AFEAGND on sufficiently wide areas. Refer to Figure 2 “Analog GND” on page 7.
- Tantalum solid electrolytic capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as capacitors for power supplies.
- Aluminum electrolytic capacitors affect the jitter value during measurement of EYE diagram. Use the capacitors after sufficiently designing and testing them. Refer to Table 3 “RMS Jitter value” on page 9.

### 3.3 Oscillation

- Allocate an oscillation circuit near XIN and XOUT of the USB device. It is recommended to girdle XIN and XOUT at grounds.

### 3.4 Reset

- It is recommended to girdle the reset signal at ground. For resetting, a reset IC (M5195xx Series) is recommended.

### 3.5 VBUS

- The USB standard recommends that a capacitor (1.0 $\mu$ F) should be mounted on VBUS to absorb flyback voltage generated when the USB cable is connected and disconnected.

### 3.6 Non-connected pins

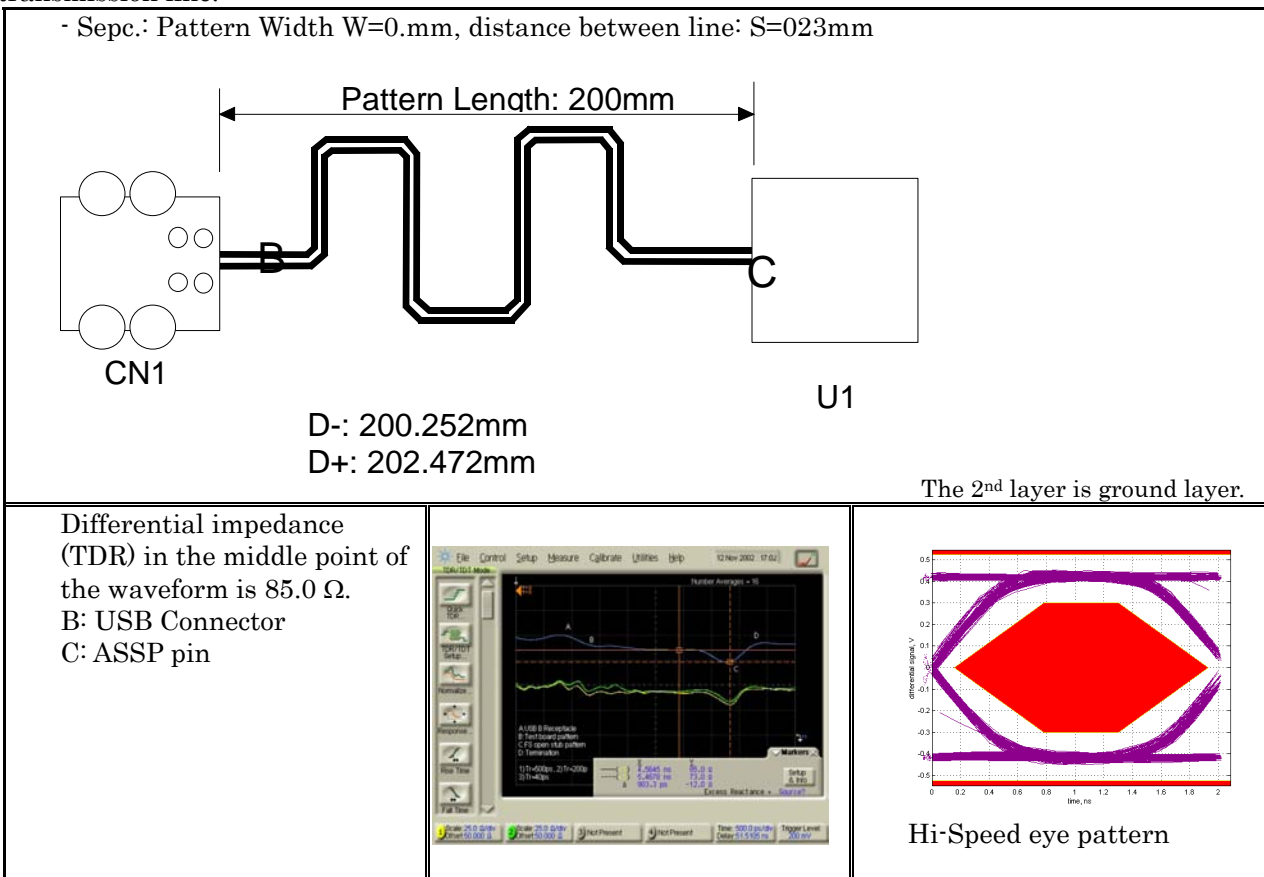
- Please refer to “Table 1.2 example of not used pins” of M66591 Datasheet (REJ03F0101).

### 3.7 REFRIN pin

- Allocate the reference resistor, 1.2k $\Omega$  $\pm$ 1%, between REFRIN-pin and BIASGND.
- Allocate the reference resistor as close as possible to M66591.
- REFRIN-pin, the reference resistor and BIASGND should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for REFRIN-pin and BIASGND. Then the pattern should be connected to the analog ground. The pattern should be designed avoiding the potential for common impedance between REFRIN and other signals.
- To prevent cross talk, High frequently switching signals like DP, DM, clocks, and control signals for Addresses and Data, should not be placed near by the reference resistor, and their patterns should neither get across nor go side by side with the wiring pattern between the reference resistor and REFRIN-pin.
- Wiring pattern between the reference resistor and REFRIN-pin should be guard-ringed with ground.

3.8 The data of test board

The impedance and the eye pattern shown in below are the data of a test board with 200mm transmission line.



#### 4. M66591 utility board M3A-0037

An example is shown below using the utility board M3A-0037G01 on which the M66591GP has been mounted.

The M3A-0037G01 is a size of 70 mm × 80 mm × 1.6 mm and used in combination with the evaluation board M3A-0033. The M3A-0037G01 cannot operate by itself. It is possible to connect it with other boards depending on the connector specifications.

The outline of the specifications is shown as follows:

- USB device: M66591GP
- Oscillation frequency: 24MHz
- Transmission speed: 480Mbps
- Board name: M3A-0037G01 (Control MCU Board M3A-0033)

##### 4.1 USB transmission line

The M3A-0037G01 uses a glass epoxy 4-layer board (FR4), and the USB transmission line is passed through the first layer of the board. The pattern width is 0.35 mm, and the pattern pitch is 0.23 mm. The second layer is a ground layer, the third is a power supply layer, and the fourth is a signal and analog ground layer.

##### 4.2 Power supply and ground pattern

The power supplies and ground patterns are separated into digital and analog.

Table 1 and Table 2 show the classifications of power supplies and grounds in the M3A-0037G01.

Table 1 Classification of M3A-0037G01 power supplies

M66591		Classification of M3A-0037G01 power supplies (O indicates that these pins are connected.)			
Pin name	M66591 pin No.	Analog power supply (AFEAVDD)	Digital power supply 1 (AFEDVDD)	Digital power supply 2 (VDD)	Interface power supply (VIF)
	Capacitor	(C1) 100μF tantalum 0.1μF ceramic 10pF ceramic	(C2) 47μF tantalum 0.1μF ceramic 10pF ceramic	(C3) 100μF electrolysis 0.1μF ceramic 10pF ceramic	(C15) 100μF electrolysis 0.1μF ceramic 10pF ceramic
AFEAVDD	2, 6, 10	O			
BIASVDD	18	O			
PLLVD	20	O			
AFEDVDD	12		O		
VDD	21, 30, 48			O	
VIF	28, 58, 80				O

- Each power supply pin is provided with a 0.01μF ceramic capacitor.
- The digital power supplies 1 and 2 can also be used as one power supply.



Table 2 Classification of M3A-0037G01 grounds

M66591		Classification of M3A-0037G01 grounds	
Pin name	M66591 pin No.	Analog ground (AGND)	Digital ground (DGND)
AFEAGND	3,9	O	
BIASGND	16	O	
PLLGND	19	O	
AFEDGND	11		O
DGND	1,22,29,49,59,74		O

- All the digital grounds (DGND) are solid ground plane except the areas near the USB connector on the second layer. Refer to the following Figure 1 .
- The analog ground (AGND) is allocated on the fourth layer. The analog ground has almost the same shape as the analog power supply (AFEAVDD) on the third layer. Refer to the following Figure 2.
- The metallic case of the USB connector is connected to the chassis ground (FGND). The chassis ground can be disconnected from the digital ground (solid ground plane) and used independently by pattern cutting of the jumper JP5 at the rear.

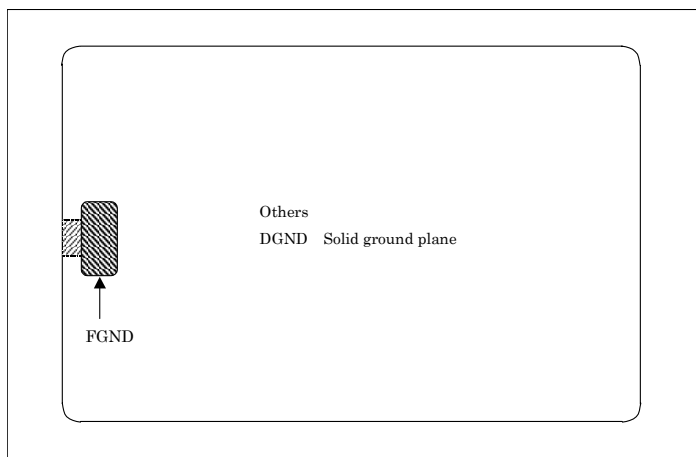


Figure 1 M3A-0037 second layer

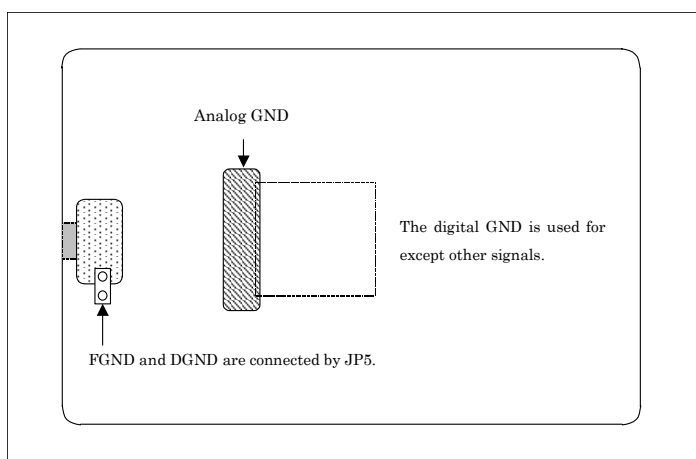


Figure 2 M3A-0037 fourth layer

### 4.3 Oscillation

The oscillation circuit of the M3A-0037G01 has a pattern on which one of the crystal oscillators made by Daishinku Corp. can be mounted among the DSX321G (or DSX630G) at 12MHz, 24MHz or 48MHz. Reset

A 0.1 $\mu$ F capacitor is connected between the reset pin and ground to prevent operation errors in the M3A-0037G01.

### 4.4 Reset

A 0.1 $\mu$ F capacitor is connected between the reset pin and ground to prevent operation errors in the M3A-0037G01.

### 4.5 VBUS

A 1.0 $\mu$ F chip monolithic ceramic capacitor is mounted between VBUS and ground in the M3A-0037G01.

### 4.6 Measures against EMI and measures against surge

The M3A-0037G01 provides the following pattern on the USB transmission line as an experimental pattern for measures against EMI and measures against surge.

- Common mode choke coil(L2) : DLW21HN900SQ2 (Murata Manufacturing Co., Ltd.)  
(When the coil is mounted, the wire for L2 foot pattern should be cut.)
- ESD protection diode(U2) : HZM6.2Z4MFA / HZM6.8Z4MFA (RENESAS)

Note: Though the influence on the eye diagram of these parts has been confirmed, please fully evaluate other influences in user system.

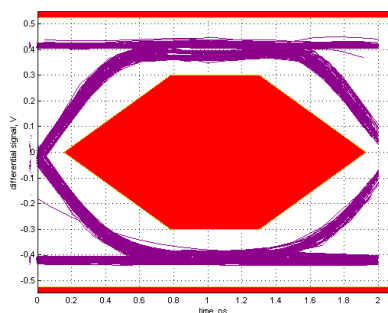
### 4.7 EYE pattern

We made experiments to verify how capacitor C1 for the analog power supply and capacitor C2 for the digital power supply of the M3A-0037G01 affect the EYE pattern when tantalum solid electrolytic capacitors, aluminum electrolytic capacitors and ceramic capacitors are used. The results of the experiments are shown below.

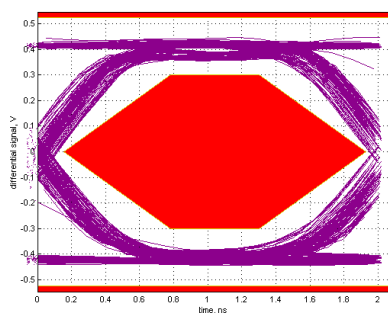
The EYE pattern was measured, and the RMS Jitter values were compared. Table 3 shows the results of measurement of the RMS Jitter values. Since the RMS Jitter values showed a certain degree of dispersion, data were obtained several times, and the average values were evaluated.

Measuring instrument: Inifiniium (Agilent Technology)  
 Probe: 1159A (Agilent Technology)  
 Test Fixture: Signal Quality Fixture (Agilent Technology)  
 Power Supply: PA18-3 (KENWOOD)  
 Board for M66591GP: M3A-0037G01 Rev.A with M3A-0033 Rev.B

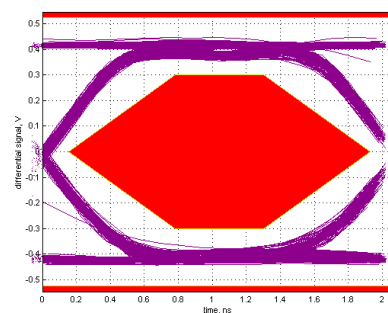
The EYE patterns when the capacitors were used are shown below.



EYE pattern when tantalum solid electrolytic capacitors were used. (Jitter: 27.8ps)



EYE pattern when aluminum electrolytic capacitors were used. (Jitter: 61.0ps)



EYE pattern when ceramic capacitors 10µF were used. (Jitter: 26.9ps)

Table 3 RMS Jitter value unit [ps]

Measurement time	M3A-0037 G01 Rev.A							
	Tantalum C1: 100µF C2: 47µF	pass or fail	Aluminum electrolysis C1: 100µF C2: 100µF	pass or fail	Ceramic C1: 10µF C2: 10µF	pass or fail	Ceramic C1: 22µF C2: 22µF	pass or fail
1	38.7	O	56.9	O	35.5	O	30.2	O
2	27.8	O	54.9	O	33.0	O	41.1	O
3	35.8	O	47.2	O	32.1	O	25.1	O
4	33.0	O	42.7	O	26.9	O	38.4	O
5	52.8	O	46.2	O	32.8	O	37.7	O
6	35.3	O	44.7	O	30.8	O	42.1	O
7	57.7	O	32.2	O	32.7	O	28.1	O
8	25.9	O	46.8	O	39.2	O	35.4	O
9	32.0	O	52.2	O	49.7	O	34.6	O
10	31.6	O	61.0	O	32.9	O	40.7	O
Total	370.6		484.9		345.6		353.4	
Average	37.06		48.49		34.56		35.34	
Result	Good		Fair		Good		Good	

The pass or fail was determined based on the results of evaluation of the signal quality. O indicates a pass.

## 5. Reference document

- Datasheet  
M66591 datasheet
- Universal Serial Bus Specification Revision 2.0 April 27,2000

## 6. Web site information and technical support

- Renesas USB Device : <http://www.renesas.com/en/usb>
- Technical support : <http://www.renesas.com/eng/contact/index.html>

REVISION HISTORY	M66591 Guidelines for board design
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Rev.	Date	Description	
		Page	Summary
1.00	July, 2002	-	First edition issued
1.01	Feb.25.05	2	3.1 USB transmission line - Deleted description of common impedance. - Changed description of pattern length from 70mm to 100mm
		3	3.6 Non-connected pins - Changed the description for explaining to "Please refer to "Table 1.2 example of not used pins" of M66591 Datasheet (REJ03F0101)"
		3	Insert "3.7 REFRIN pin" and "3.8 The data of test board"
		6	4.6 Measures against EMI and measures against surge - Deleted ESD protection diode (U2): SRV05-4 SEMTECH

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