M32C/84, 85, 87, 88, 8A and 8B Groups

Data Transmission Using the Serial Interface in Clock Synchronous Mode

R01AN0701EJ0100
Rev. 1.00
Feb. 29, 2012

Abstract

This document describes how to transmit data using the serial interface in clock synchronous mode.

Products

M32C/84 Group
M32C/85 Group
M32C/87 Group
M32C/88 Group
M32C/8A Group
M32C/8B Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document describes how to transmit data to a receiving device using the serial interface (UART0) in clock synchronous mode.
Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows a Connection Example.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Serial interface (UART0)	Data transmission

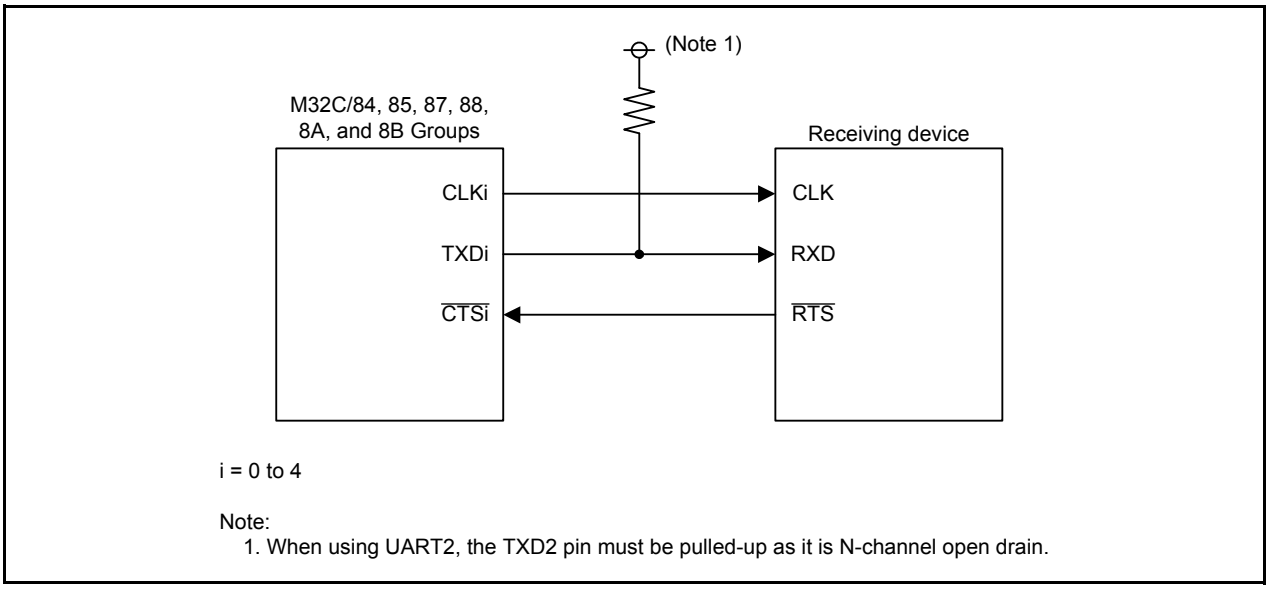


Figure 1.1 Connection Example

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	M3087BFLGP (M32C/87 Group)
Operating frequencies	• Main clock: 32 MHz • CPU clock: 32 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Version 4.08
C compiler	Renesas Electronics M32C Series Compiler V.5.42 Release 00
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0fe0000 -D__E8__ -D__WORK_RAM__=0x100 -c -finfo -dir “$(CONFIGDIR)” -M82 Default setting is used in the integrated development environment.
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Reference Application Note

The application note listed below is associated with this application note. Refer to the following application note for additional information.

- M32C/80 Series Data Reception Using the Serial Interface in Clock Synchronous Mode (R01AN0702EJ0100)

4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P6_0/$\overline{\text{CTS0}}$	Input	Input for controlling transmission
P6_1/CLK0	Output	Clock output
P6_3/TXD0	Output	Serial data output

5. Software

This chapter explains the setting procedure to transmit data at 1 Mbps (Xin = 32 MHz) using UART0 in clock synchronous mode. The formula for determining the baud rate is as follows:

$$\text{Baud rate} = \frac{\text{U0BRG register count source}}{2 \times (\text{U0BRG register setting value} + 1)}$$

The settings for this application note are listed in Table 5.1.

Table 5.1 Settings

Item	Setting
Transfer mode	Clock synchronous mode
Transmit/receive clock	Internal clock
Baud rate	1 Mbps (Xin = 32 MHz)
Transmission control	CTS function
Bit order	LSB first
Transmit interrupt source	U0IRS bit is 0 (no data in the U0TB register)
Transmit interrupt request generation timing	When data is transferred from the U0TB register to the UART0 transmit shift register (when transmission starts)
CLK polarity	Transmit data is output at the falling edge and receive data is input at the rising edge of the serial clock.
TXD and RXD I/O polarity inverse	Not inverted

CLK output and TXD output are used to transmit data. To use the CLK and TXD output, set the port direction bits for the ports corresponding to the CLK pin and TCD pin, and set the function select register. Table 5.2 lists the Pin Settings when Transmitting Data in Clock Synchronous Mode Using the M32C/87 Group.

Table 5.2 Pin Settings when Transmitting Data in Clock Synchronous Mode Using the M32C/87 Group

Channel	Pin	Bit Setting			
		Registers PD6, PD7, and PD9 (2)	Registers PSC and PSC3	Registers PSL0, PSL1, and PSL3	Registers PS0, PS1, and PS3 (1, 2)
UART0	P6_0/$\overline{\text{CTS0}}$ input	PD6_0 = 0	—	—	PS0_0 = 0
	P6_1/CLK0 output	—	—	PSL0_1 = 0	PS0_1 = 1
	P6_3/TXD0 output	—	—	PSL0_3 = 0	PS0_3 = 1
UART1	P6_4/$\overline{\text{CTS1}}$ input	PD6_4 = 0	—	—	PS0_4 = 0
	P6_5/CLK1 output	—	—	PSL0_5 = 0	PS0_5 = 1
	P6_7/TXD1 output	—	—	PSL0_7 = 0	PS0_7 = 1
UART2	P7_0/TXD2 output	—	PSC_0 = 0	PSL1_0 = 0	PS1_0 = 1
	P7_2/CLK2 output	—	PSC_2 = 0	PSL1_2 = 0	PS1_2 = 1
	P7_3/$\overline{\text{CTS2}}$ input	PD7_3 = 0	—	—	PS1_3 = 0
UART3	P9_0/CLK3 output	—	—	PSL3_0 = 0	PS3_0 = 1
	P9_2/TXD3 output	—	—	PSL3_2 = 0	PS3_2 = 1
	P9_3/$\overline{\text{CTS3}}$ input	PD9_3 = 0	—	PSL3_3 = 0	PS3_3 = 0
UART4	P9_4/$\overline{\text{CTS4}}$ input	PD9_4 = 0	—	PSL3_4 = 0	PS3_4 = 0
	P9_5/CLK4 output	—	—	—	PS3_5 = 1
	P9_6/TXD4 output	—	PSC3_6 = 0	—	PS3_6 = 1

Notes:
1. Set registers PS0, PS1, and PS3 after setting the other registers.
2. Set registers PD9 and PS3 immediately after the PRC2 bit in the PRCR register is set to 1 (write enable). Do not generate an interrupt or a DMA or DMAC II transfer between these two instructions.

5.1 Operation Overview

A description of the sample code operation is as follows:

(1) Transmission enabled
After setting the TE bit in the U0C1 register to 1 (transmit operation enabled) and writing transmit data to the U0TB register, the data waits to be transmitted.

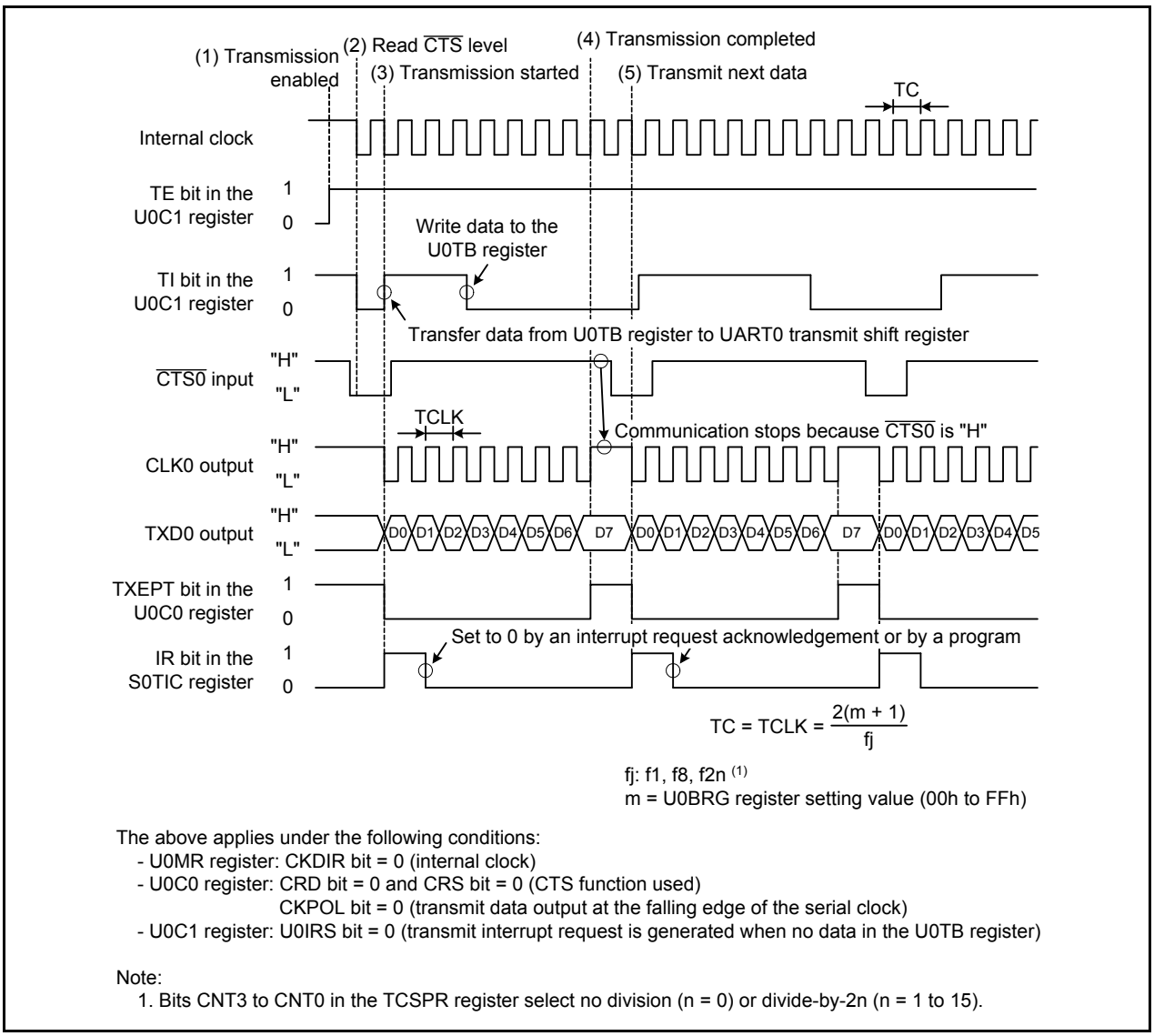
(2) $\overline{\text{CTS0}}$ read
Transmission starts when the input signal to the $\overline{\text{CTS0}}$ pin is low. The input signal to the $\overline{\text{CTS0}}$ pin is controlled by the receiving device.

(3) Transmission started
Synchronizing with the falling edge of the first transmit/receive clock, transmit data written to the U0TB register is transferred to the UART0 transmit shift register. At the same time, the IR bit in the S0TIC register becomes 1 (interrupt requested), and the LSB in the transmit data is transmitted from the TXD0 pin. From the second bit, data transmission is synchronized with the falling edge of the transmit/receive clock.

(4) Transmission completed
After 1 byte of data is transmitted, the TXEPT bit in the U0C0 register becomes 1 (no data in the transmit shift register) and transmission complete is shown. The transmit/receive clock stops high.

(5) Next data is transmitted
If the next data to be transmitted is set to the U0TB register before the 8th bit is output, transmission will continue.

Figure 5.1 shows the Timing Diagram.



The above applies under the following conditions:
- U0MR register: CKDIR bit = 0 (internal clock)
- U0C0 register: CRD bit = 0 and CRS bit = 0 (CTS function used)
  CKPOL bit = 0 (transmit data output at the falling edge of the serial clock)
- U0C1 register: U0IRS bit = 0 (transmit interrupt request is generated when no data in the U0TB register)

Note:
1. Bits CNT3 to CNT0 in the TCSPR register select no division (n = 0) or divide-by-2n (n = 1 to 15).

Figure 5.1 Timing Diagram

5.2 Constant

Table 5.3 lists the Constant Used in the Sample Code.

Table 5.3 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
TRN_DATA	00h	Initial value of the transmit data

5.3 Flowcharts

5.3.1 Main Processing

Figure 5.2 shows the Main Processing.

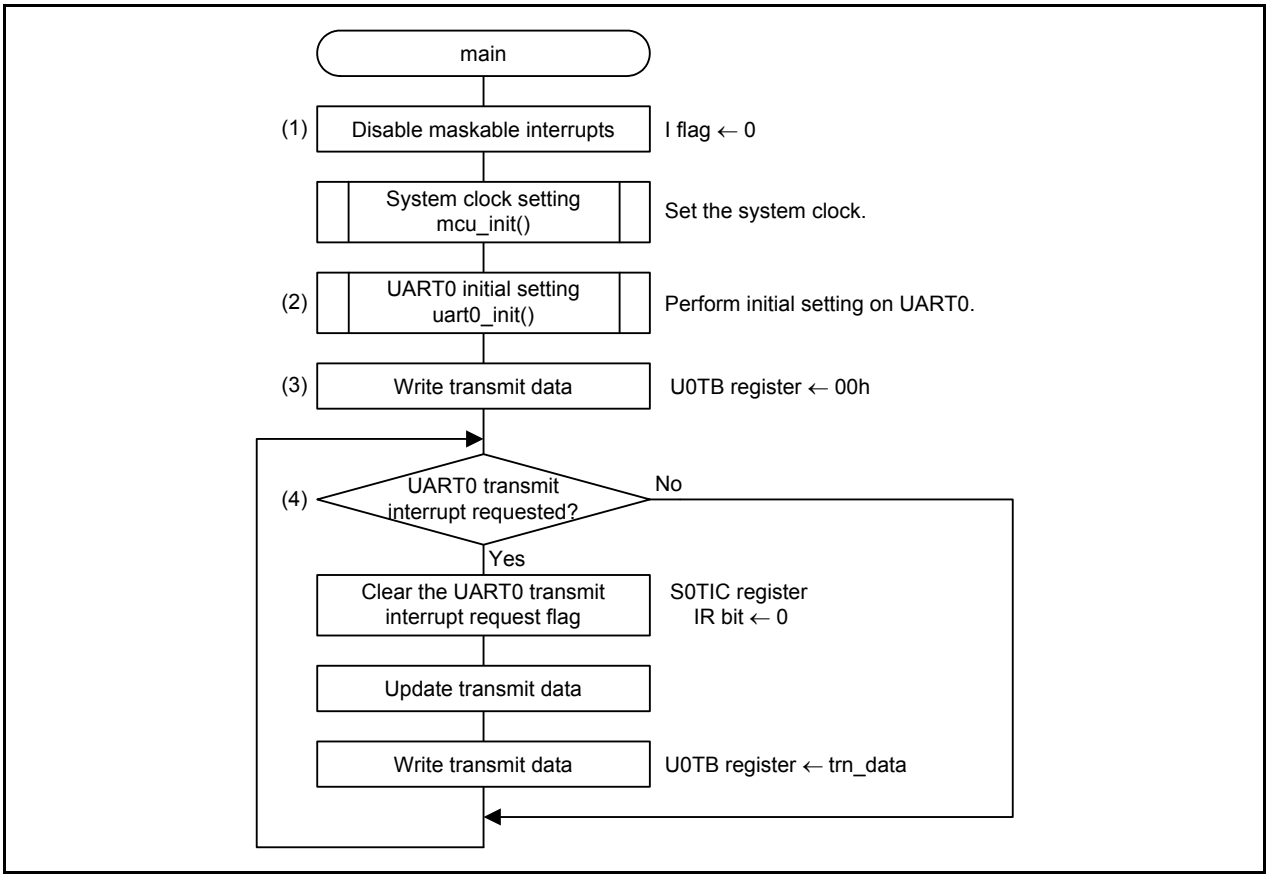


Figure 5.2 Main Processing

5.3.2 UART0 Initial Setting

Figure 5.3 shows the UART0 Initial Setting.

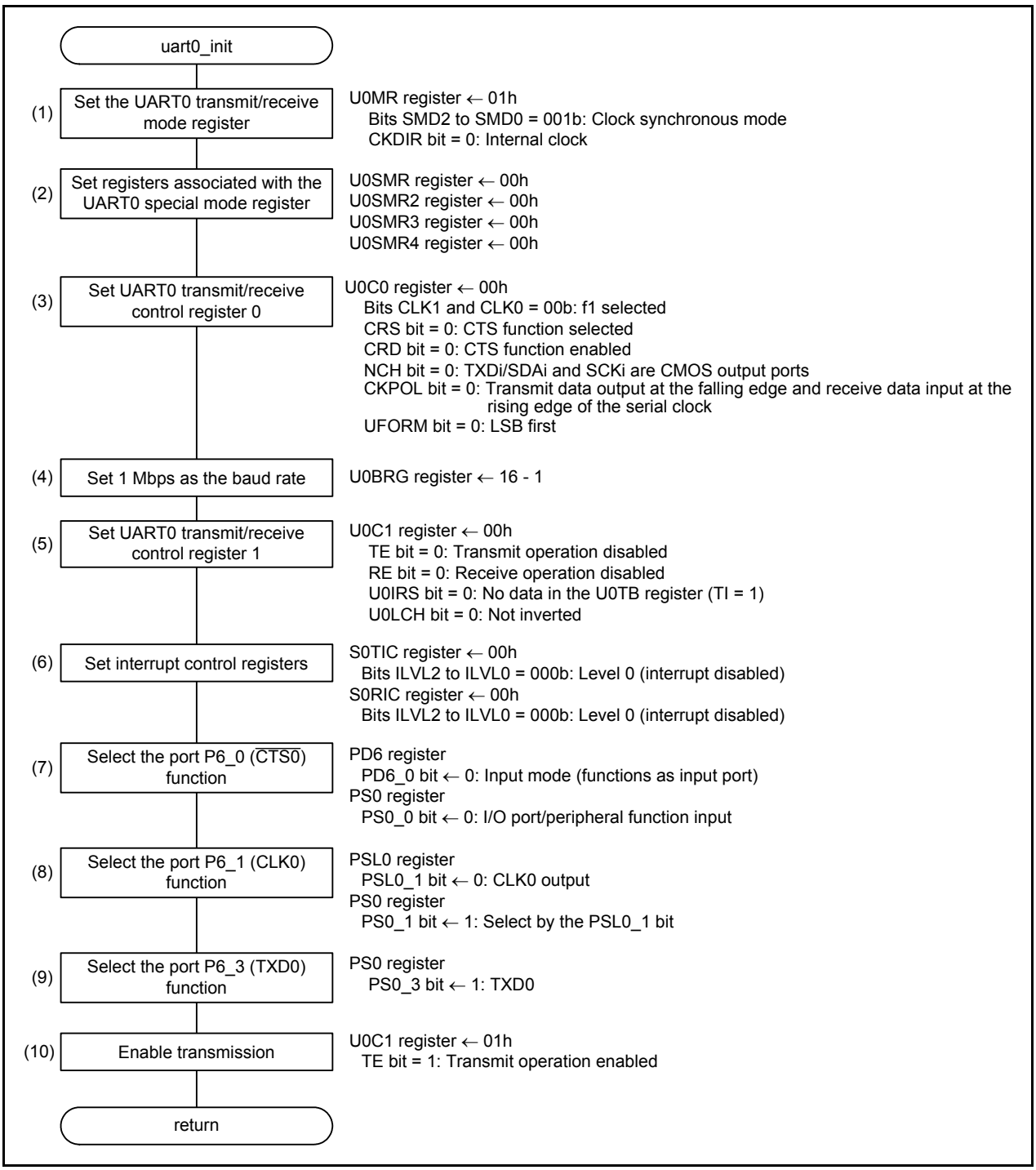


Figure 5.3 UART0 Initial Setting

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M32C/84 Group (M32C/84, M32C/84T) User's Manual: Hardware Rev.1.01
M32C/85 Group (M32C/85, M32C/85T) User's Manual: Hardware Rev.1.03
M32C/87 Group (M32C/87, M32C/87A, M32C/87B) User's Manual: Hardware Rev.1.51
M32C/88 Group (M32C/88T) User's Manual: Hardware Rev.1.10
M32C/8A Group User's Manual: Hardware Rev.1.01
M32C/8B Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M32C Series C Compiler Package V.5.42
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	M32C/84, 85, 87, 88, 8A and 8B Groups Data Transmission Using the Serial Interface in Clock Synchronous Mode

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 29, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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