M16C/5LD, 5L, 5M, 6C Groups

Outputting a 16-Bit PWM Waveform Using Timer S in Set/Reset Waveform Output Mode

R01AN0393EJ0101
Rev. 1.01
June 30, 2011

Abstract

This document describes a method for outputting a 16-bit PWM waveform using timer S in set/reset waveform output mode with the M16C/5LD, 5L, 5M, and 6C Group microcomputers (MCUs).

Products

MCUs: M16C/5LD, 5L, 5M, 6C Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Introduction

Timer S has an input capture/output compare function (IC/OC). The input capture (IC) is used for time measurement and the output compare (OC) is used for waveform generation. The IC/OC has one 16-bit free-running base timer and eight channels for timer measurement and waveform generation.

1.1 Waveform Generation Function

Waveforms are generated based on the values of the base timer and the G1POj register (j = 0 to 7). Table 1.1 lists the Waveform Generation Function Settings. Items marked with a check mark (✓) are described in this chapter.

Table 1.1 Waveform Generation Function Settings

Item		Setting
Waveform generation function		Single-phase waveform output mode
		Inverted waveform output mode
	✓	Set/reset waveform output mode (SR waveform output mode)
Base timer reset source	✓	Base timer is reset when the base timer and G1BTRR register values match
		Base timer is reset when the base timer and G1PO0 register values match
		Base timer is reset when the input level to the $\overline{\text{INT1}}$ pin is low
Initial output level selection	✓	Output low as default level
		Output high as default level
Output level inversion selection	✓	Output level not inverted
		Output level inverted
Channels	✓	Channel 0
		Channel 1
	✓	Channel 2
		Channel 3
	✓	Channel 4
		Channel 5
	✓	Channel 6
		Channel 7
Interrupts	✓	IC/OC base timer interrupt
		IC/OC interrupt 0
		IC/OC interrupt 1
		IC/OC channel 0 interrupt
		IC/OC channel 1 interrupt
		IC/OC channel 2 interrupt
		IC/OC channel 3 interrupt

1.2 SR Waveform Output Mode

When the base timer and G1POj register values match, if the INV bit in the G1POCRj register is 0 (output level not inverted), the output level from the OUTC1_j pin becomes high (j = 0, 2, 4, 6). When the base timer matches the G1POk register, the OUTC1_j pin outputs low (k = j + 1). When using SR waveform output mode, set the base timer to increment mode.

In SR waveform output mode, not only can the PWM period and duty variable, but the duty start position (set width) and end position (reset width) are user discretionary.

The following is an explanation for setting the PWM period using the G1BTRR register, setting the set width using the G1POj register, and setting the reset width using the G1POk register (j = 0, 2, 4, 6; k = j + 1). PWM waveforms are output from the OUTC1_j pin corresponding to channel j. fBT1 is the operating clock for the base timer.

(1) PWM period setting

The base timer is reset when the base timer and G1BTRR register values match. If the G1BTRR register setting value is p, the PWM period is as follows:

PWM period: $\frac{p + 2}{fBT1}$

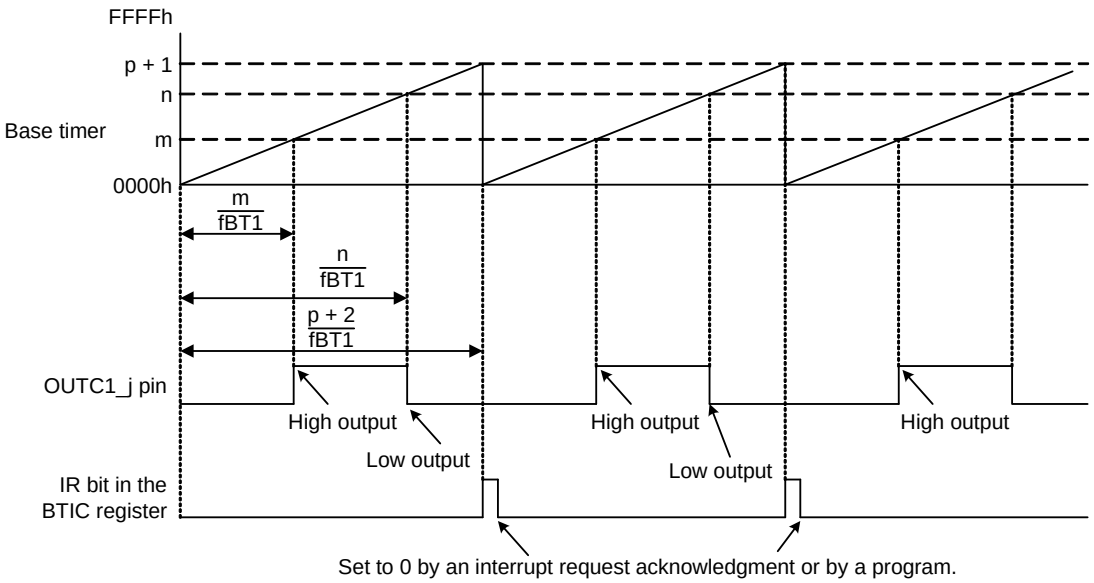
When changing the period, change the G1BT register in the interrupt handling without changing the G1BTRR register, or set the BTS bit in the G1BCR1 register to 0 before changing the G1BTRR register.

(2) Set width and reset width setting

Set channel j to SR waveform output mode in the waveform generation function. If the G1POj register setting value is m, and the G1POk register setting value is n, the set width and reset width are as follows:

Set width: $\frac{m}{fBT1}$; reset width: $\frac{n}{fBT1}$

Figure 1.1 shows the operation of SR waveform output mode when the base timer is reset by the base timer and G1BTRR register values matching.



j = 0 to 7; k = j + 1
m: G1POj register setting value
n: G1POk register setting value
p: G1BTRR register setting value

The above diagram assumes the following:
- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{INT1}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- The IVL bit in the G1POCRj register is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 1.1 SR Waveform Output Mode Operation

2. Software

2.1 Operation Overview

The OUTC1_k (P2_k) pin is used by timer S and outputs a PWM waveform (k = 0, 2, 4, 6). Every five times a base timer interrupt is generated, the G1POi register is rewritten in the base timer interrupt handler, and the set width and reset width are changed (i = 0 to 7).

Clock statistics are as follows:

- Main clock: 20 MHz
- Base timer operating clock (fBT1): 1 MHz

Figure 2.1 shows the Pin Output, and Table 2.1 lists the Set Width and Reset Width Setting Values.

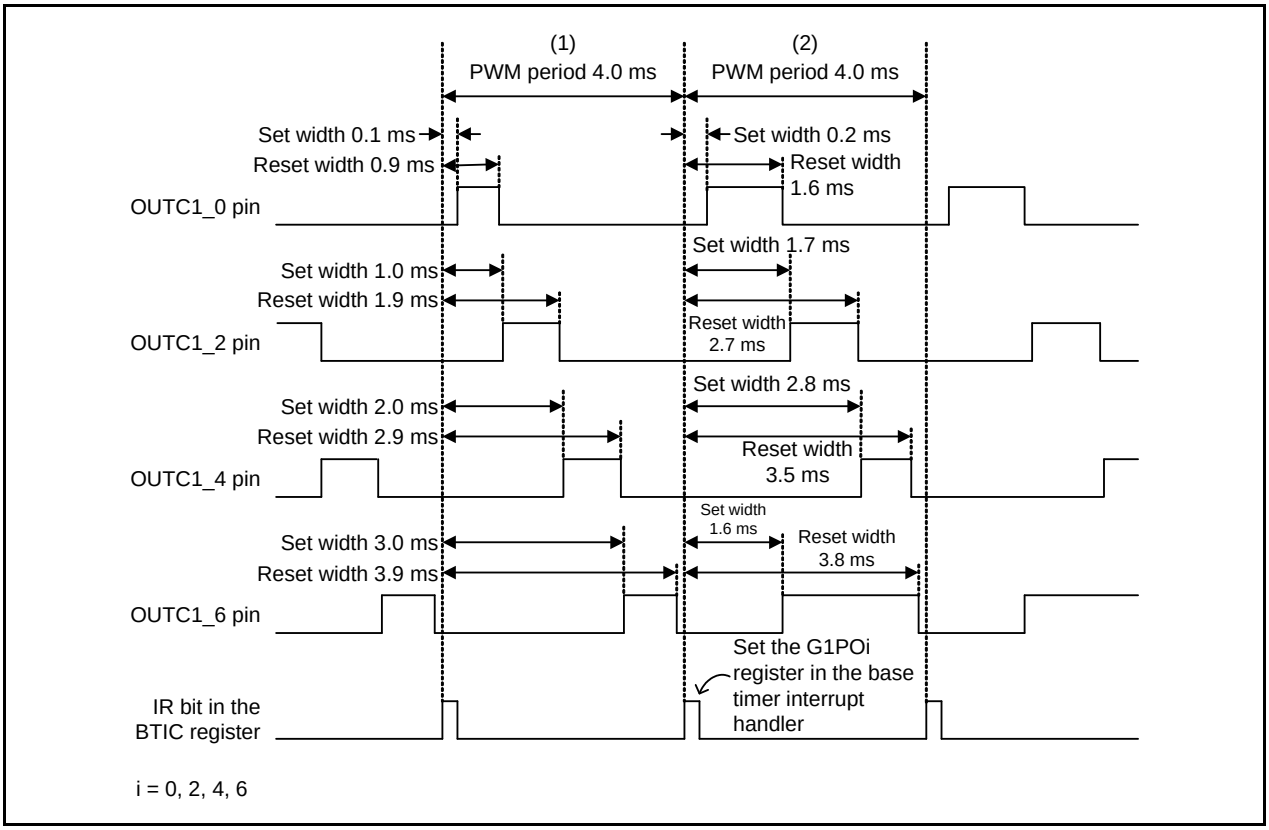


Figure 2.1 Pin Output

Table 2.1 Set Width and Reset Width Setting Values

Output Pin	Width	Register	(1)	(2)
OUTC1_0 (P2_0)	Set width: $\frac{m}{fBT1}$	G1PO0	0.1 ms (m = 100)	0.2 ms (m = 200)
	Reset width: $\frac{n}{fBT1}$	G1PO1	0.9 ms (n = 900)	1.6 ms (n = 1600)
OUTC1_2 (P2_2)	Set width: $\frac{m}{fBT1}$	G1PO2	1.0 ms (m = 1000)	1.7 ms (m = 1700)
	Reset width: $\frac{n}{fBT1}$	G1PO3	1.9 ms (n = 1900)	2.7 ms (n = 2700)
OUTC1_4 (P2_4)	Set width: $\frac{m}{fBT1}$	G1PO4	2.0 ms (m = 2000)	2.8 ms (m = 2800)
	Reset width: $\frac{n}{fBT1}$	G1PO5	2.9 ms (n = 2900)	3.5 ms (n = 3500)
OUTC1_6 (P2_6)	Set width: $\frac{m}{fBT1}$	G1PO6	3.0 ms (m = 3000)	1.6 ms (m = 1600)
	Reset width: $\frac{n}{fBT1}$	G1PO7	3.9 ms (n = 3900)	3.8 ms (n = 3800)

2.2 Flowcharts

2.2.1 Main Processing

Figure 2.2 shows the Main Processing.

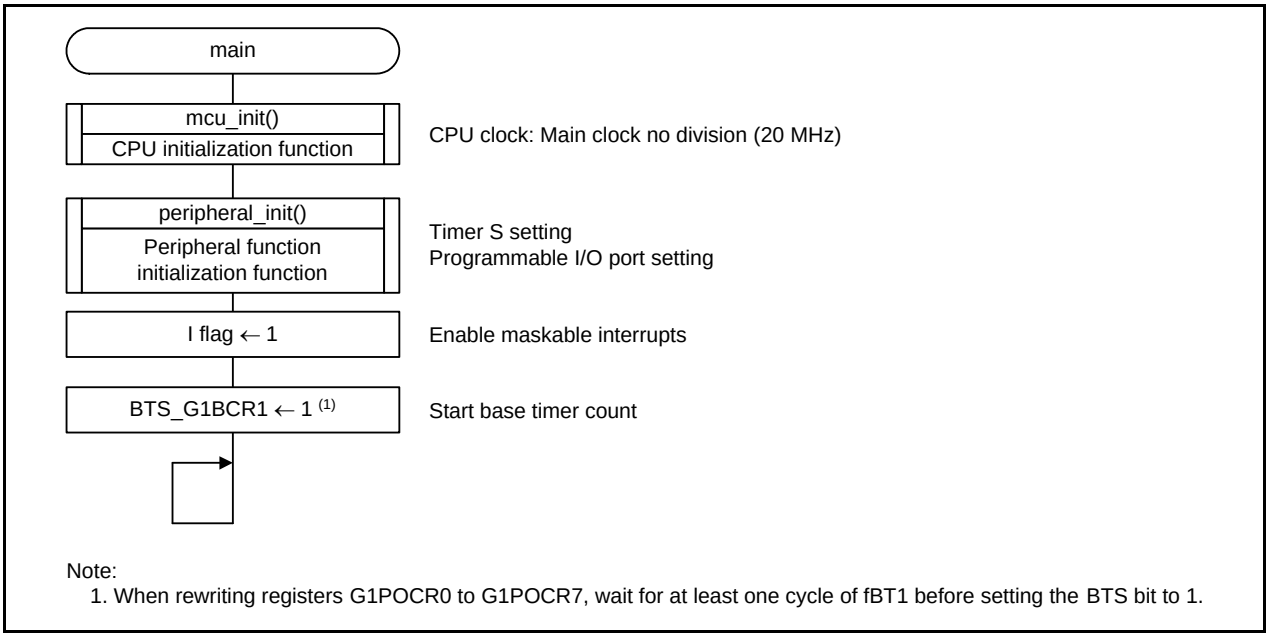
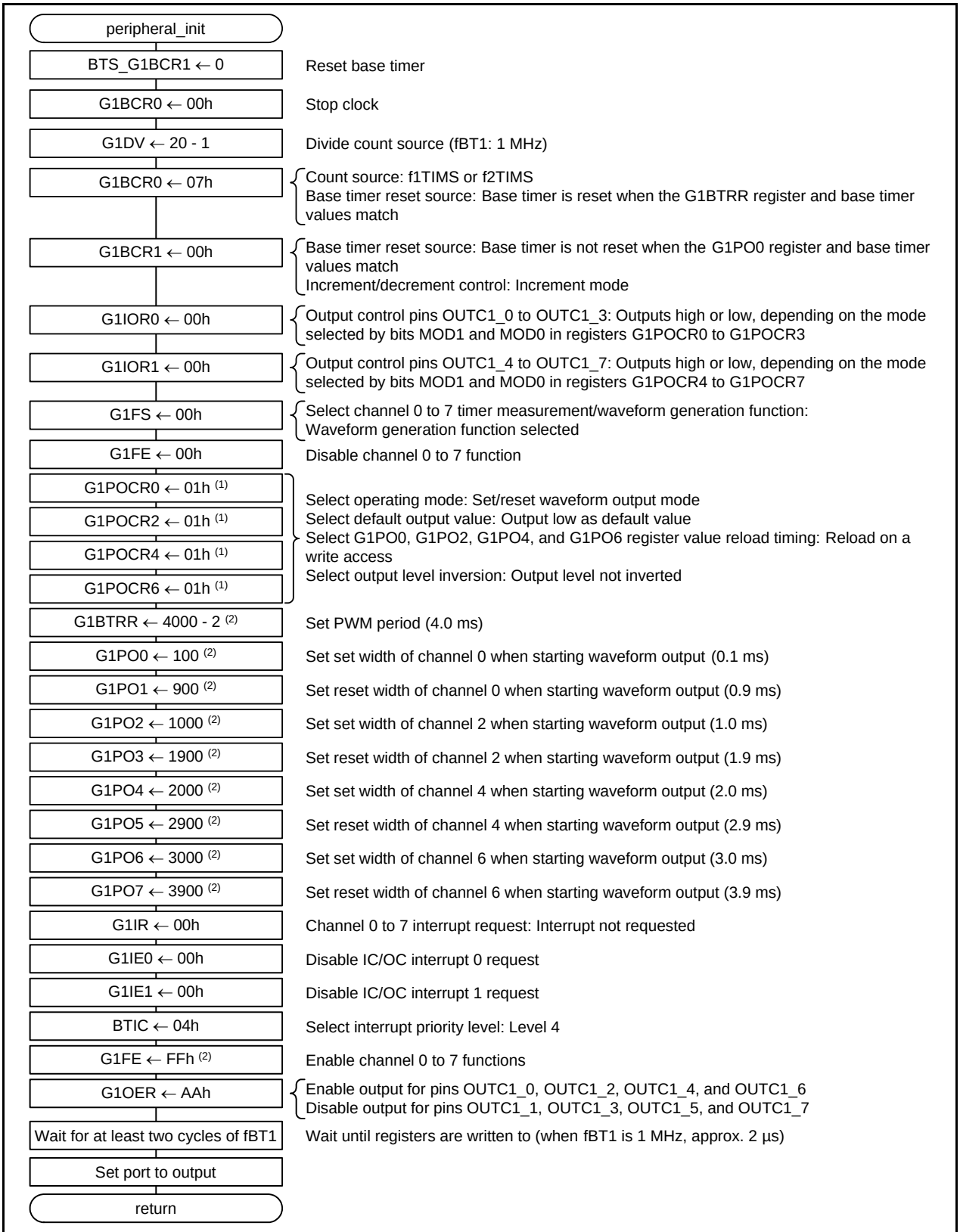


Figure 2.2 Main Processing

2.2.2 Peripheral Function Initialization Function

Figure 2.3 shows the Peripheral Function Initialization Function.



Notes:
1. When rewriting this register, after waiting for at least one cycle of fBT1, set the BTS bit to 1.
2. The values written to these registers are simultaneously reflected to the base timer count source (fBT1).

Figure 2.3 Peripheral Function Initialization Function

2.2.3 Base Timer Interrupt Handling Function

Figure 2.4 shows the Base Timer Interrupt Handling Function.

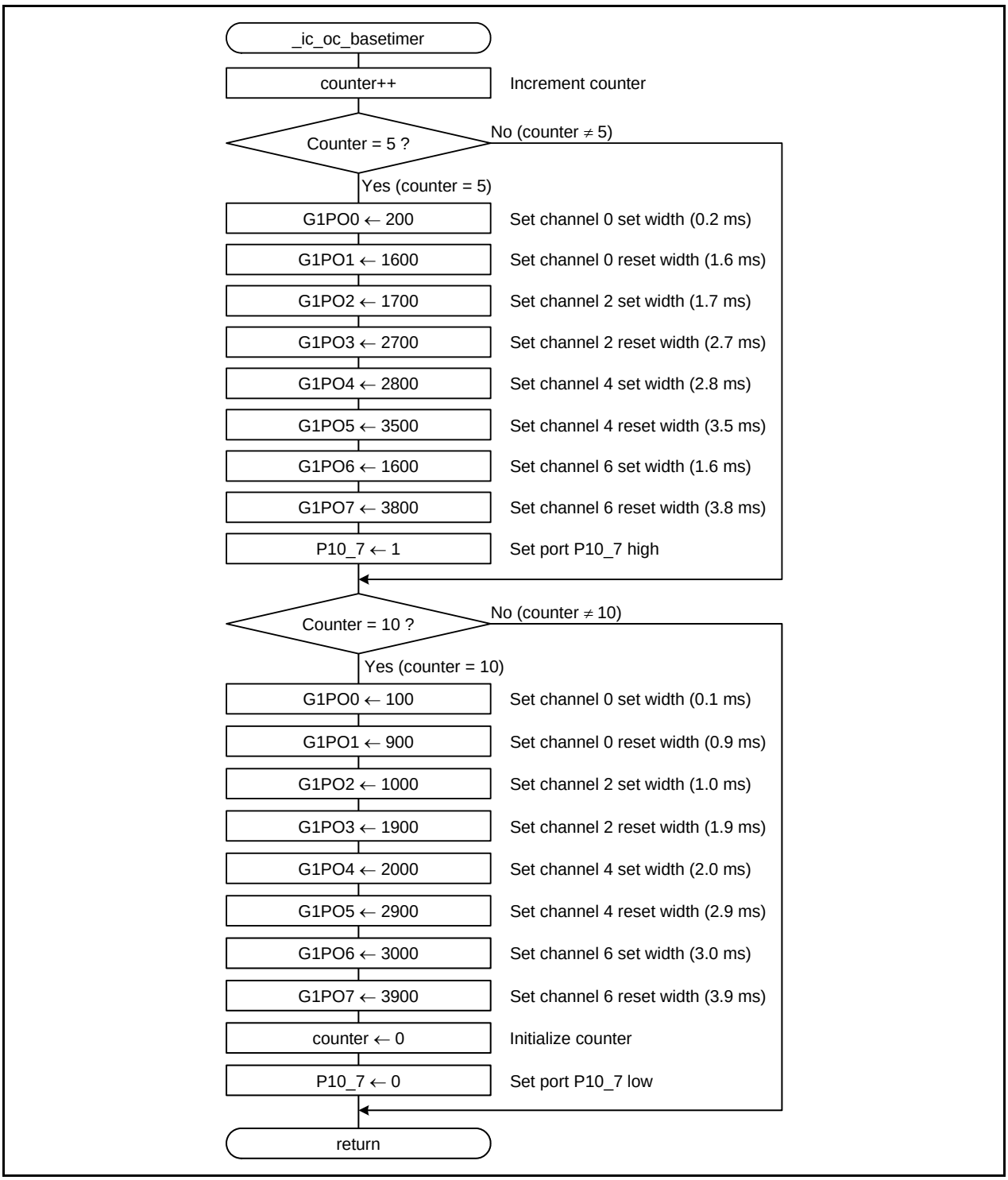


Figure 2.4 Base Timer Interrupt Handling Function

3. Application Example

3.1 Changing the Period

The PWM output period can be set using the G1BTRR register when the RST4 bit in the G1BCR0 register is 1, or it can be set using the G1PO0 register when the RST1 bit in the G1BCR1 register is 1. When changing the period during a count operation, after setting the BTS bit in the G1BCR1 register to 0 (base timer reset), wait at least one cycle of fBT1, and rewrite the G1BTRR or G1PO0 register. The procedure is as follows:

(1) Set the BTS bit to 0. (1)
(2) Wait at least one cycle of fBT1.
(3) Rewrite the register where the period was set.
(4) Set the BTS bit to 1.

Note:
1. One cycle of fBT1 passes between setting the BTS bit to 0 and the count stopping.

When changing the period in SR waveform output mode, the output waveform changes using the timing in the following:

[1] Before the base timer and G1POj register values match (j = 0, 2, 4, 6)
[2] After the base timer and G1POj register values match, or before the base timer and G1POk register values match (j = 1, 3, 5, 7)
[3] After the base timer and G1POk register values match, or before the base timer and G1BTRR register values match

Figure 3.1 shows Timing Diagram for Period Change When Using SR Waveform Output Mode. Figure 3.2 shows Output When Changing the Period Before the Base Timer and G1POj Register Values Match. Figure 3.3 shows Output When Changing the Period After the Base Timer and G1POj Register Values Match and Before the Base Timer and G1POk Register Values Match. Figure 3.4 shows Output When Changing the Period After the Base Timer and G1POk Register Values Match and Before the Base Timer and G1BTRR Register Values Match.

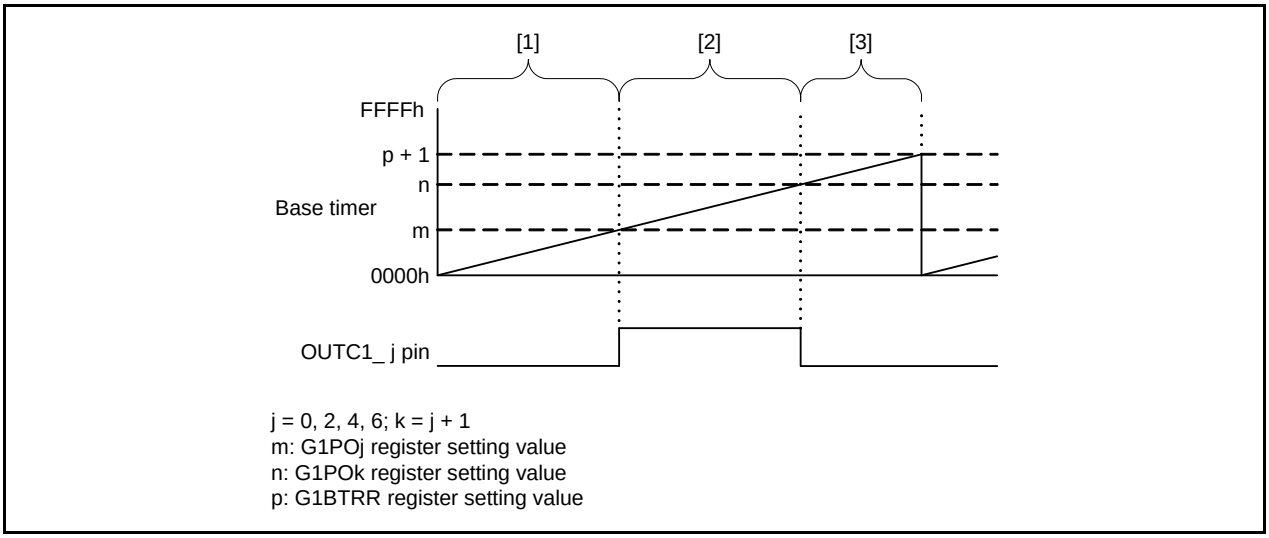
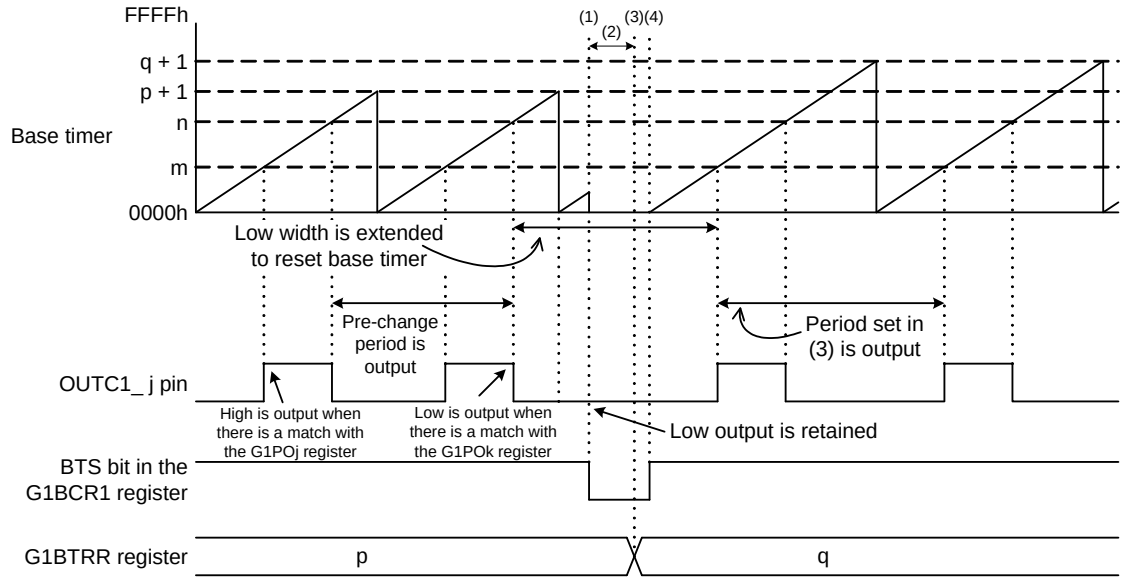


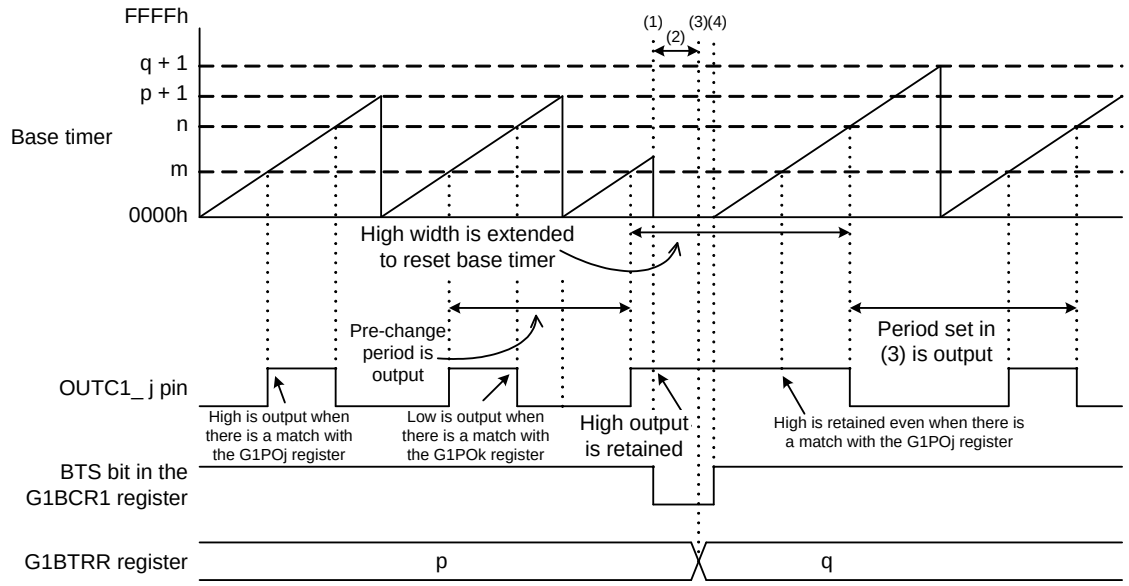
Figure 3.1 Timing Diagram for Period Change When Using SR Waveform Output Mode



j = 0, 2, 4, 6; k = j + 1
m: G1POj register setting value
n: G1POk register setting value
p, q: G1BTRR register setting values

The above diagram assumes the following:
- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{INT1}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- Bits MOD1 and MOD0 in the G1POCRj register are 01b (SR waveform output mode), the IVL bit is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

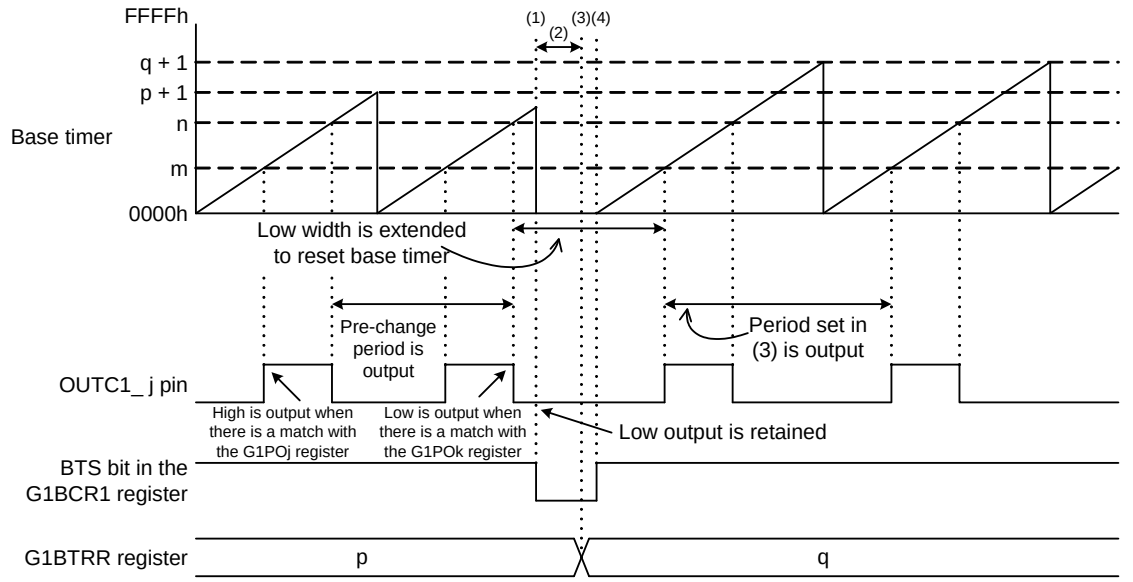
Figure 3.2 Output When Changing the Period Before the Base Timer and G1POj Register Values Match



j = 0, 2, 4, 6; k = j + 1
m: G1POj register setting value
n: G1POk register setting value
p, q: G1BTRR register setting values

The above diagram assumes the following:
- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{\text{INT1}}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- Bits MOD1 and MOD0 in the G1POCRj register are 01b (SR waveform output mode), the IVL bit is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 3.3 Output When Changing the Period After the Base Timer and G1POj Register Values Match and Before the Base Timer and G1POk Register Values Match



j = 0, 2, 4, 6; k = j + 1
m: G1POj register setting value
n: G1POk register setting value
p, q: G1BTRR register setting values

The above diagram assumes the following:
- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{\text{INT1}}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- Bits MOD1 and MOD0 in the G1POCRj register are 01b (SR waveform output mode), the IVL bit is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 3.4 Output When Changing the Period After the Base Timer and G1POk Register Values Match and Before the Base Timer and G1BTRR Register Values Match

4. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

5. Reference Documents

M16C/5LD, M16C/56D Group User's Manual: Hardware Rev.1.10
M16C/5L, M16C/56 Group User's Manual: Hardware Rev.1.00
M16C/5M, M16C/57 Group User's Manual: Hardware Rev.1.01
M16C/6C Group User's Manual: Hardware Rev.2.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
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Revision History	M16C/5LD, 5L, 5M, 6C Groups Outputting a 16-Bit PWM Waveform Using Timer S in Set/Reset Waveform Output Mode

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2010	—	First edition issued
1.01	June 30, 2011	—	Added chapter 3

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   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
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