M16C/6C Group
Using the Voltage Detector

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1. Abstract

This document describes an application example for using the voltage detector. The sample code shows how to detect the rise or fall of VCC1 input voltage using the voltage detector.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

- MCU: M16C/6C Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

The sample code operates under following conditions.

- XIN frequency: 8 MHz
- Message transmission
  Channel: UART1

- Communication settings
  - Baud rate: 38400 bps
  - Data length: 8 bits
  - Parity: None
  - Stop bit: 1 bit
  - Flow control: None

Depending on the MCU used, the surrounding temperature, and other variables, characteristics for the voltage detector such as the detection voltage and detection time will vary within the range listed in the Electrical Characteristics chapter of the User's Manual: Hardware. The settings described in this document are examples used only for reference. The variation in the electrical characteristics should be considered when designing your system. Refer to the User’s Manual: Hardware for details on electrical characteristics.

3. Application Example

3.1 Overview

In this sample code, the voltage of VCC1 is checked every 10 ms after the power-on reset. When VCC1 is equal to or above Vdet2 ten times consecutively (i.e. VCC1 ≥ Vdet2 for 100 ms), the program determines that the VCC1 voltage is stable at or above Vdet2.

When VCC1 is equal to or above Vdet2 after the power-on reset.

(1) Configure the voltage monitor interrupt.
(2) Transmit the message “Start” to the personal computer (hereinafter referred to as PC), and perform normal operation.

When VCC1 is equal to or below Vdet2 after the power-on reset.

(1) Invert the alarm port every 1 second. (1)
(2) Transmit the message “Please set 5.0V” to the PC.

When a rise or a fall is detected in the VCC1 voltage, an interrupt occurs. Read the VW2C2 bit in the VW2C register and the VW1C2 bit in the VW1C register in the interrupt handler, then determine whether the source is the voltage monitor 2 interrupt or voltage monitor 1 interrupt. The digital filter is not used here.

(1) Normal operation (when voltage is stable)
Every 0.5 seconds, the count port value is incremented and then output. (1)

(2) Operation when the voltage monitor 2 interrupt occurs

When VCC1 is equal to or below Vdet2 and the voltage monitor 2 interrupt occurs:
• Transmit the message “Under Vdet2” to the PC.
• Change the condition for the voltage monitor 2 interrupt to “VCC1 ≥ Vdet2”.

When VCC1 is equal to or above Vdet2 and the voltage monitor 2 interrupt occurs:
• Transmit the message “Over Vdet2” to the PC.
• Change the condition for the voltage monitor 2 interrupt to “VCC1 ≤ Vdet2”.

(3) Operation when the voltage monitor 1 interrupt occurs

When VCC1 is equal to or below Vdet1 and the voltage monitor 1 interrupt occurs:
• Transmit the message “Under Vdet1” to the PC.
• Change the condition for the voltage monitor 1 interrupt to “VCC1 ≥ Vdet1”.

When VCC1 is equal to or above Vdet1 and the voltage monitor 1 interrupt occurs:
• Transmit the message “Over Vdet1” to the PC.
• Change the condition for the voltage monitor 1 interrupt to “VCC1 ≤ Vdet1”.

(4) Operation when the voltage monitor 0 reset occurs
Reset is executed.

Note:
1. Count ports: P4_0 to P4_2
Alarm port: P4_3

3.2 Circuit Example

Figure 3.1 shows the Power-On Reset Circuit.

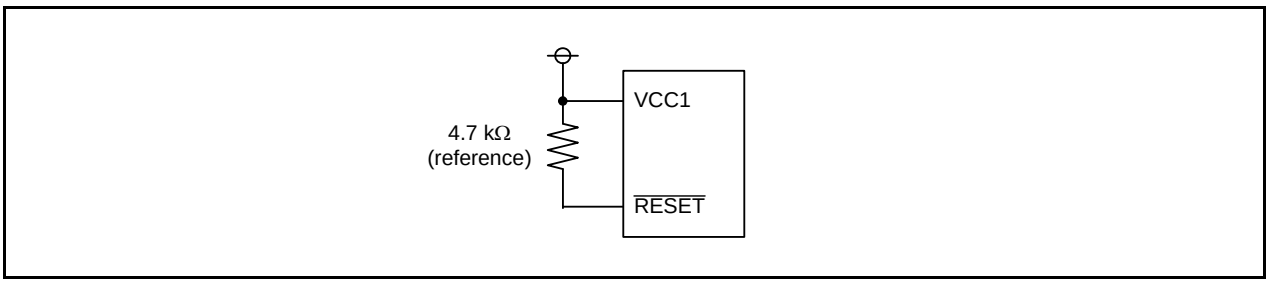


Figure 3.1 Power-On Reset Circuit

3.3 Operation

Table 3.1 lists the operations when the voltage transitions as shown in Figure 3.2.

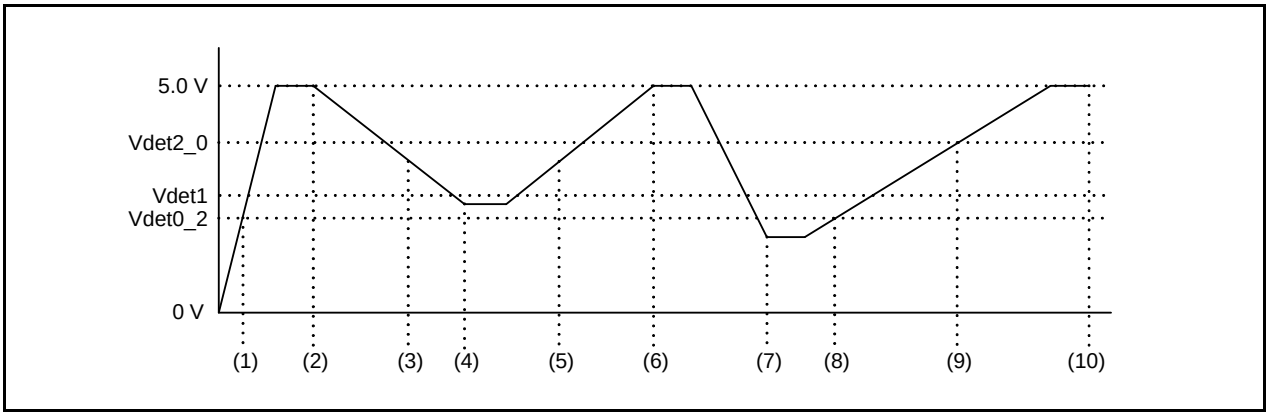


Figure 3.2 Voltage Transition

Table 3.1 Operations for (1) to (10) in Figure 3.2

	Operation	Condition
(1)	Power-on reset	When VCC1 is equal to or above Vdet0.
(2)	Start incrementing the count port. Transmit the message “Start” to the PC.	VCC1 is equal to or above Vdet2 for 100 ms.
(3)	Transmit the message “Under Vdet2” to the PC. Change the VW2C7 bit to 0 (when VCC1 is equal to or above Vdet2).	VCC1 passed downward through Vdet2.
(4)	Transmit the message “Under Vdet1” to the PC. Change the VW1C7 bit to 0 (when VCC1 is equal to or above Vdet1).	VCC1 passed downward through Vdet1.
(5)	Transmit the message “Over Vdet1” to the PC. Change the VW1C7 bit to 1 (when VCC1 is equal to or below Vdet1).	VCC1 passed upward through Vdet1.
(6)	Transmit the message “Over Vdet2” to the PC. Change the VW2C7 bit to 1 (when VCC1 is equal to or below Vdet2).	VCC1 passed upward through Vdet2.
(7)	Voltage monitor 0 reset	VCC1 is below Vdet0.
(8), (9)	Invert the alarm port in 1 second intervals and transmit the message “Please set 5.0V” to the PC.	VCC1 is equal to or above Vdet0, and below Vdet2.
(10)	Start incrementing a count port. Transmit the message “Start” to the PC.	VCC1 is equal to or above Vdet2 for 100 ms.

3.4 Determining When VCC1 ≥ Vdet2

Figure 3.3 shows how to read the VC13 bit in the VCR1 register to determine whether VCC1 is equal to or above Vdet2.

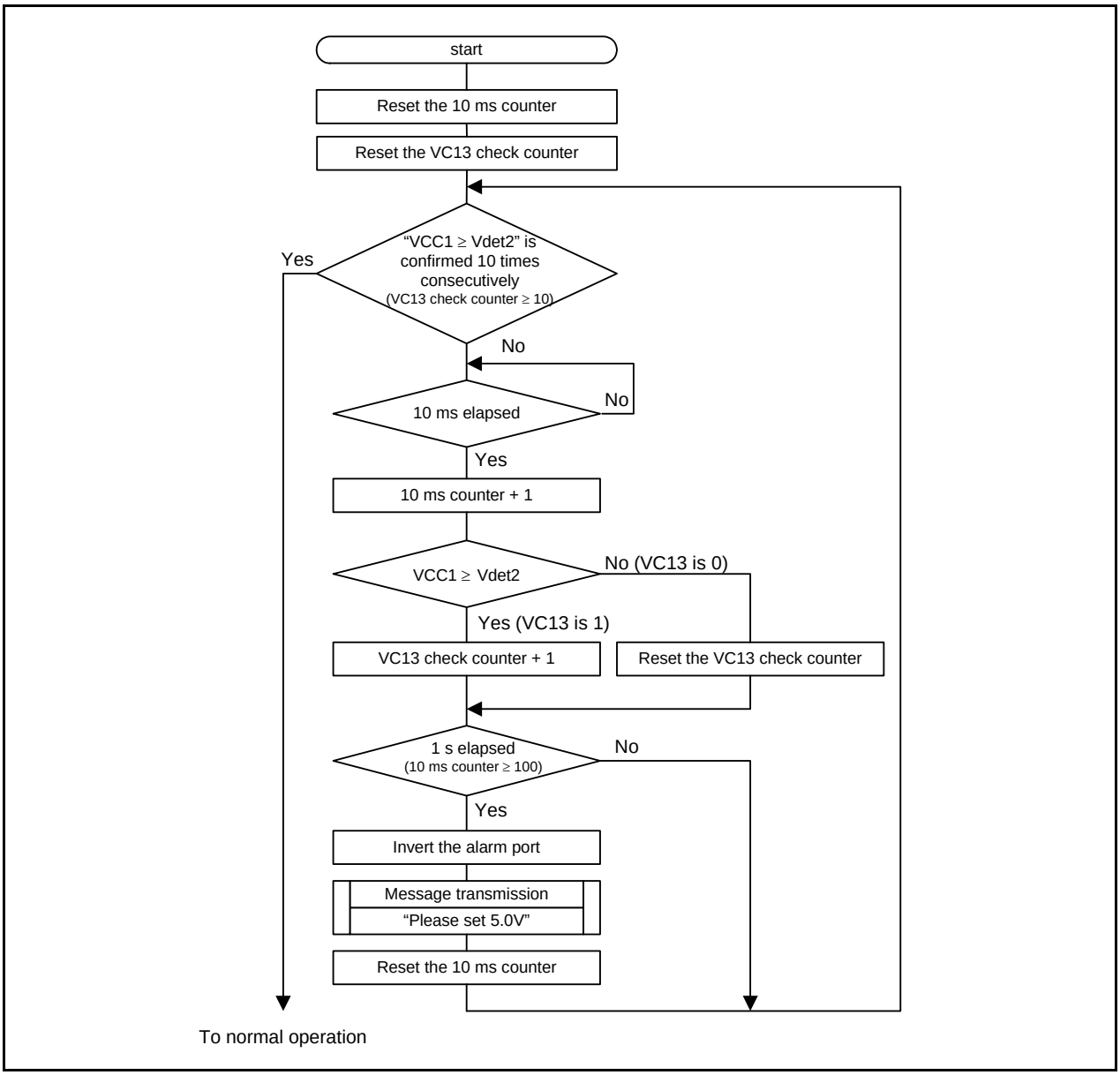


Figure 3.3 Determining When VCC1 ≥ Vdet2

3.5 Determining the Voltage Monitor Interrupt Source

Read the voltage change detection flag in the interrupt handler to determine whether the source is the voltage monitor 1 interrupt or voltage monitor 2 interrupt. Chattering check is not performed here. Figure 3.4 shows a flowchart for determining the voltage monitor interrupt source.

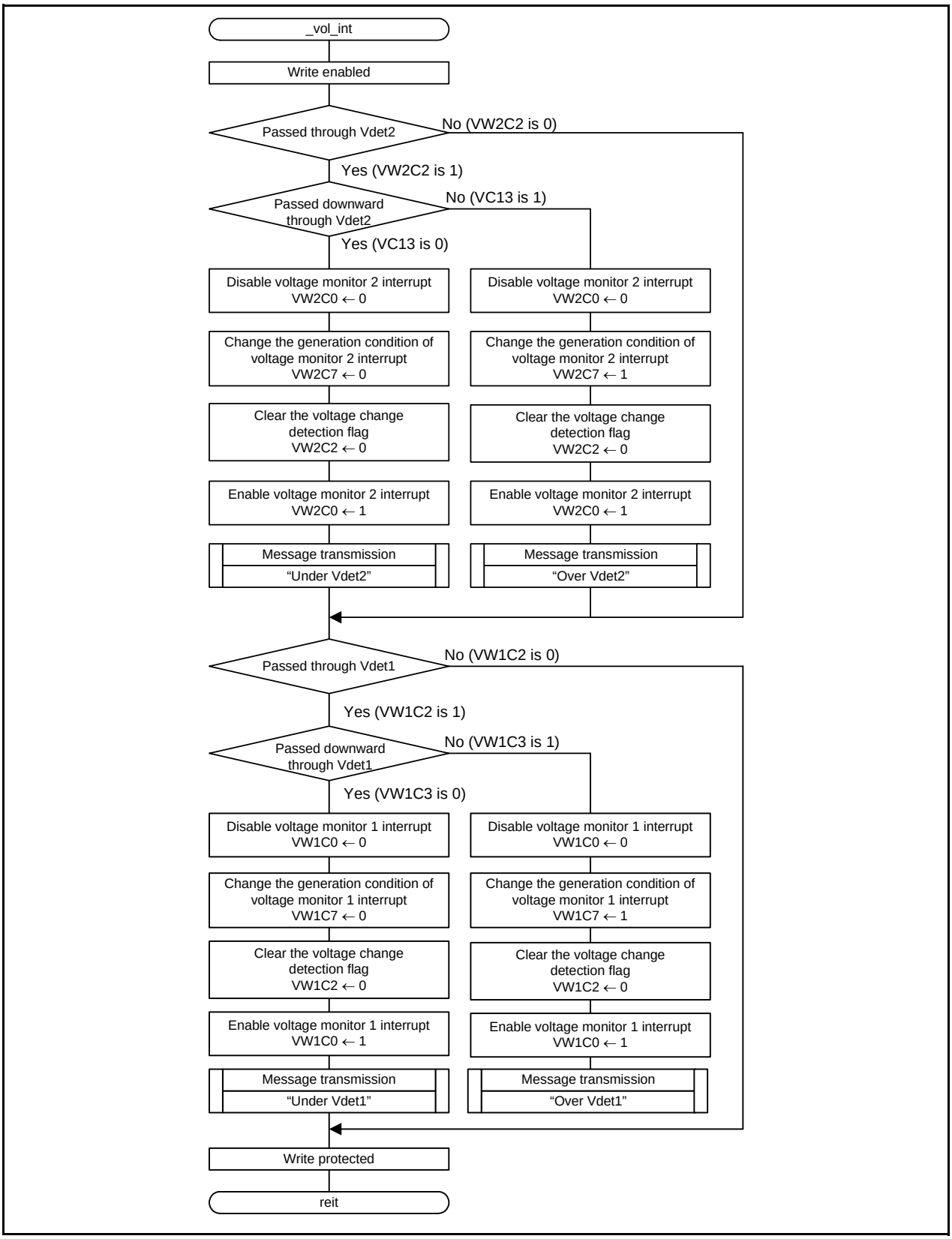


Figure 3.4 Determining the Voltage Monitor Interrupt Source

4. Setting Procedures

4.1 Setting Optional Function Select Address 1 (OFS1)

Enabling and disabling the voltage monitor 0 reset after hardware reset can be selected by setting the LVDAS bit in the OFS1 address. In this sample code, the voltage monitor 0 reset is enabled after hardware reset.

The OFS1 address is assigned to address FFFFFh in the M16C/6C Group.
Refer to User's Manual: Hardware for the OFS1 address setting values.
Table 4.1 shows script examples for enabling the voltage monitor 0 reset after hardware reset in the M16C/6C Group.

Table 4.1 Script Examples for the OFS1 Address

Tool	Description
Script in C language	_asm(".ofsreg 09Fh");
Script in assembly language	.ofsreg 09Fh

4.2 Procedure for Setting Voltage Monitor Related Bits

Table 4.2 shows Procedure for Setting Voltage Monitor 0 Reset Related Bits. Table 4.3 shows Procedure for Setting Voltage Monitor 1 Interrupt/Reset Related Bits. Table 4.4 shows Procedure for Setting Voltage Monitor 2 Interrupt/Reset Related Bits.

Table 4.2 Procedure for Setting Voltage Monitor 0 Reset Related Bits

Step	Processing
1	Set the VC25 bit in the VCR2 register to 1 (voltage detector 0 enabled).
2	Wait for td(E-A).
3	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).

Table 4.3 Procedure for Setting Voltage Monitor 1 Interrupt/Reset Related Bits

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage monitor 1 interrupt	Voltage monitor 1 reset	Voltage monitor 1 interrupt	Voltage monitor 1 reset
1	Set the VW12E bit in the VWCE register to 1 (voltage monitors 1 and 2 enabled).			
2	Set the VC26 bit in the VCR2 register to 1 (voltage detector 1 enabled).			
3	Wait for td(E-A).			
4	Use bits VW1F1 and VW1F0 in the VW1C register to select the digital filter sampling clock.		Use the VW1C7 bit in the VW1C register to select the timing of the interrupt and reset request. (1)	
5 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).		Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).	
6 (2)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset).	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset).
7	Set the VW1C2 bit in the VW1C register to 0 (Vdet1 passage not detected).			
8	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		-	
9	Wait for digital filter sampling clock × 3 cycles.		- (no wait time)	
10	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt/reset enabled).			

Notes:

1. Set the VW1C7 bit to 1 for the voltage monitor 1 reset (when VCC1 reaches or goes below Vdet1).
2. When the VW1C0 bit is 0, steps 4, 5, and 6 can be executed simultaneously (with one instruction).
3. If the above setting is performed while the voltage monitor 1 interrupt/reset is disabled (VW1C0 bit in the VW1C register is 0, VC26 bit in the VCR2 register is 0), and VCC1 < Vdet1 (or VCC1 > Vdet1) is detected before enabling the voltage monitor 1 interrupt/reset (step 10), an interrupt does not occur. When VCC1 < Vdet1 (or VCC1 > Vdet1) is detected while executing steps 8 to 10, the VW1C2 bit becomes 1.
   When using the detection results from steps 8 to 10, read the VW1C2 bit after step 10. If the bit is 1, execute the process to be performed after detecting VCC1 < Vdet1 (or VCC1 > Vdet1).
   When ignoring the detection results from steps 8 to 10, set the VW1C2 bit to 0 after step 10.

Table 4.4 Procedure for Setting Voltage Monitor 2 Interrupt/Reset Related Bits

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage monitor 2 interrupt	Voltage monitor 2 reset	Voltage monitor 2 interrupt	Voltage monitor 2 reset
1	Set the VW12E bit in the VWCE register to 1 (voltage monitors 1 and 2 enabled).			
2	Set the VC27 bit in the VCR2 register to 1 (voltage detector 2 enabled).			
3	Wait for td(E-A).			
4	Set bits VW2F0 to VW2F1 in the VW2C register to select the digital filter sampling clock.		Set the VW2C7 bit in the VW2C register to select the timing of the interrupt and reset request. (1)	
5 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).	
6 (2)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset).	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset).
7	Set the VW2C2 bit in the VW2C register to 0 (Vdet2 passage not detected).			
8	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		-	
9	Wait for digital filter sampling clock × 3 cycles.		- (no wait time)	
10	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled).			

Notes:

1. Set the VW2C7 bit to 1 for the voltage monitor 2 reset (when VCC1 reaches or goes below Vdet2).
2. When the VW2C0 bit is 0, steps 4, 5, and 6 can be executed simultaneously (with one instruction).
3. If the above settings are performed while the voltage monitor 2 interrupt/reset is disabled (VW2C0 bit in the VW2C register is 0, VC27 bit in the VCR2 register is 0), and VCC1 < Vdet2 (or VCC1 > Vdet2) is detected before enabling the voltage monitor 2 interrupt/reset (step 10), an interrupt is not generated. When VCC1 < Vdet2 (or VCC1 > Vdet2) is detected while executing steps 8 to 10, the VW2C2 bit becomes 1.
   When using the detection results from steps 8 to 10, read the VW2C2 bit after step 10. If the bit is 1, execute the process to be performed after detecting VCC1 < Vdet2 (or VCC1 > Vdet2).
   When ignoring the detection results from steps 8 to 10, set the VW2C2 bit to 0 after step 10.

5. Setting Method

The setting procedures and values in this chapter are used to achieve the example described in 3. “Application Example”. Refer to the User’s Manual: Hardware for details on registers.

5.1 Setting Optional Function Select Address 1 (OFS1)

Figure 5.1 shows Setting Optional Function Select Address 1 (OFS1).

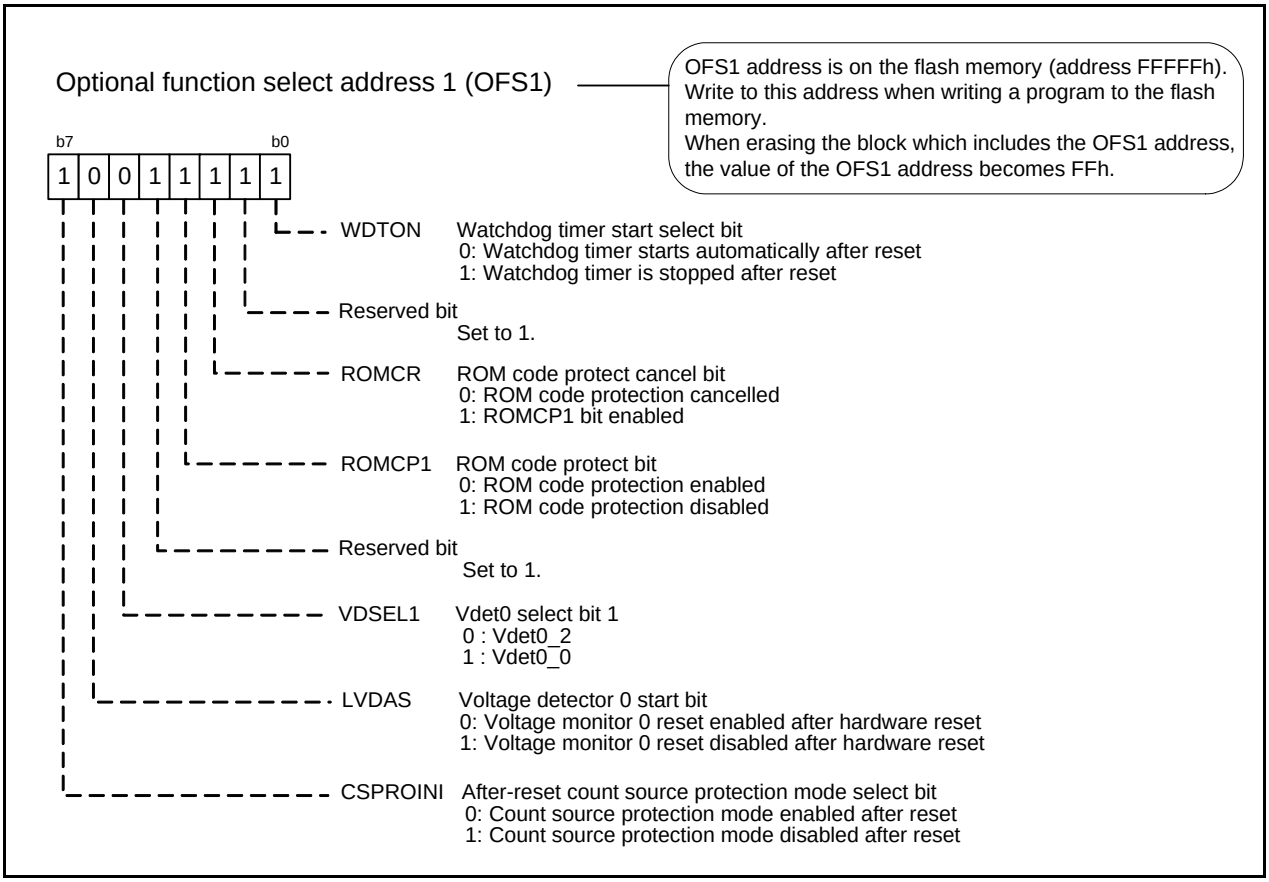


Figure 5.1 Setting Optional Function Select Address 1 (OFS1)

5.2 Setting Registers Associated with Voltage Detectors

Figure 5.2 to Figure 5.5 show register settings associated with voltage detectors.

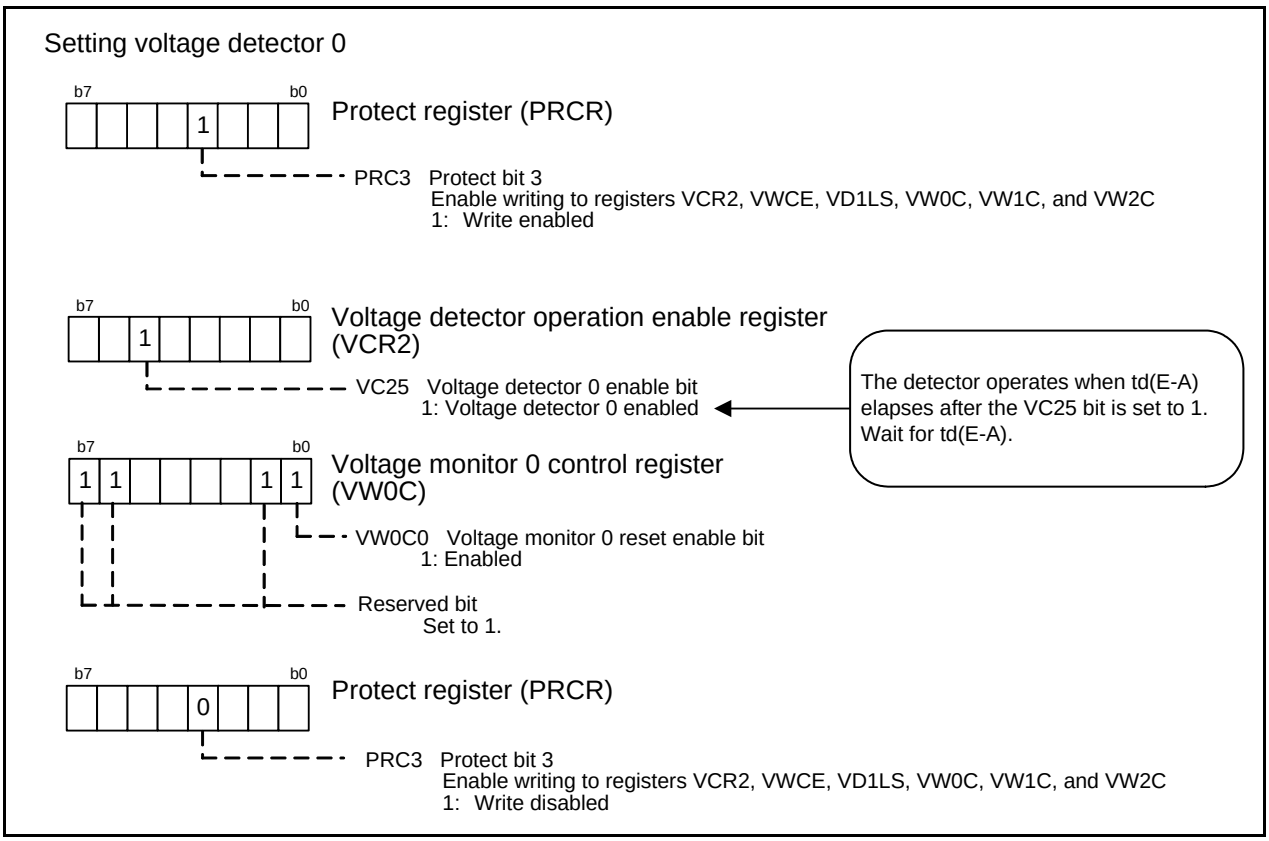


Figure 5.2 Setting Registers Associated with Voltage Monitor 0

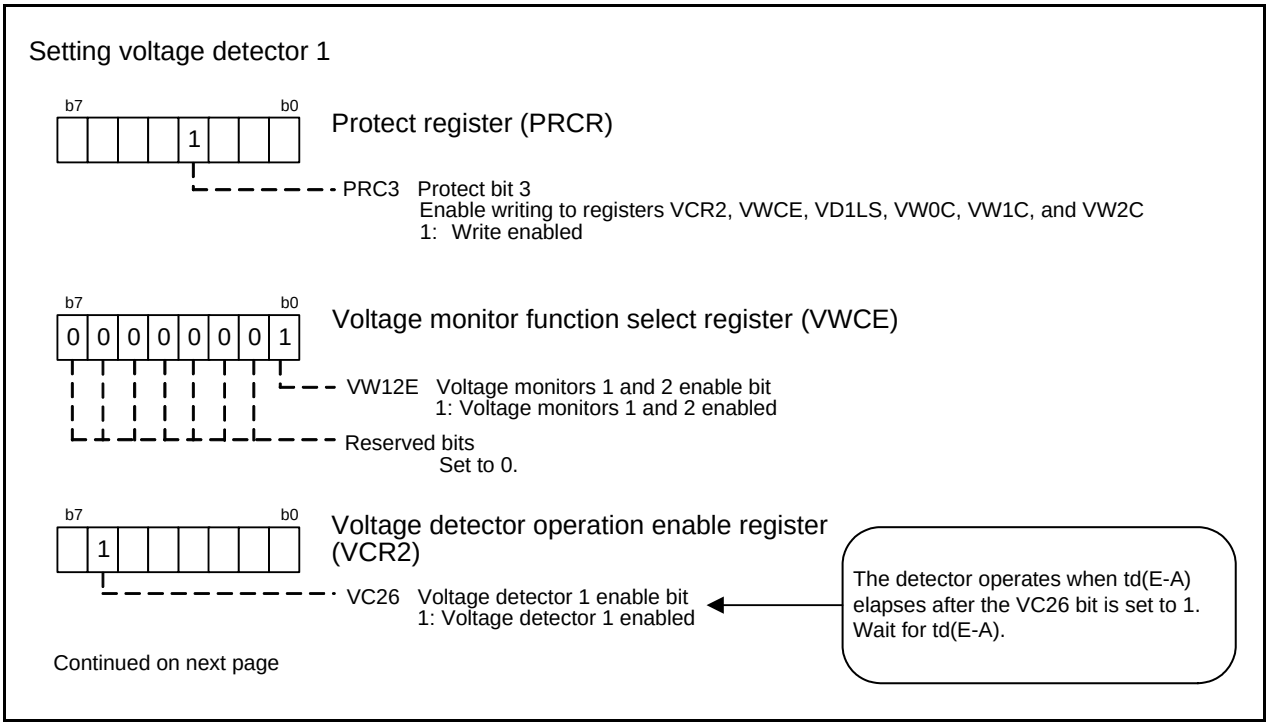


Figure 5.3 Setting Registers Associated with Voltage Monitor 1 (1/2)

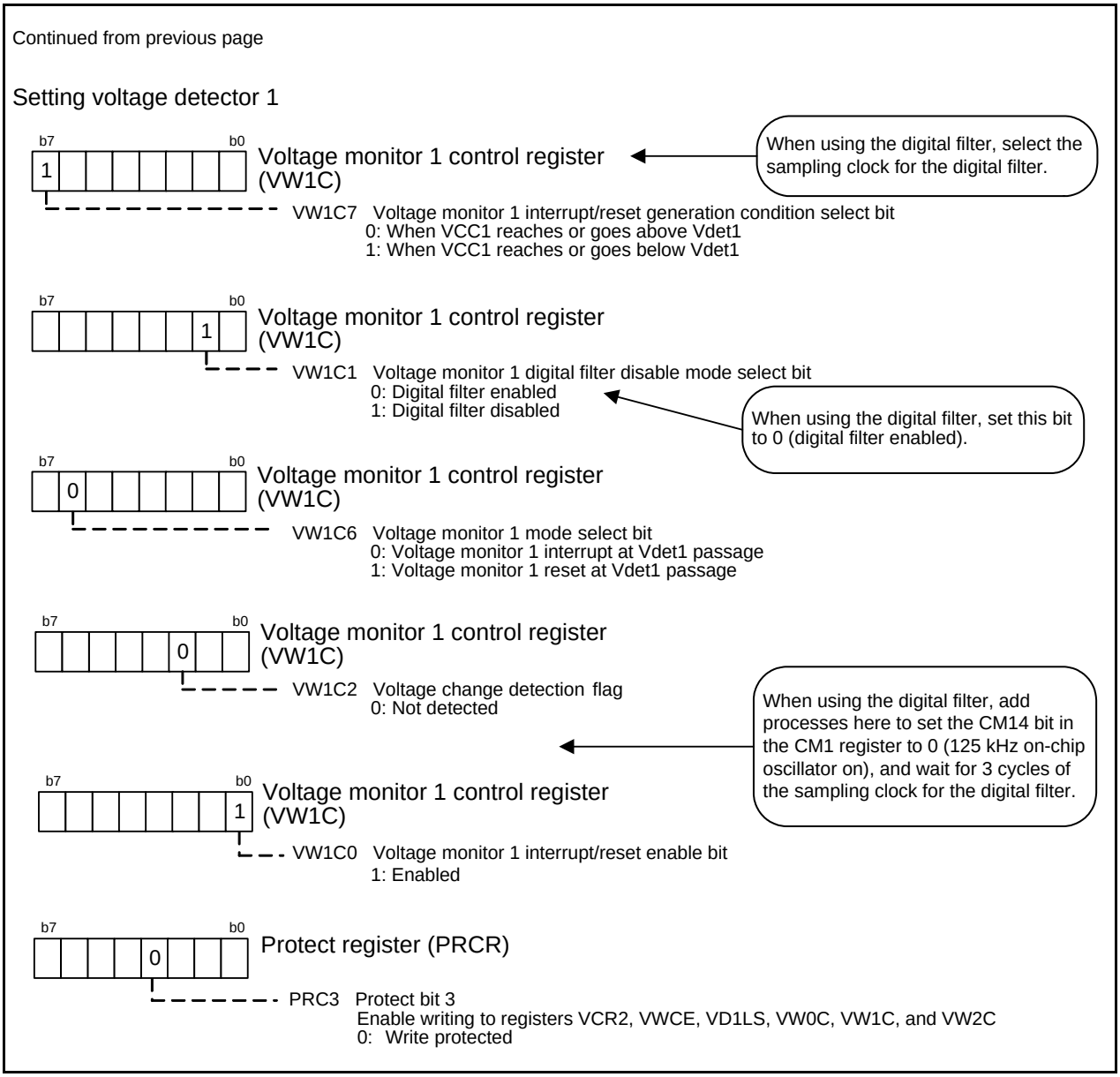


Figure 5.4 Setting Registers Associated with Voltage Monitor 1 (2/2)

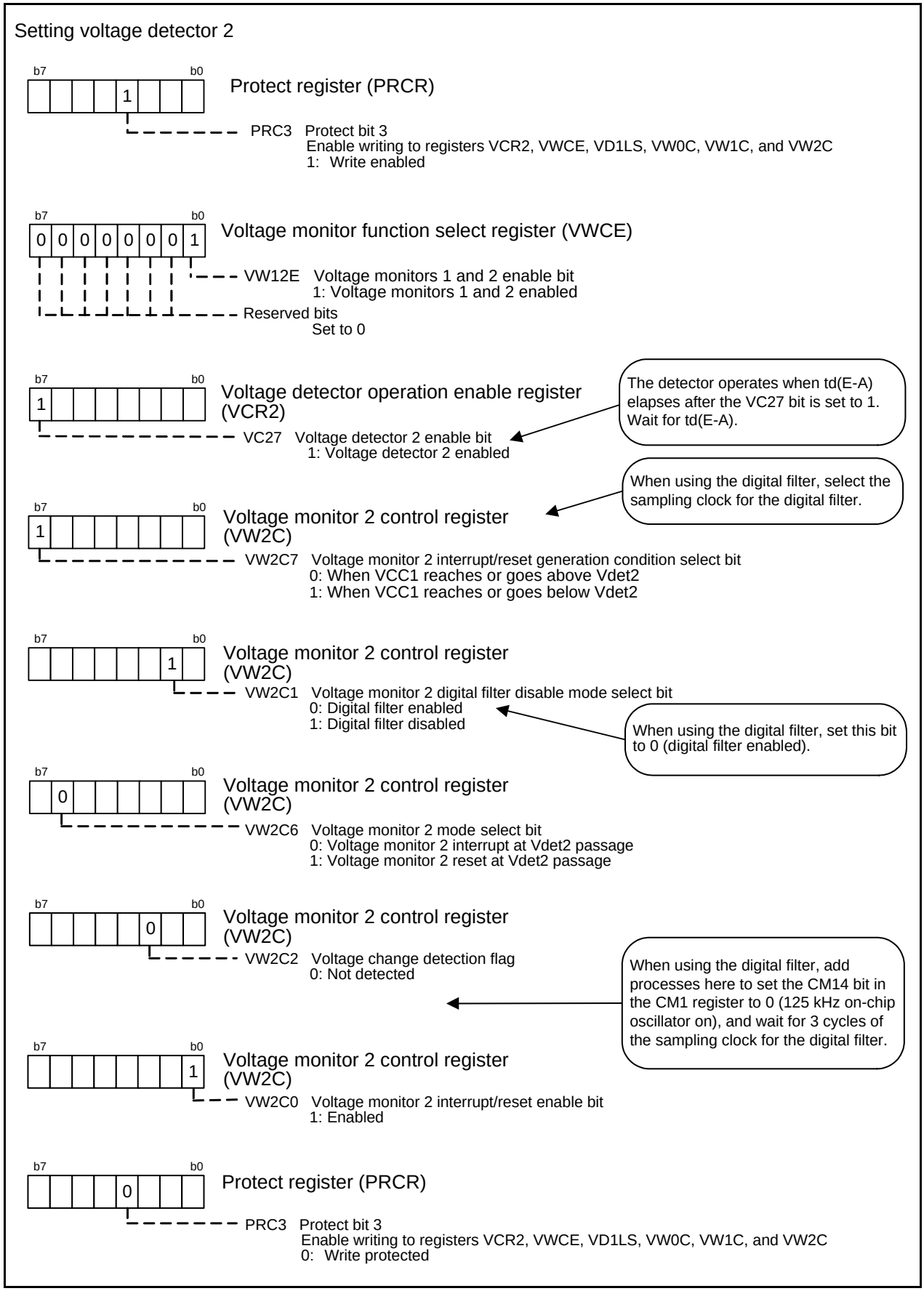
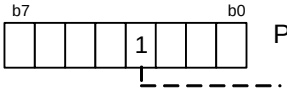


Figure 5.5 Setting Registers Associated with Voltage Monitor 2

5.3 Interrupt Handling and Register Setting

Figure 5.6 and Figure 5.7 show interrupt handling and register setting.

(1) Disable write protection



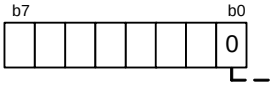
Protect register (PRCR)

PRC3 Protect bit 3
Enable writing to registers VCR2, VWCE, VD1LS, VW0C, VW1C, and VW2C
1: Write enabled

(2) Vdet2 passage

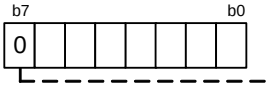
When passed downward through Vdet2

1. Change the conditions to generate the voltage monitor 2 interrupt.



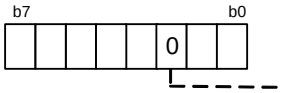
Voltage monitor 2 control register (VW2C)

VW2C0 Voltage monitor 2 interrupt/reset enable bit
0: Disabled



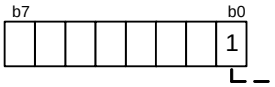
Voltage monitor 2 control register (VW2C)

VW2C7 Voltage monitor 2 interrupt/reset generation condition select bit
0: When VCC1 reaches or goes above Vdet2



Voltage monitor 2 control register (VW2C)

VW2C2 Voltage change detection flag
0: Not detected



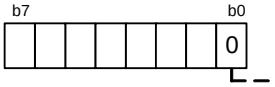
Voltage monitor 2 control register (VW2C)

VW2C0 Voltage monitor 2 interrupt/reset enable bit
1: Enabled

2. Transmit the message “Under Vdet2” to the PC.

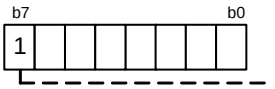
When passed upward through Vdet2

1. Change the conditions to generate the voltage monitor 2 interrupt.



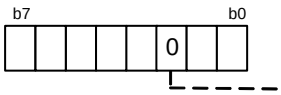
Voltage monitor 2 control register (VW2C)

VW2C0 Voltage monitor 2 interrupt/reset enable bit
0: Disabled



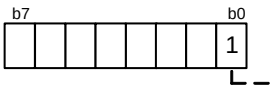
Voltage monitor 2 control register (VW2C)

VW2C7 Voltage monitor 2 interrupt/reset generation condition select bit
1: When VCC1 reaches or goes below Vdet2



Voltage monitor 2 control register (VW2C)

VW2C2 Voltage change detection flag
0: Not detected



Voltage monitor 2 control register (VW2C)

VW2C0 Voltage monitor 2 interrupt/reset enable bit
1: Enabled

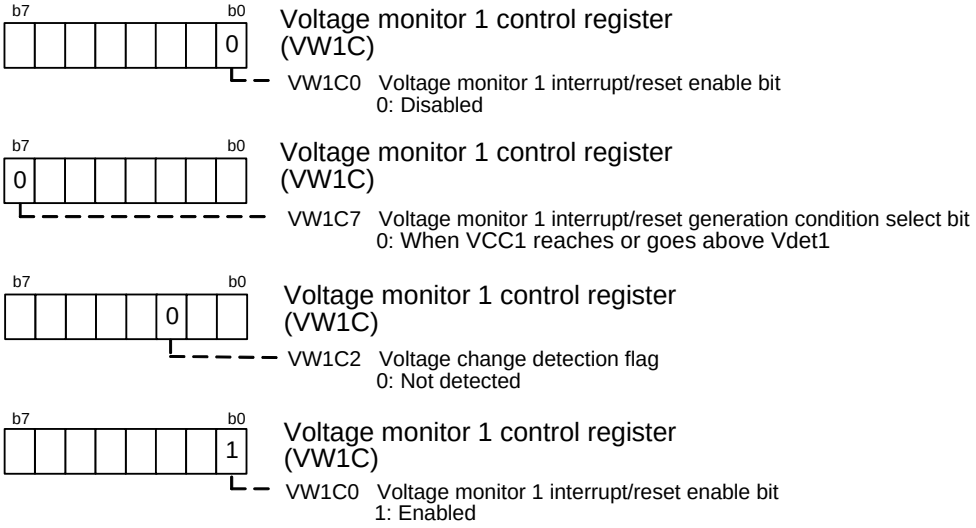
2. Transmit the message “Over Vdet2” to the PC.

Figure 5.6 Interrupt Handling and Register Setting (1/2)

(3) Vdet1 passage

When passed downward through Vdet1

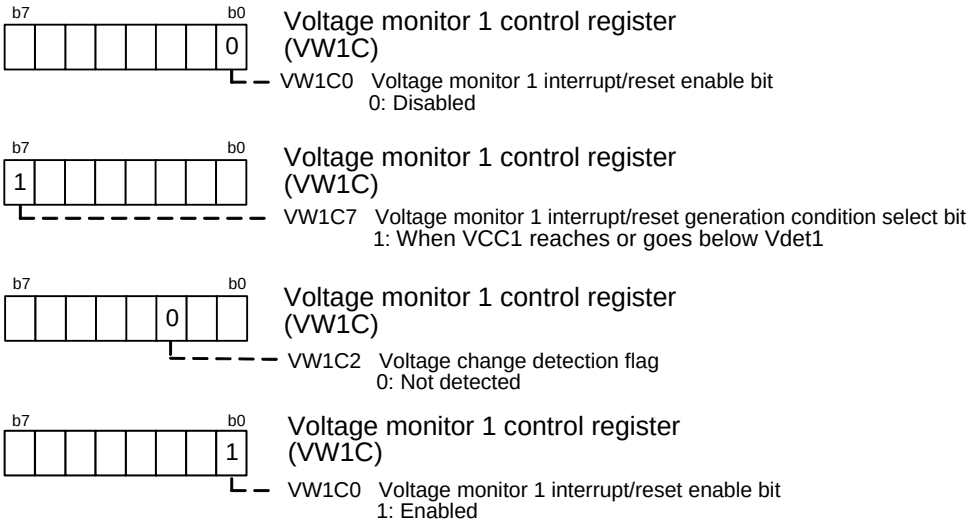
1. Change the conditions to generate the voltage monitor 1 interrupt.



1. Transmit the message “Under Vdet1” to the PC.

When passed upward through Vdet1

1. Change the conditions to generate the voltage monitor 1 interrupt.



2. Transmit the message “Over Vdet1” to the PC.

(4) Enable write protection

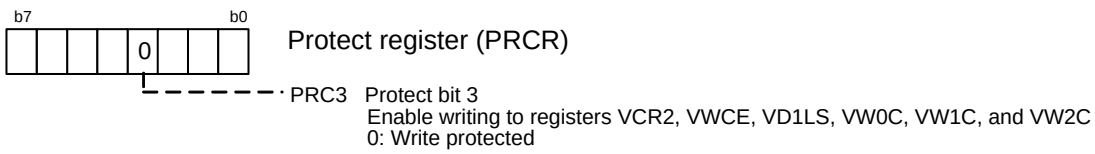


Figure 5.7 Interrupt Handling and Register Setting (2/2)

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/6C Group User's Manual: Hardware Rev. 2.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series/R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	M16C/6C Group Using the Voltage Detector

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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