M16C/6C Group

Supplement for Serial Interface UARTi (i = 0 to 5)

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1. Abstract

This document is a supplement for serial interface UARTi (i = 0 to 5) specifications in the M16C/6C Group.

2. Introduction

This document includes modifications to the serial interface UARTi specifications in Technical Update: TN-16C-A201A/E “Specification Modifications in M16C/65, M16C/64A, M16C/63 and M16C/6C Groups”, and supplemental information for the Serial Interface UARTi chapter in the M16C/6C Group User’s Manual: Hardware.

Use this document to verify changes made to the specifications. A previous version of the chapter from the hardware manual is attached at the end for comparison.

When making a program using I^2C mode, refer to application notes listed below.

- I^2C-bus Interface Using UARTi Special Mode 1 (REJ05B1349)
- I^2C-bus Interface Using UARTi Special Mode 1 (Master Transmit/Receive) (REJ05B1422)
- I^2C-bus Interface Using UARTi Special Mode 1 (Slave Transmit/Receive) (REJ05B1423)

3. Supplement Content and Modifications to Specifications

3.1 Clock Synchronous Serial I/O Mode, UART Mode

The description for “Transmit/Receive Circuit Initialization” in the previous version of the hardware manual is correct, but not clear enough. The description has been rewritten as shown below.

Processing When Terminating Communication or When an Error Occurs
When communication is terminated in clock synchronous serial I/O mode or UART mode, or when a communication error occurs, use the following procedure to reset communication:

(1) Set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to one of the following:
- 001b (clock synchronous serial I/O mode)
- 100b (UART mode, character length is 7 bits)
- 101b (UART mode, character length is 8 bits)
- 110b (UART mode, character length is 9 bits)

(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

3.2 I^2C Mode

This section describes the modifications made to the specifications. I^2C mode function descriptions have been revised. Refer to 4. “Special Mode 1 (I^2C Mode)” for details on major changes.

3.2.1 UiSMR4 Register

Bits in the UiSMR4 register are used in I^2C mode. To set these bits to 1, preset the IICM bit in the UiSMR register to 1 (I^2C mode). Do not set these bits to 1 when the IICM bit is 0.
Bits STAREQ, RSTAREQ, STPREQ, STSPSEL, and SCLHI are used in master mode of I^2C mode. Set the STSPSEL bit to 1 (select start condition/stop condition generate circuit) after setting the STARREQ, RSTAREQ, or STPREQ bit to 1 (start).
Bits ACKD, ACKC, and SWC9 are used in slave mode of I^2C mode.

3.2.2 UiBRG Register

Set the UiBRG register to a value of 03h or greater in I^2C mode.

3.2.3 UiSMR3 Register

Set the CKPH bit in the UiSMR3 register to 1 (with clock delay) in I^2C mode.

3.2.4 Additional Notes

Notes listed below have been added.

3.2.4.1 Low/High-level Input Voltage and Low-level Output Voltage

The low-level input voltage, high-level input voltage, and low-level output voltage differ from the I^2C-bus specification.
Refer to the recommended operating conditions for I/O ports which share the pins with SCL and SDA.

I^2C-bus specification
High level input voltage (V_{IH}) = min. 0.7 V_{CC}
Low level input voltage (V_{IL}) = max. 0.3 V_{CC}

3.2.4.2 Setup and Hold Times When Generating a Start/Stop Condition

When generating a start condition, the hold time (t_{HD}:STA) is a half cycle of the SCL clock. When generating a stop condition, the setup time (t_{SU}:STO) is a half cycle of the SCL clock.

When the SDA digital delay function is enabled, take delay time into consideration.

The following shows a calculation example of hold and setup times when generating a start/stop condition.

Calculation example when setting 100 kbps

- UiBRG count source: f1 = 20 MHz
- UiBRG register setting value: n = 100 - 1
- SDA digital delay setting value: DL2 to DL0 are 101b (5 or 6 cycles of UiBRG count source)

f_{SCL} (theoretical value) = f1 / (2(n+1)) = 20 MHz / (2 × (99 + 1)) = 100 kbps

t_{DL} = delay cycle count / f1 = 6 / 20 MHz = 0.3 µs

$t_{HD:STA}$ (theoretical value) = 1 / (2f_{SCL} (theoretical value)) = 1 / (2 × 100 kbps) = 5 µs

$t_{SU:STO}$ (theoretical value) = 1 / (2f_{SCL} (theoretical value)) = 1 / (2 × 100 kbps) = 5 µs

$f_{HD:STA}$ (actual value) = $t_{HD:STA}$ (theoretical value) - t_{DL} = 5 µs - 0.3 µs = 4.7 µs

$f_{SU:STO}$ (actual value) = $t_{SU:STO}$ (theoretical value) + t_{DL} = 5 µs + 0.3 µs = 5.3 µs

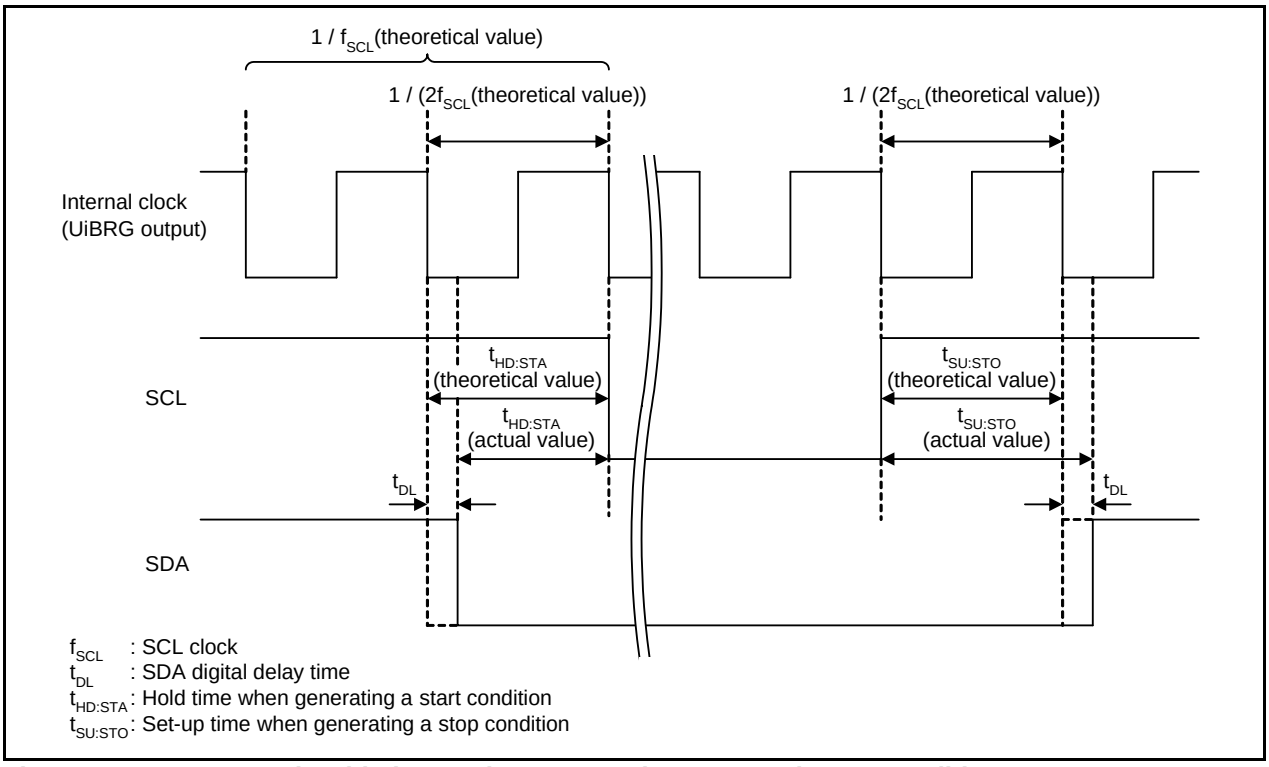


Figure 3.1 Setup and Hold Times When Generating Start and Stop Conditions

3.2.4.3 Restrictions on the Bit Rate When Using the UiBRG Count Source

In I^2C mode, set the UiBRG register to a value of 03h or greater.

A maximum of three UiBRG count source cycles are necessary until the internal circuit acknowledges the SCL clock level. The connectable I^2C-bus bit rate is one third or less than the UiBRG count source speed. If a value between 00h to 02h is set to the UiBRG register, bit slippage may occur.

3.2.4.4 Restart Condition in Slave Mode

When a restart condition is detected in slave mode, the successive processes may not be executed correctly. In slave mode, do not use a restart condition.

3.2.4.5 Requirements to Start Transmission/Reception in Slave Mode

When transmission/reception is started in slave mode and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.

Requirements to start transmission (in no particular order):

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

•Requirements to start reception (in no particular order):

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

3.3 Special Mode 2

Use special mode 2 in master mode. Do not use special mode 2 in slave mode (external clock). Set the CKDIR bit in the UiMR register to 0 (internal clock) in special mode 2.

However, slave mode can be used under certain conditions. An application note for this is being prepared.

Serial Interface Special Mode 2 (Slave Transmission) (REJ05B1472-0100)

4. Special Mode 1 (I²C Mode)

4.1 Detecting Start and Stop Conditions

Start and stop conditions are detected by their respective detectors.
Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDAi pin changes state from high to low while the SCLi pin is in the high state. A stop condition detect interrupt request is generated when the SDAi pin changes state from low to high while the SCLi pin is in the high state.
Because the start and stop condition detect interrupts share the interrupt control register and vector, check the BBS bit in the UiSMR register to determine which interrupt source is requesting the interrupt.
To detect a start or stop condition, both the set-up and hold times require at least six cycles of the BRGi count source as shown in Figure 4.1. To meet the condition for the Fast-mode specification, the BRGi count source must be at least 10 MHz.

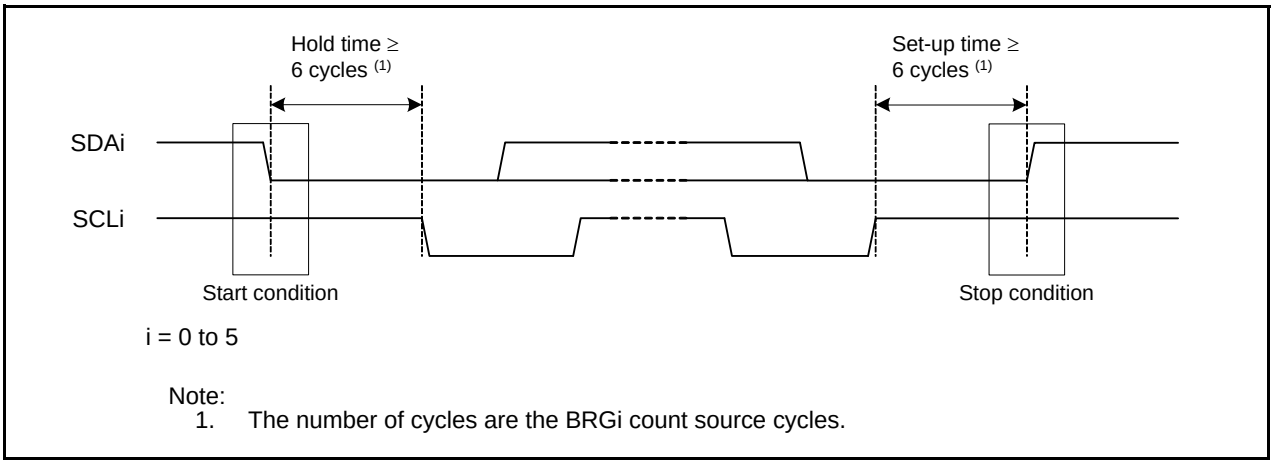


Figure 4.1 Detecting Start and Stop Conditions

4.2 Generating Start and Stop Conditions

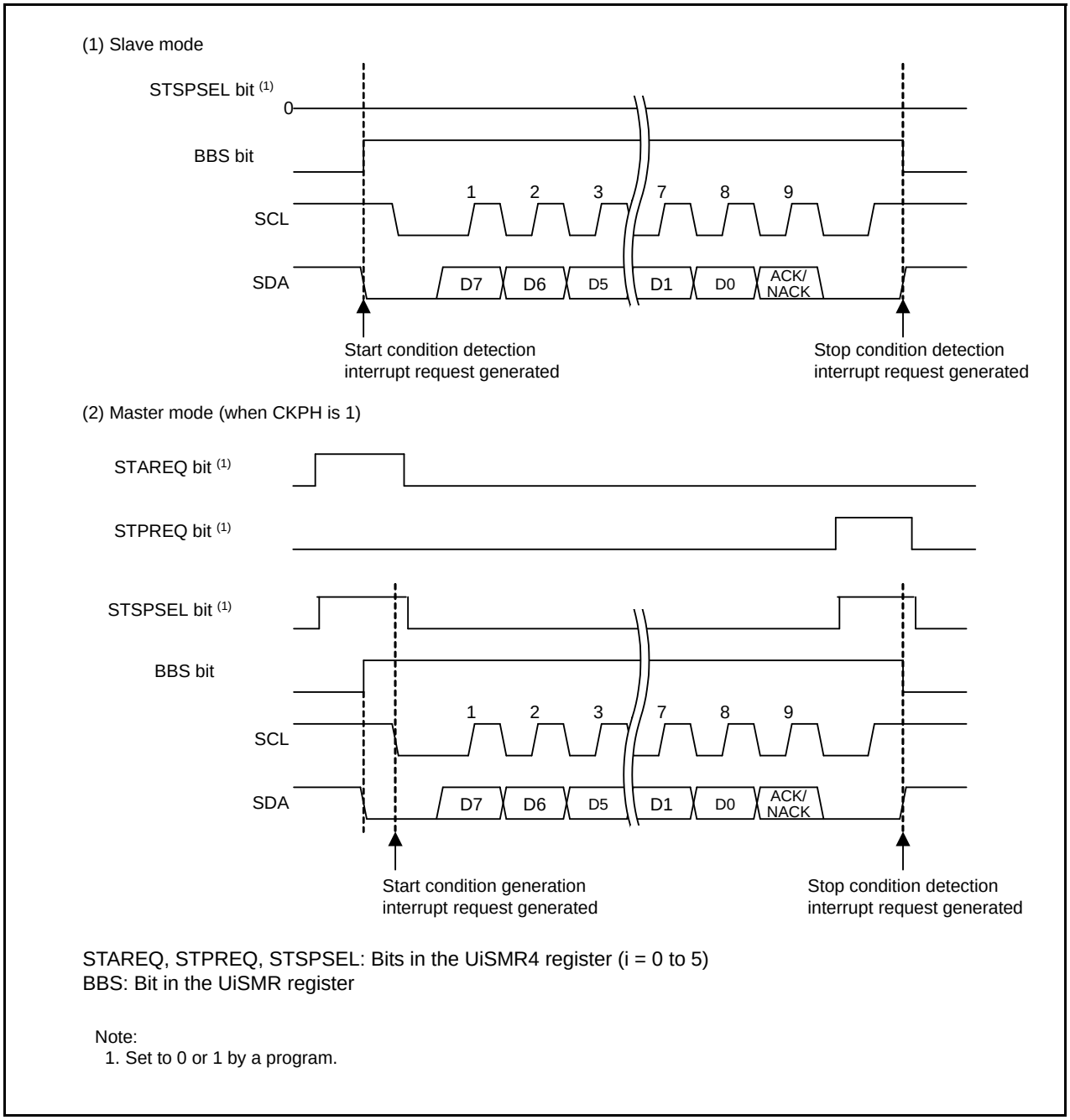
A start condition is generated by setting the STAREQ bit in the UiSMR4 register (i = 0 to 5) to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the UiSMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the UiSMR4 register to 1 (start).
The output procedure is described below.

(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the UiSMR4 register to 1 (output).

The functions of the STSPSEL bit are shown in Table 4.1 and Figure 4.2.

Table 4.1 STSPSEL Bit Functions

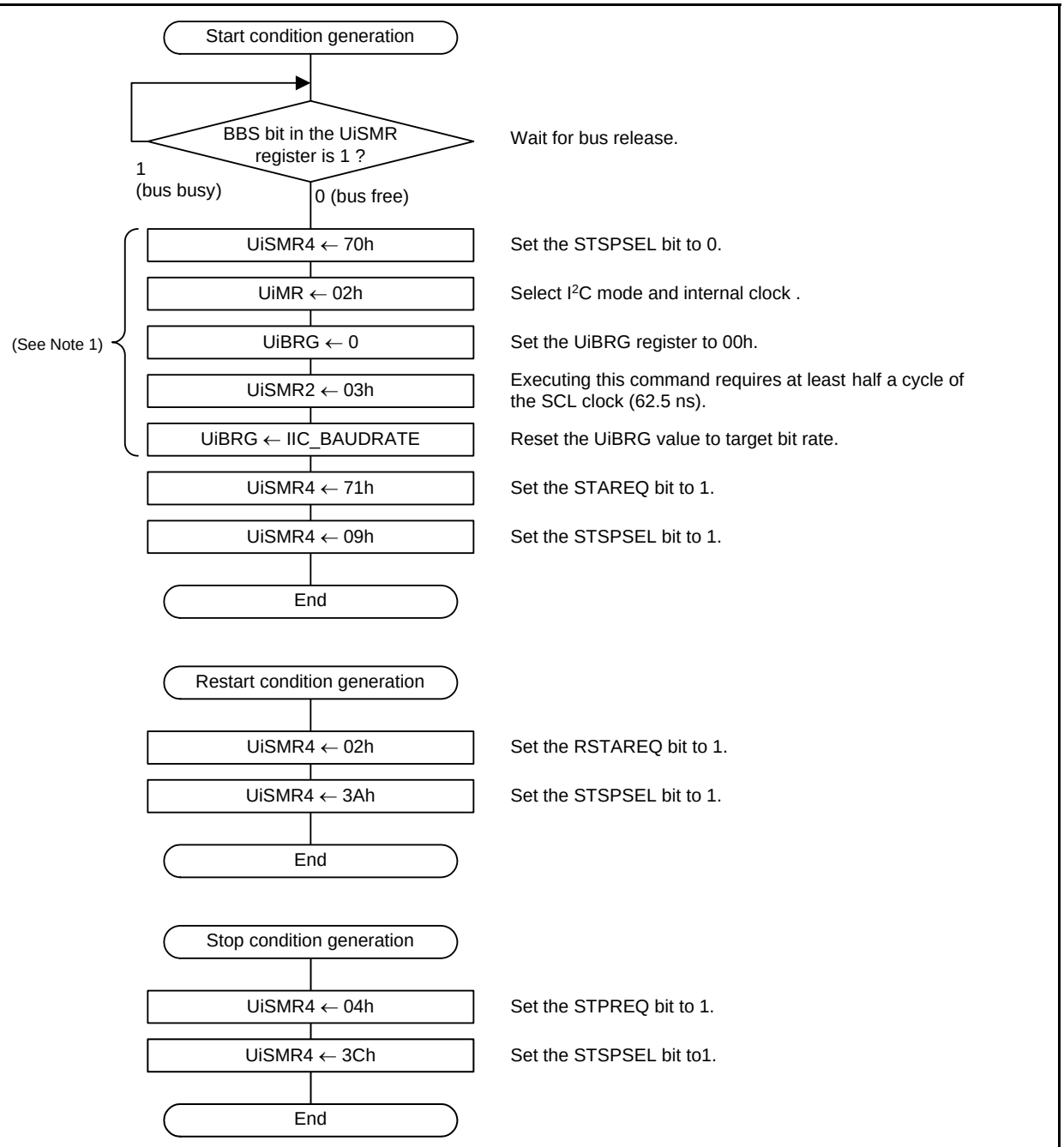
Function	STSPSEL = 0	STSPSEL = 1
Output of pins SCLi and SDAi	Output of transmit/receive clock and data Output of start/stop condition is accomplished by a program using ports (not automatically generated in hardware)	Output of a start/stop condition according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition Interrupt request generation timing	Detection of start/stop condition	Completion of generating start/stop condition



STAREQ, STPREQ, STSPSEL: Bits in the UiSMR4 register (i = 0 to 5)
BBS: Bit in the UiSMR register

Note:
1. Set to 0 or 1 by a program.

Figure 4.2 STSPSEL Bit Functions



The above assumes the following:
XIN = 16 MHz, main clock divided by 1 (no division), UiBRG count source = f1

Note:
1. After a stop condition is generated, when generating the next start condition, after setting the STSPSEL bit in the UiSMR4 register to 0 and waiting at least half a cycle of the SCL clock, then set the STAREQ bit to 1.

Technical update number: TN-16C-130A/EA

Figure 4.3 Register Setting Procedures for Condition Generation

4.3 Arbitration

The MCU determines whether the transmit data matches data input to the SDAi pin on the rising edge of SCLi. If it does not match the input data, arbitration takes place at the SDAi pin by stopping data output.

The ABC bit in the UiSMR register (i = 0 to 5) determines the update timing for the ABT bit in the UiRB register. When the ABC bit is 0 (update per bit), the ABT bit becomes 1 as soon as a data discrepancy is detected. If not detected, the ABT bit becomes 0. When the ABC bit is 1 (update per byte), the ABT bit becomes 1 on the falling edge of the eighth bit of SCLi if any discrepancy is detected. In this ABC bit setting, the ABT bit should be set to 0 to start the next 1-byte transmission/reception.

When the ALS bit in the UiSMR2 register is set to 1 (SDA output stop enabled), an arbitration lost occurs. As soon as the ABT bit becomes 1, the SDAi pin becomes high-impedance.

4.4 SCL Control and Clock Synchronization

Data transmission/reception in I^2C mode uses the transmit/receive clock. The clock speed increase makes it difficult to secure the required time for ACK generation and data transmit procedure. The I^2C mode supports a function of wait-state insertion to secure this required time and a function of clock synchronization with a wait-state inserted by other devices.

The SWC bit in the UiSMR2 register (i = 0 to 5) is used to insert a wait-state for ACK generation. When the SWC bit is set to 1 (the SCLi pin is held low after the eighth bit of SCLi is received), the SCLi pin is held low on the falling edge of the eighth bit of SCLi. When the SWC bit is set to 0 (no wait-state/wait-state cleared), the SCLi line is released.

When the SWC2 bit in the UiSMR2 register is set to 1 (the SCLi pin is held low), the SCLi pin is forced low even during transmission or reception. When the SWC2 bit is set to 0 (transmit/receive clock is output at the SCLi pin), the SCLi line is released to output the transmit/receive clock.

The SWC9 bit in the UiSMR4 register is used to insert a wait-state for checking received acknowledge bits. While the CKPH bit in the UiSMR3 register is 1 (clock delayed), when the SWC9 bit is set to 1 (the SCLi pin is held low after the ninth bit of the SCLi is received), the SCLi pin is held low on the falling edge of the ninth bit of SCLi. When the SWC9 bit is set to 0 (no wait-state/wait-state cleared), the SCLi line is released.

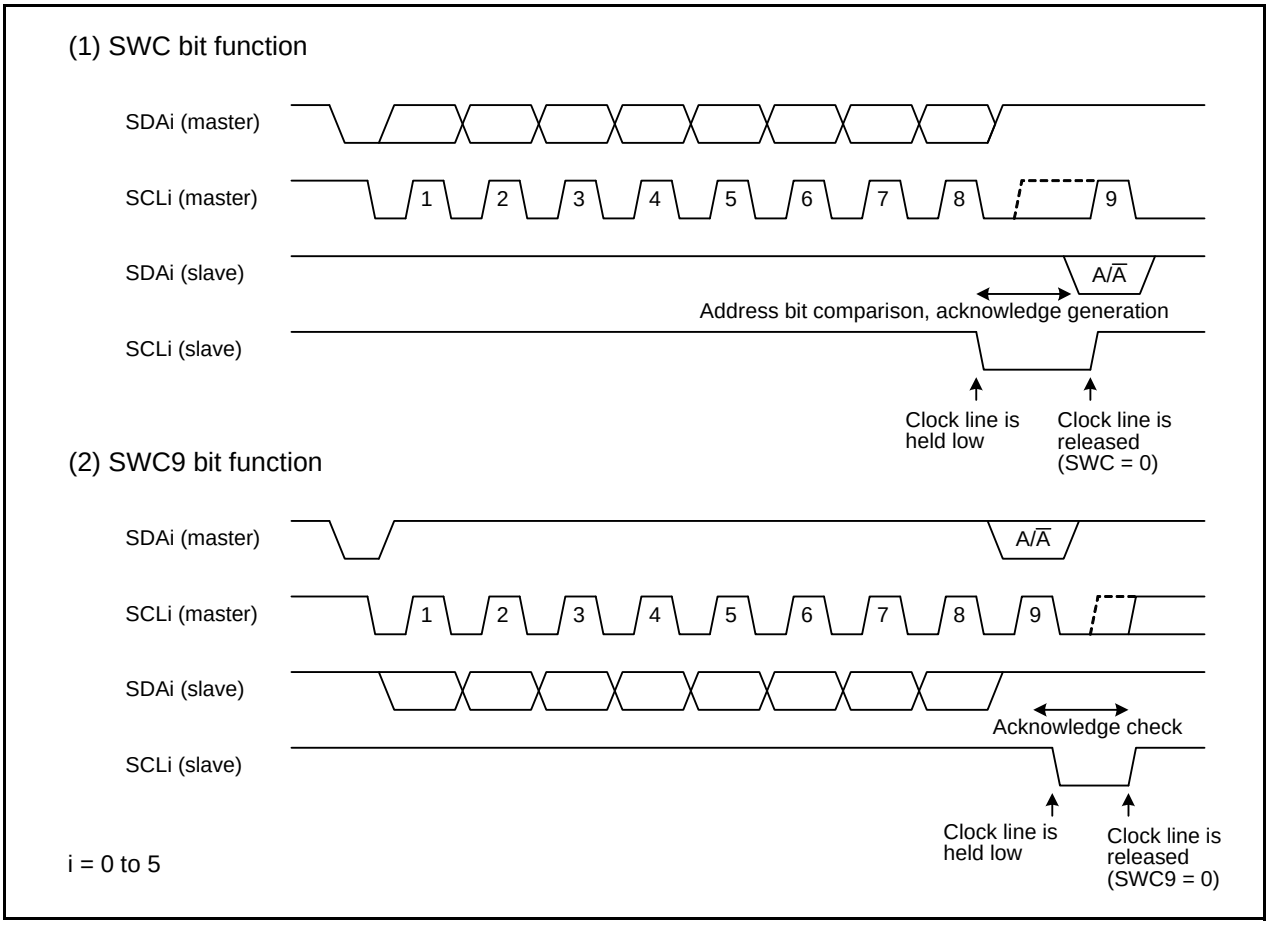


Figure 4.4 Inserting Wait-states Using Bits SWC and SWC9

The CSC bit in the UiSMR2 register synchronizes an internally generated clock with the clock applied to the SCLi pin. For example, if a wait-state is inserted from other devices, the two clocks are not synchronized. While the CSC bit is 1 (clock synchronization enabled) and the internal clock is held high, when a high at the SCLi pin changes to low, the internal clock becomes low in order to reload the UiBRG register value and resume counting. While the SCLi pin is held low, when the internal clock changes from low to high, the count is stopped until the SCLi pin becomes high. That is, the UARTi transmit/receive clock is the logical AND of the internal clock and SCLi. The synchronized period starts from one clock prior to the first synchronized clock and ends when the ninth clock is completed. The CSC bit can be set to 1 only when the CKDIR bit in the UiMR register is set to 0 (internal clock selected).

The SCLHI bit in the UiSMR4 register is used to leave the SCLi pin open when another master generates a stop condition while the master is performing a transmit/receive operation. While the SCLHI bit is set to 1 (output stopped), the SCLi pin is open (the pin is high-impedance) when a stop condition is detected and the clock output is stopped.

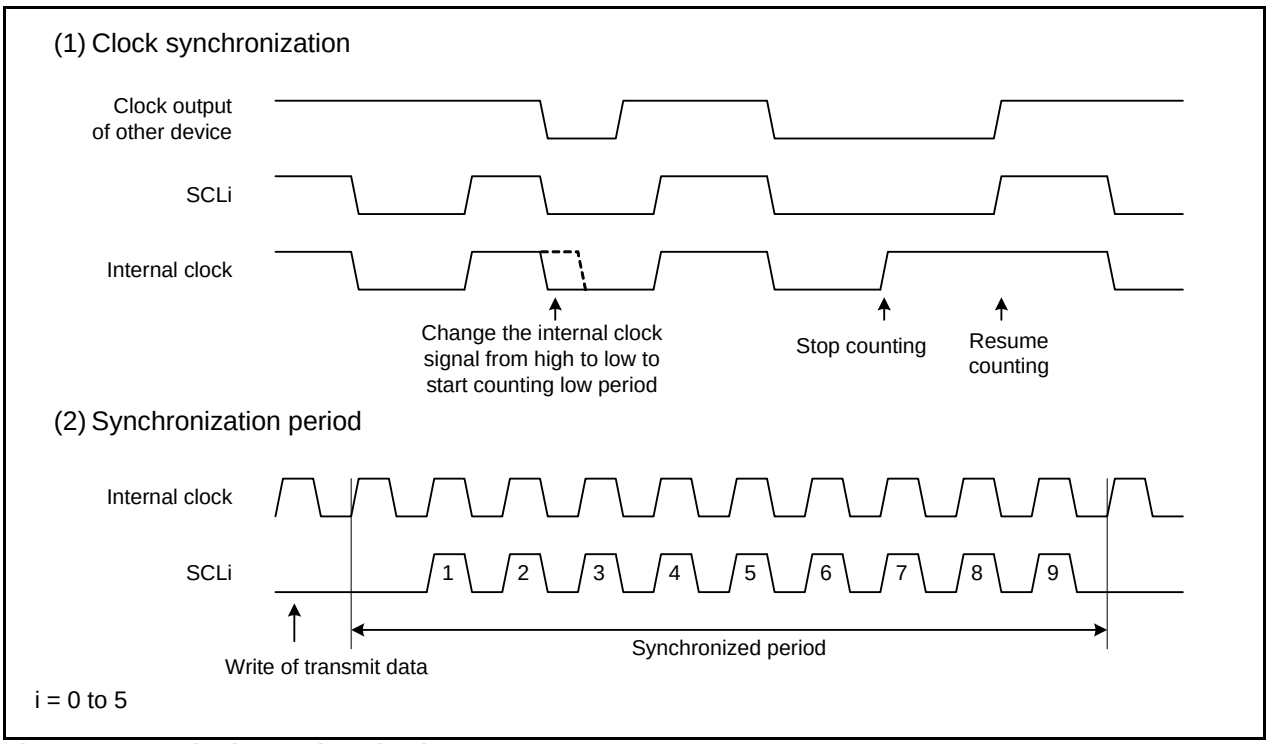


Figure 4.5 Clock Synchronization

4.5 SCL Clock Frequency

The SCL clock duty generated in I²C mode is 50%. The low-level width of the SCL clock is 1.25 µs when the I²C-bus setting is Fast-mode maximum SCL clock (400 kbps). This value does not satisfy the Fast-mode I²C-bus specification (f_{LOW} = minimum 1.3 µs). Set the SCL clock to 384.6 kbps or less to satisfy the SCL clock low-level width of 1.3 µs or more.

When the clock synchronous function (Figure 4.5 “Clock Synchronization”) is enabled, there is a sampling delay of the noise filter plus 1 to 1.5 cycles of UiBRG count source.

There is also a delay of the SCL clock when high is determined and the SCL clock high width is extended. Therefore, the actual SCL clock becomes slower than SCL clock bit rate setting.

To calculate the effective value of SCL clock, take the SCL clock rise time (t_R) into consideration.

The following is an example of an SCL clock calculation.

Example of an effective value of SCL clock calculation at 384.6 kbps

- UiBRG count source: f1 = 20 MHz
- UiBRG register setting value: n = 26 - 1
- SCL clock rise time: t_R = 100 ns
- SCL clock fall time: t_F = 0 ns
- Noise filter width: t_{NF} = 100 ns (1)
- Sampling delay: t_{SD} = 1 cycle

f_{SCL} (theoretical value) = f1 / (2(n + 1)) = 20 MHz / (2(25 + 1)) = 384.6 kbps

t_{LOW} = 1 / ($2f_{SCL}$ (theoretical value)) = 1 / (2 × 384.6 kbps) = 1.3 µs

t_{HIGH} = 1 / ($2f_{SCL}$ (theoretical value)) + t_{NF} + (t_{SD} × 1 / f1)
= 1 / (2 × 384.6 kbps) + 100 ns + (1 × 1 / 20 MHz)
= 1.45 µs

f_{SCL} (actual value) = 1 / (t_F + t_{LOW} + t_R + t_{HIGH}) = 1 / (0 ns + 1.3 µs + 100 ns + 1.45 µs) ≈ 350.8 kbps

Note:

1. Maximum 200 ns.

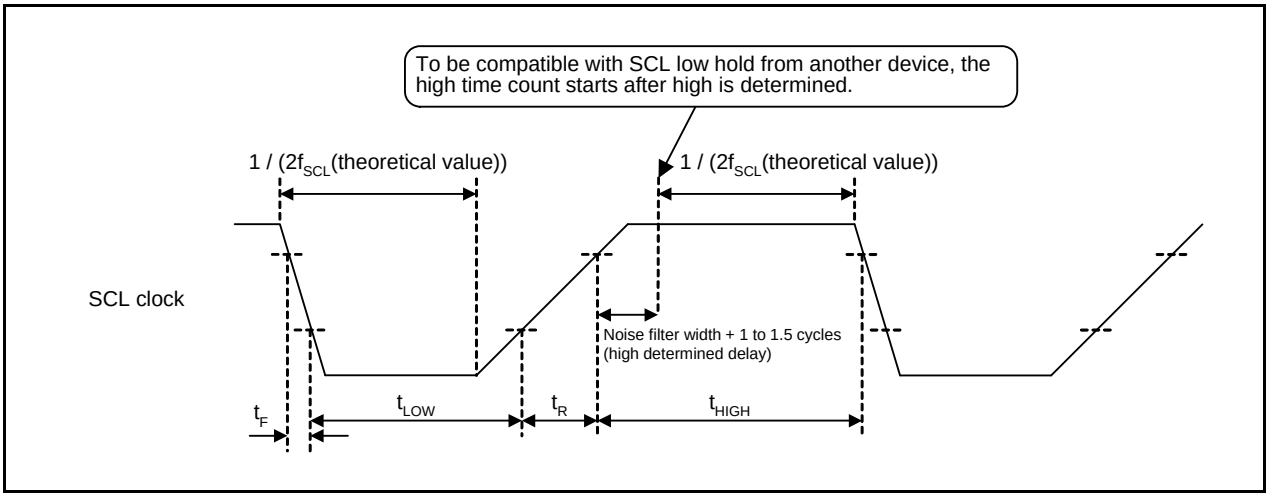


Figure 4.6 SCL Clock

4.6 SDA Output Control

When transmitting byte data, the SDAi pin outputs transmit data for the first to eighth bits, and it is released to receive an acknowledgement for the ninth bit.

In I^2C mode, set 9-bit data to the UiTB register. In 9-bit data, set the transmit data to bits b7 to b0 and set b8 to 1. By setting the UFORM bit in the UiC0 register to 1 (MSB first) and 9-bit data to the UiTB register, transmit data is output from the SDAi pin in the following order: b7, b6, b5, b4, b3, b2, b1, b0 and b8. As b8 is 1, the SDAi pin becomes high-impedance at the ninth bit and an acknowledgment can be received.

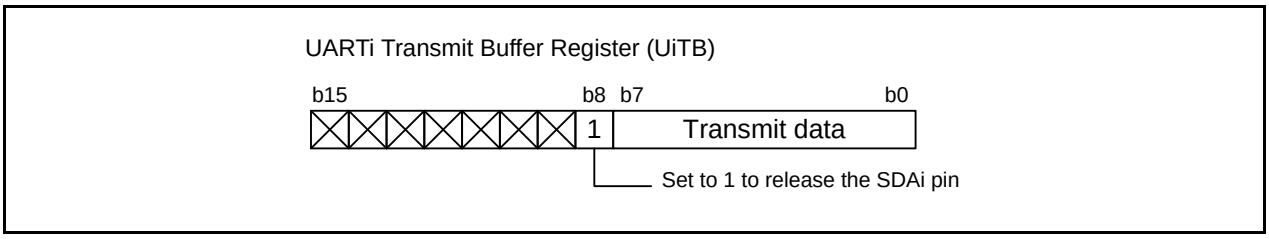


Figure 4.7 UiTB Register Setting (SDA Output)

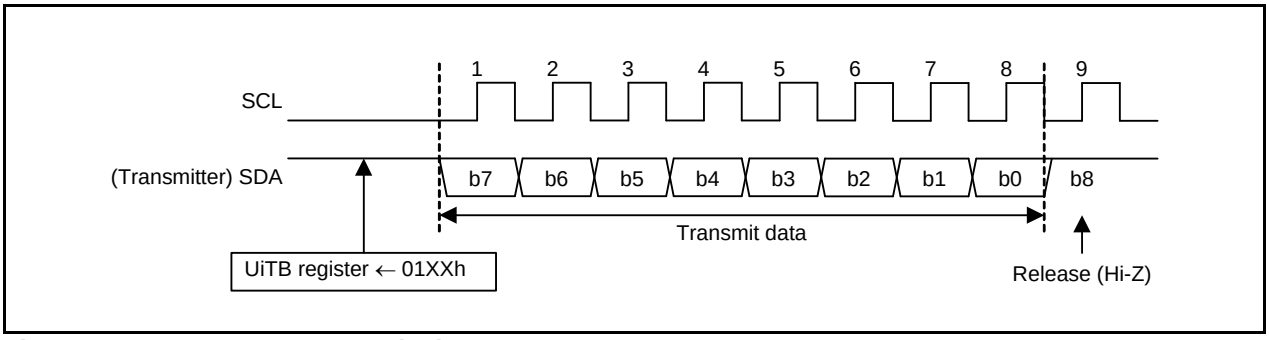


Figure 4.8 Byte Data Transmission

Set bits DL2 to DL0 in the UiSMR3 register to add no delays or a delay of one to eight UiBRG count source clock cycles to SDAi output.

Setting the SDHI bit in the UiSMR2 register to 1 (SDA output disabled) forcibly places the SDAi pin in a high-impedance state. Do not write to the SDHI bit at the rising edge of the UARTi transfer clock as the ABT bit may inadvertently become 1 (detected).

4.7 SDA Digital Delay

When transferring data with the I2C-bus, change the data while the SCL clock is low. When SDA is changed while the SCL clock is a high, the change is recognized as one of the corresponding conditions (see 3.2.4.2 “Setup and Hold Times When Generating a Start/Stop Condition”).
This function delays output from the SDAi pin. By delaying the change of the SDA, the data can be changed while the SCL clock is low. This function is enabled by setting bits DL2 to DL0 in the UiSMR3 register to 001b to 111b, and disabled by setting them to 000b.

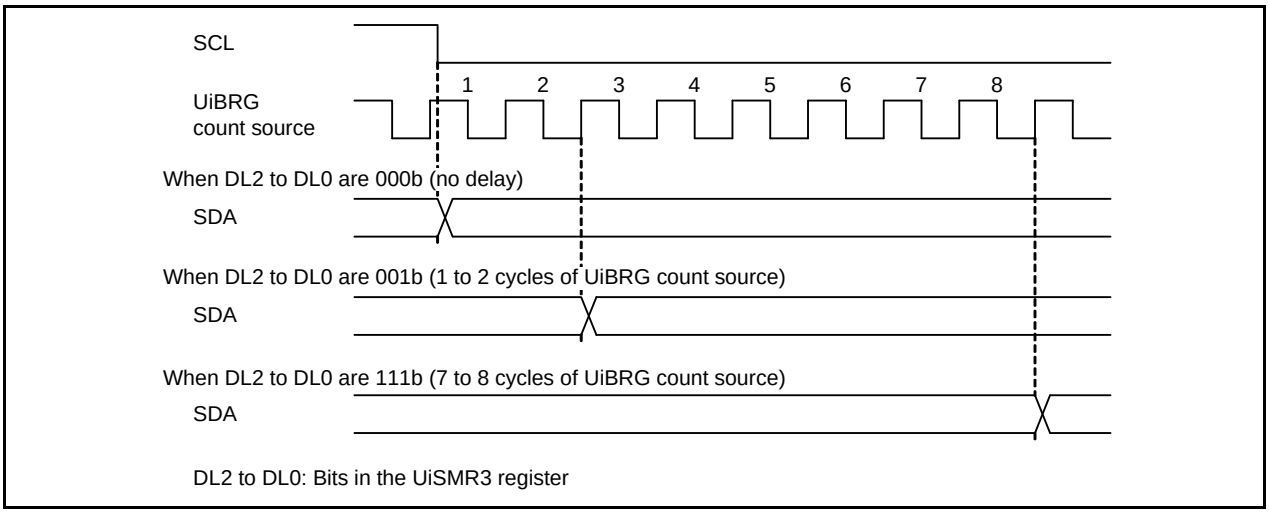


Figure 4.9 SDA Output Selection by Setting Bits DL2 to DL0

4.8 SDA Input

When the IICM2 bit in the UiSMR2 register (i = 0 to 5) is set to 0, the first 8 bits of received data (D7 to D0) are stored in bits 7 to 0 in the UiRB register and the ninth bit (ACK/NACK) is stored in bit 8.
When the IICM2 bit is 1, the first to seventh bits (D7 to D1) of the received data are stored in bits 6 to 0 in the UiRB register and the eighth bit (D0) is stored in bit 8 in the UiRB register. Even when the IICM2 bit is 1, if the CKPH bit in the UiSMR3 register is 1, the same data as when the IICM2 bit is 0 can be read. To read the data, read the UiRB register after the rising edge of ninth bit of the corresponding clock pulse.

When receiving byte data, the SDAi pin is released for the first to eighth bits to receive data, and an acknowledgment is generated for the ninth bit. NACK is generated when the last byte data is received in master mode, or when the slave address does not match in slave mode. In all other cases, ACK is generated.
In I2C mode, set 9-bit data to the UiTB register. In 9-bit data, set FFh to b7 to b0 to release the SDAi pin and set b8 to 0 to generate ACK or 1 to generate NACK.
By setting 00FFh or 01FFh as 9-bit data to the UiTB register, the SDAi pin becomes high-impedance for the first to eighth bits, and data can be received. ACK or NACK is generated at the ninth bit.
Read the received data from the UiRB register. When the clock delay function is used, data transfer to the UiRB register occurs twice and each UiRB register value is different.

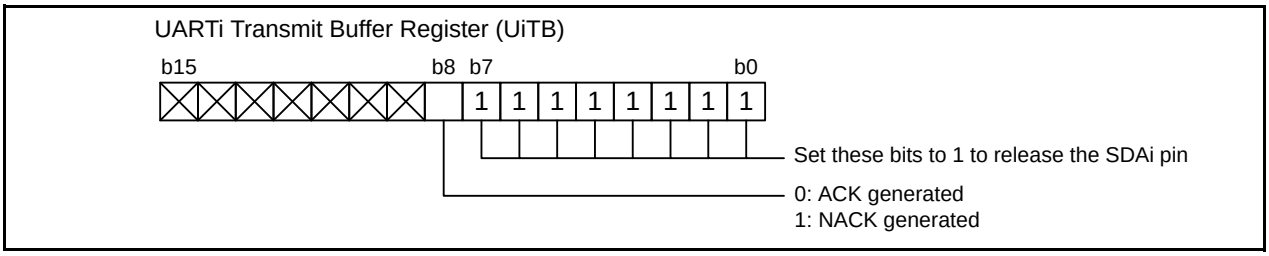


Figure 4.10 UiTB Register Setting (SDA Input)

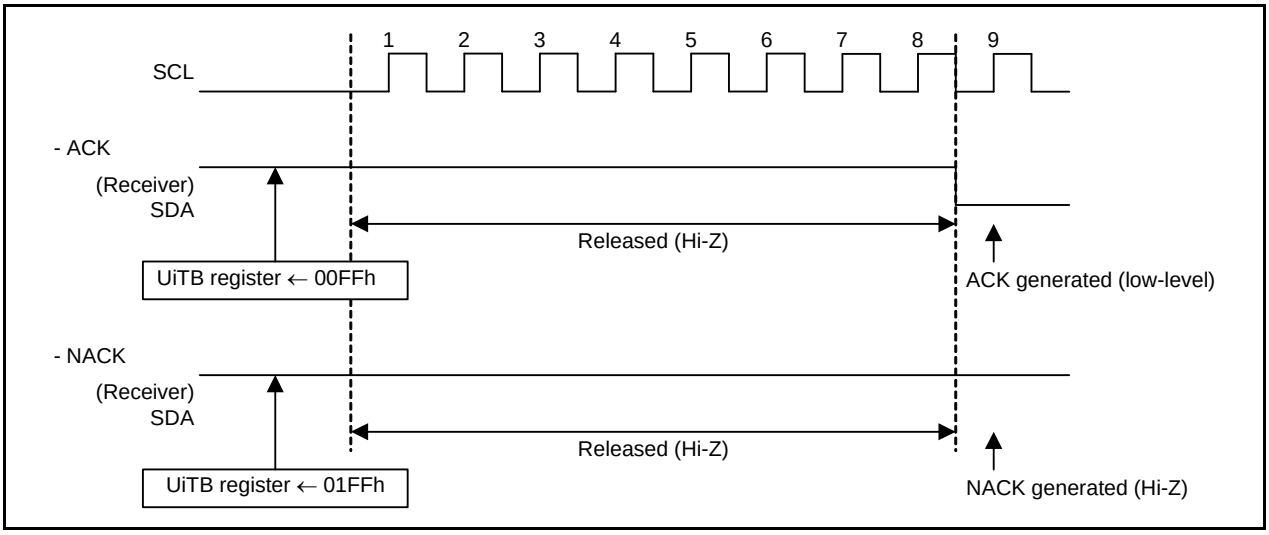


Figure 4.11 Byte Data Reception

4.9 ACK and NACK

When data is to be received in master mode, ACK is output after 8 bits are received by setting the UiTB register to 00FFh as dummy data. When the STSPSEL bit in the UiSMR4 register (i = 0 to 5) is set to 0 (serial I/O circuit selected) and the ACKC bit is set to 1 (ACK data output), the value of the ACKD bit is output at the SDAi pin.

If the IICM2 bit is 0, a NACK interrupt request is generated when the SDAi pin is held high at the rising edge of the ninth bit of SCLi. An ACK interrupt request is generated when the SDAi pin is held low.

If the DMA request source is “UARTi receive interrupt request or ACK interrupt request”, the DMA transfer is activated when ACK is detected.

4.10 Initialization of Transmission/Reception

Select the external clock as the transmit/receive clock when using this function.

If a start condition is detected while the STAC bit in the UiSMR2 register is 1 (initialize the circuit if the start condition is detected), the serial interface operates as follows:

- The transmit shift register is initialized, and the UiTB register value is transferred to the transmit shift register. Doing so starts the data transmission when the next clock pulse is applied. However, the UARTi output value does not change until the first bit of data is output synchronously with the input clock. It remains the same as when a start condition was detected.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit becomes 1 (hold the SCLi pin low after the eighth bit of SCLi is received). Consequently, the SCLi pin is pulled low at the falling edge of the ninth clock pulse.

When UARTi transmission/reception is started using this function, the TI bit does not change.

When the UARTi initializing function is used in slave mode, UARTi is initialized automatically when a start condition is detected. Therefore, an interrupt is unnecessary for detecting a start condition.

5. Reference Documents

M16C/6C Group User's Manual: Hardware Rev.2.00 (R01UH0138EJ0200)

Application Notes
Application notes indicated in 2. "Introduction" and application notes for other modes have been prepared.

The latest versions can be downloaded from the Renesas Electronics website.

Reference: the previous version of the UARTi document
The previous version of UARTi document is attached at the end of this document.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	M16C/6C Group Supplement for Serial Interface UARTi (i = 0 to 5)

Rev.	Date	Description	
		Page	Summary
1.00	2011.03.09	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Colophon 1.0

22. Serial Interface UARTi (i = 0 to 5)

22.1 Introduction

Each UARTi has a dedicated timer to generate a transmit/receive clock, so it operates independently of the others.

Table 22.1 lists Specifications of UARTi (i = 0 to 5), Table 22.2 lists Specification Difference in UART0 to UART5, Figure 22.1 to Figure 22.3 show UARTi Block Diagram, and Figure 22.4 shows UARTi Transmit/ Receive Unit Block Diagram.

Table 22.1 Specifications of UARTi (i = 0 to 5)

Item	Specification
Operational mode	• Clock synchronous serial I/O mode • Clock asynchronous serial I/O mode (UART mode) • Special mode 1 (I^2C mode) • Special mode 2 The simplified I^2C-bus interface is supported. • Special mode 3 (bus collision detection function, IE mode) A 1-byte wave of the UART mode approximates 1-bit of the IEBus. • Special mode 4 (SIM mode) UART2 is available. The SIM interface is supported.

Table 22.2 Specification Difference in UART0 to UART5

Mode	UART0	UART1	UART2	UART3	UART4	UART5
Clock synchronous serial I/O mode	Available		Available	Available		Available
Clock asynchronous serial I/O mode (UART mode)	Available		Available	Available		Available
Special mode 1 (I^2C mode)	Available		Available	Available		Available
Special mode 2	Available		Available	Available		Available
Special mode 3 (IE mode)	Available		Available	Available		Available
Special mode 4 (SIM mode)	Not available		Available	Not available		Not available
Memory expansion mode or microprocessor mode	Can be used			Do not use		Can be used

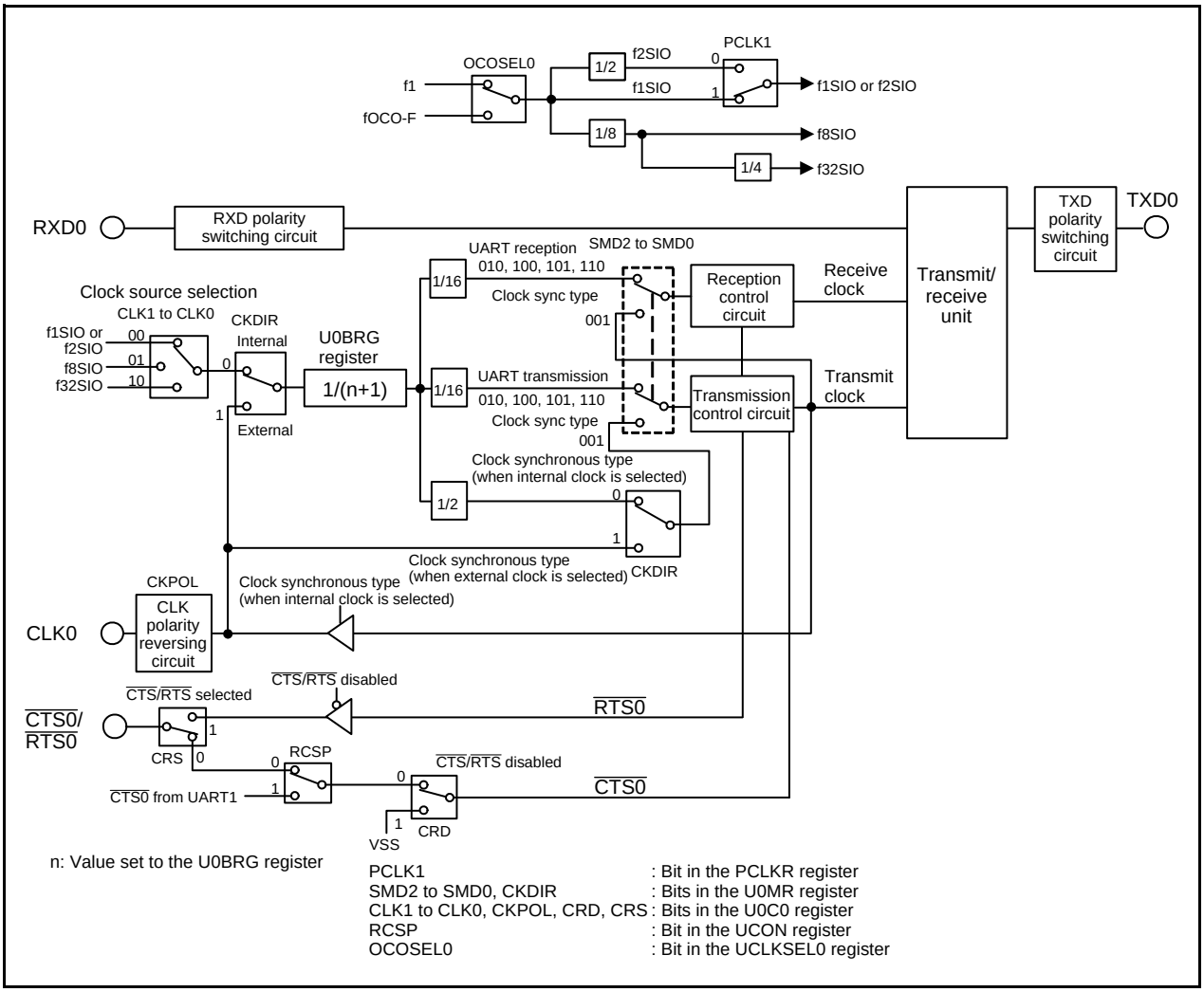


Figure 22.1 UART0 Block Diagram

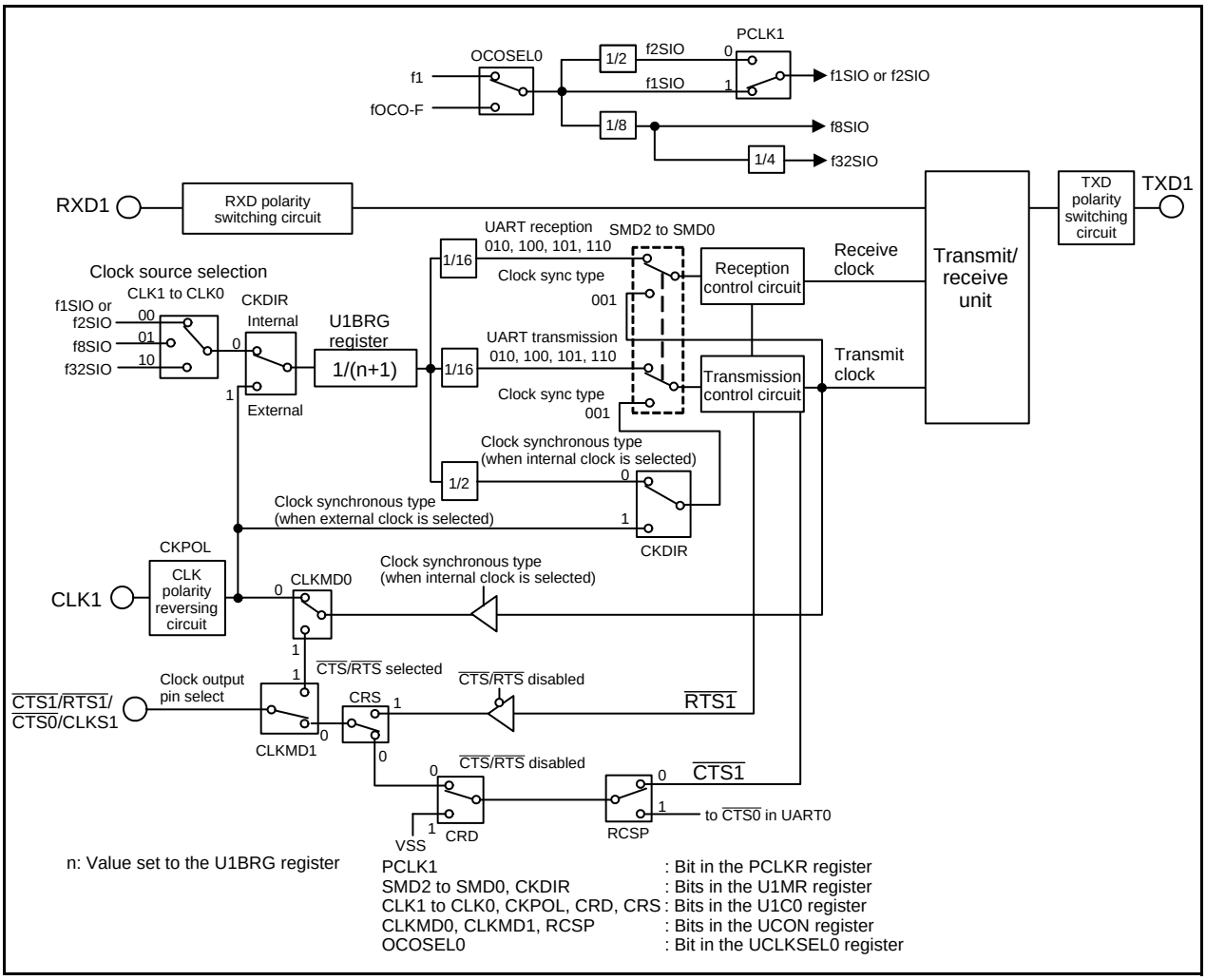
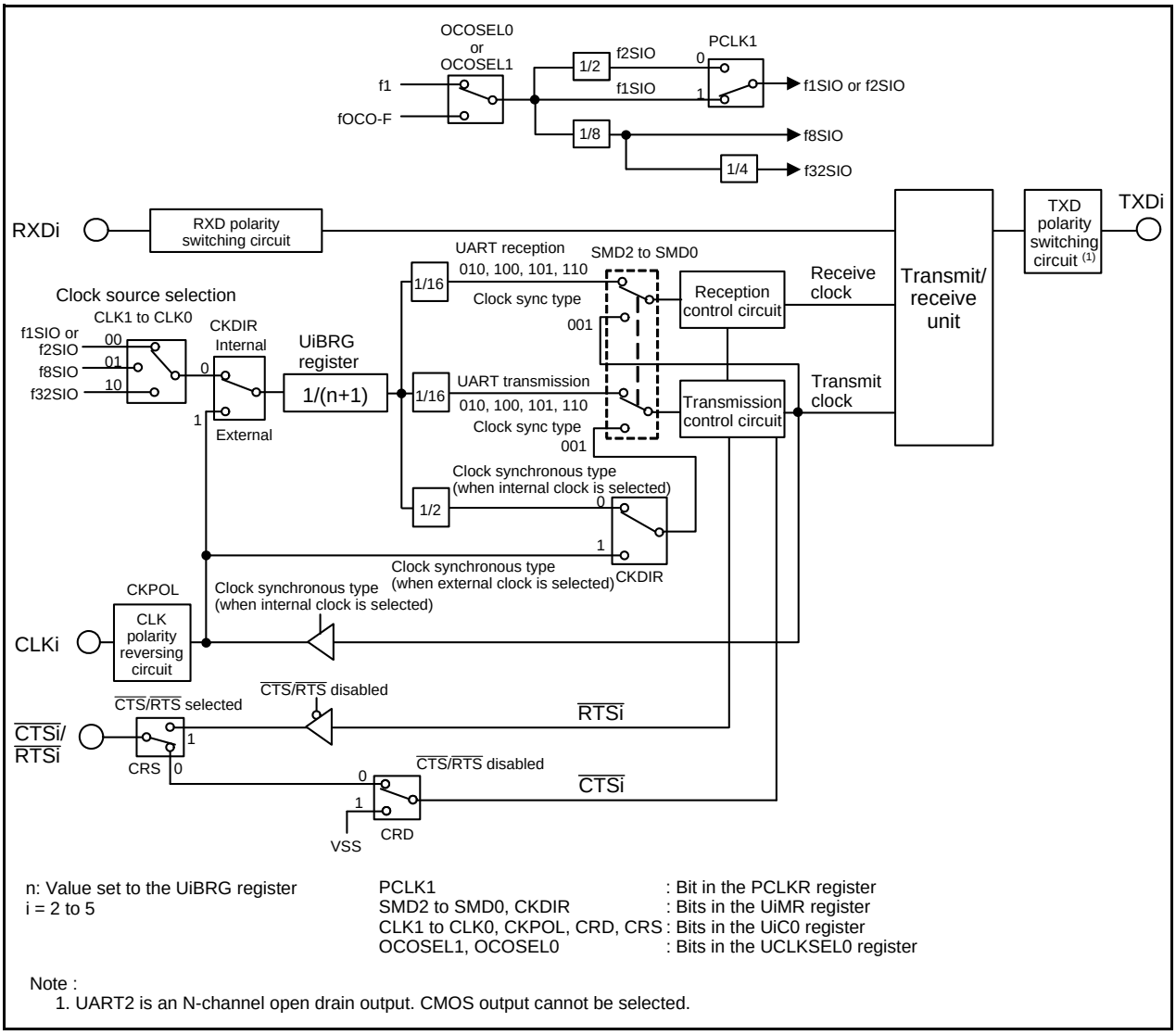


Figure 22.2 UART1 Block Diagram



n: Value set to the UiBRG register
i = 2 to 5

PCLK1 : Bit in the PCLKR register
SMD2 to SMD0, CKDIR : Bits in the UiMR register
CLK1 to CLK0, CKPOL, CRD, CRS : Bits in the UiC0 register
OCOSEL1, OCOSEL0 : Bits in the UCLKSEL0 register

Note :
1. UART2 is an N-channel open drain output. CMOS output cannot be selected.

Figure 22.3 Block Diagram of UART2 to UART5

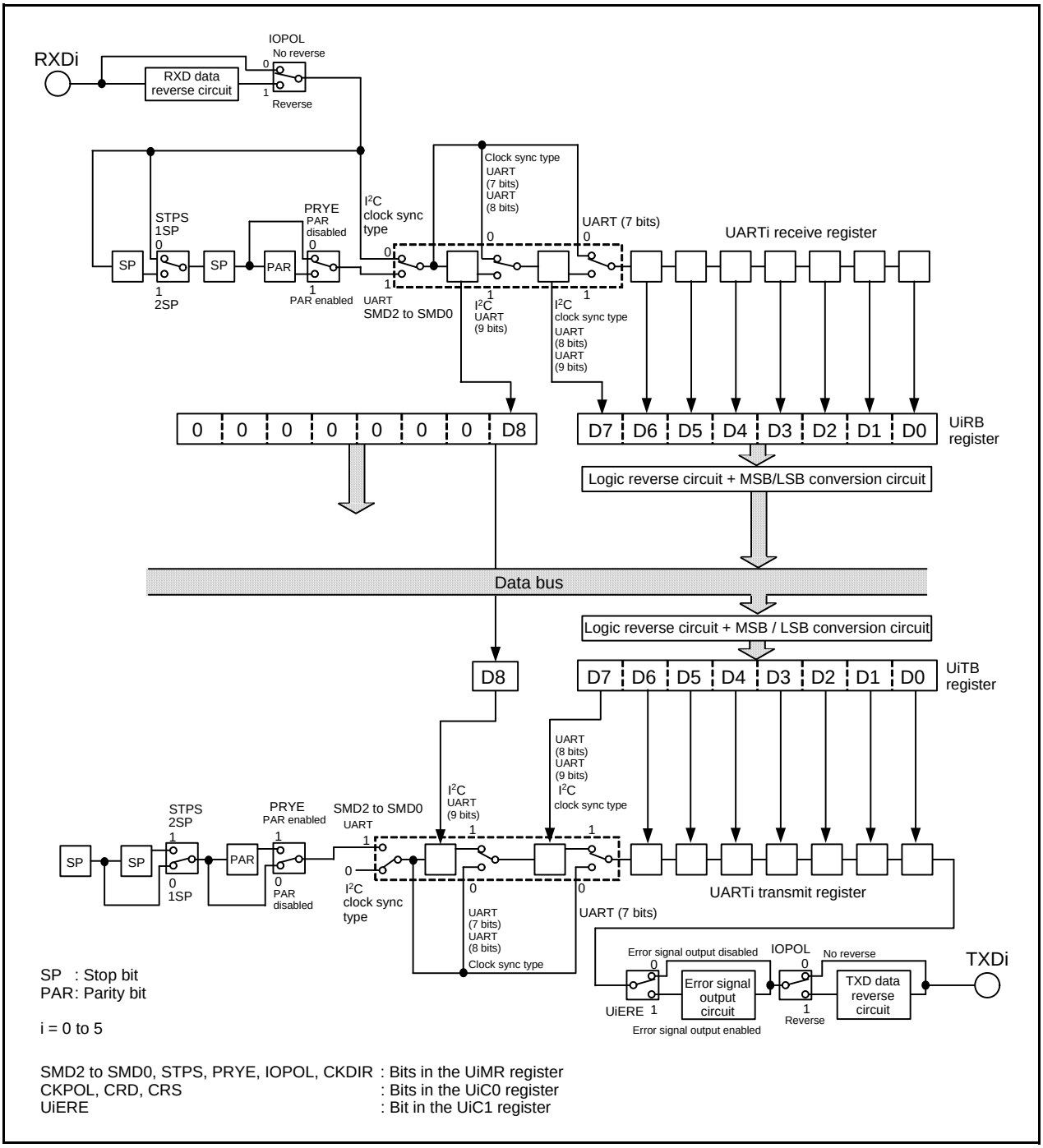


Figure 22.4 UARTi Transmit/Receive Unit Block Diagram

22.2 Registers

Table 22.3 and Table 22.4 list registers associated with UART0 to UART5.
Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART5. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART5 again.
Refer to “Registers Used and Settings” in each mode for the settings of registers and bits.

Table 22.3 Register Structure (1/2)

Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0252h	UART Clock Select Register	UCLKSEL0	X0h
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb

Table 22.4 Register Structure (2/2)

Address	Register	Symbol	Reset Value
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah 028Bh	UART5 Transmit Buffer Register	U5TB	XXh XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh 028Fh	UART5 Receive Buffer Register	U5RB	XXh XXh
0294h	UART4 Special Mode Register 4	U4SMR4	00h
0295h	UART4 Special Mode Register 3	U4SMR3	000X 0X0Xb
0296h	UART4 Special Mode Register 2	U4SMR2	X000 0000b
0297h	UART4 Special Mode Register	U4SMR	X000 0000b
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah 029Bh	UART4 Transmit Buffer Register	U4TB	XXh XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh 029Fh	UART4 Receive Buffer Register	U4RB	XXh XXh
02A4h	UART3 Special Mode Register 4	U3SMR4	00h
02A5h	UART3 Special Mode Register 3	U3SMR3	000X 0X0Xb
02A6h	UART3 Special Mode Register 2	U3SMR2	X000 0000b
02A7h	UART3 Special Mode Register	U3SMR	X000 0000b
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh 02ABh	UART3 Transmit Buffer Register	U3TB	XXh XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh 02AFh	UART3 Receive Buffer Register	U3RB	XXh XXh

22.2.1 UART Clock Select Register (UCLKSEL0)

UART Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	X	X			0	0	UCLKSEL0	0252h	X0h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
OCOSEL0	UART0 to UART2 clock prior to division select bit	0 : f1 1 : fOCO-F	RW
OCOSEL1	UART3 to UART5 clock prior to division select bit	0 : f1 1 : fOCO-F	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		—

OCOSEL0 (UART0 to UART2 clock prior to division select bit) (b2)
OCOSEL1 (UART3 to UART 5 clock prior to division select bit) (b3)

Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART5 stops.
Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART5.
After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART5 again.

22.2.2 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

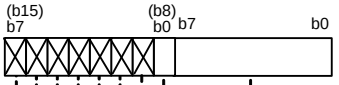
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
0	0		0	0	0			PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A, B and S clock select bit (clock source for timers A, B and S, the dead time timer, and muliti-master I^2C-bus interface)	0: f2TIMAB / f2IIC / f2TIMS 1: f1TIMAB / f1IIC / f1TIMS	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART5)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before the PCLKR register is rewritten.

22.2.3 UARTi Transmit Buffer Register (UiTB) (i = 0 to 5)

UARTi Transmit Buffer Register (i = 0 to 5)



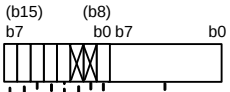
Symbol	Address	After Reset
U0TB	024Bh to 024Ah	Undefined
U1TB	025Bh to 025Ah	Undefined
U2TB	026Bh to 026Ah	Undefined
U5TB	028Bh to 028Ah	Undefined
U4TB	029Bh to 029Ah	Undefined
U3TB	02ABh to 02AAh	Undefined

Function	RW
Transmit data	WO
No register bits. If necessary, set to 0. Read as undefined value	—

Use MOV instruction to write to this register.
When character bit is 9 bits long, write in 16-bit units, or write in 8-bit units in the order of high-order bytes to low-order bytes.

22.2.4 UARTi Receive Buffer Register (UiRB) (i = 0 to 5)

UARTi Receive Buffer Register (i = 0 to 5)



Symbol	Address	After Reset
U0RB	024Fh to 024Eh	Undefined
U1RB	025Fh to 025Eh	Undefined
U2RB	026Fh to 026Eh	Undefined
U5RB	028Fh to 028Eh	Undefined
U4RB	029Fh to 029Eh	Undefined
U3RB	02AFh to 02AEh	Undefined

Bit Symbol	Bit Name	Function	RW
— (b7-b0)	——	Receive data (D7 to D0)	RO
— (b8)	——	Receive data (D8)	RO
— (b10-b9)	No register bits. If necessary, set to 0. Read as undefined value		—
ABT	Arbitration lost detect flag	0 : Not detected 1 : Detected	RW
OER	Overrun error flag	0 : No overrun error 1 : Overrun error found	RO
FER	Framing error flag	0 : No framing error 1 : Framing error found	RO
PER	Parity error flag	0 : No parity error 1 : Parity error found	RO
SUM	Error sum flag	0 : No error 1 : Error found	RO

When bits SMD2 to SMD0 in the UiMR register is 100b, 101b or 110b, read in 16-bit units, or read in 8-bit units in the order of high-order bytes to low-order bytes.
Bits FER and PER arranged in the high-order bytes become 0 when the lower bytes of the UiRB register are read.
If an overrun error occurs, the receive data of the UiRB register will be undefined.

ABT (Arbitration lost detect flag) (b11)

The ABT bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

OER (Overrun error flag) (b12)

Condition to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).

Condition to become 1:

- The RI bit in the UiC1 register is 1 (data present in UiRB register), and the last bit of the next data is received.

FER (Framing error flag) (b13)

The FER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). The read value is undefined.

Condition to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The set number of stop bits is not detected.
  (detected when the received data is transferred from the UARTi receive register to the UiRB register.)

PER (Parity error flag) (b14)

The PER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). The read value is undefined.

Condition to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The number of 1s of the parity bit and character bit does not match the set value of the PRY bit in the UiMR register.
  (detected when the received data is transferred from the UARTi receive register to the UiRB register.)

SUM (Error sum flag) (b15)

The SUM bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). The read value is undefined.

Condition to become 0:

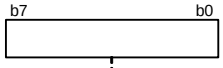
- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- All of bits PER, FER and OER are 0 (no error).

Condition to become 1:

- More than one of bits PER, FER or OER is 1 (error found).

22.2.5 UARTi Bit Rate Register (UiBRG) (i = 0 to 5)

UARTi Bit Rate Register (i = 0 to 5)



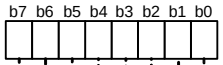
Symbol	Address	After Reset
U0BRG, U1BRG, U2BRG U5BRG, U4BRG, U3BRG	0249h, 0259h, 0269h 0289h, 0299h, 02A9h	Undefined Undefined

Function	Setting Range	RW
If set value is n, UiBRG divides the count source by n + 1	00h to FFh	WO

Write to the UiBRG register while serial interface is neither transmitting nor receiving.
Use MOV instruction to write to the UiBRG register.
Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.

22.2.6 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 to 5)

UARTi Transmit/Receive Mode Register (i = 0 to 5)

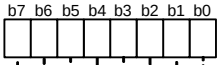


Symbol	Address	After Reset
U0MR, U1MR, U2MR U5MR, U4MR, U3MR	0248h, 0258h, 0268h 0288h, 0298h, 02A8h	00h 00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : I^2C mode 1 0 0 : UART mode character bit length is 7 bits 1 0 1 : UART mode character bit length is 8 bits 1 1 0 : UART mode character bit length is 9 bits Do not set values other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Valid when PRYE is 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TXD, RXD I/O polarity reverse bit	0 : No reverse 1 : Reverse	RW

22.2.7 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 5)

UARTi Transmit/Receive Control Register 0 (i = 0 to 5)



Symbol	Address	After Reset
U0C0, U1C0, U2C0 U5C0, U4C0, U3C0	024Ch, 025Ch, 026Ch 028Ch, 029Ch, 02ACh	0000 1000b 0000 1000b

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG count source select bit	b1 b0 0 0 : f1SIO or f2SIO selected 0 1 : f8SIO selected 1 0 : f32SIO selected 1 1 : Do not set	RW
CLK1			RW
CRS	$\overline{CTS}/\overline{RTS}$ function select bit	Valid when CRD is 0 0 : $\overline{CTS}$ function selected 1 : $\overline{RTS}$ function selected	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (transmission in progress) 1 : No data present in transmit register (transmission completed)	RO
CRD	$\overline{CTS}/\overline{RTS}$ disable bit	0 : $\overline{CTS}/\overline{RTS}$ function enabled 1 : $\overline{CTS}/\overline{RTS}$ function disabled	RW
NCH	Data output select bit	0 : Pins TXDi/SDAi and SCLi are CMOS output 1 : Pins TXDi/SDAi and SCLi are N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge 1 : Transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge	RW
UFORM	Bit order select bit	0 : LSB first 1 : MSB first	RW

CLK1 to CLK0 (UiBRG count source select bit) (b1-b0)

When bits CLK1 to CLK0 are 00b (f1SIO or f2SIO selected), select f1SIO or f2SIO by the PCLK1 bit in the PCLKR register.
Set bits CLK1 to CLK0 after setting registers UCLKSEL0 and PCLKR.
If bits CLK1 to CLK0 are changed, set the UiBRG register.

CRS ($\overline{CTS}/\overline{RTS}$ function select bit) (b2)

$\overline{CTS1}/\overline{RTS1}$ can be used when the CLKMD1 bit in the UCON register is 0 (CLK output is only from CLK1) and the RCSP bit in the UCON register is 0 ($\overline{CTS0}/\overline{RTS0}$ not separated).

CRD ($\overline{CTS}/\overline{RTS}$ disable bit) (b4)

When the CRD bit is 1 ($\overline{CTS}/\overline{RTS}$ function disabled), the $\overline{CTSi}/\overline{RTSi}$ pin can be used as an I/O port.

NCH (Data output select bit) (b5)

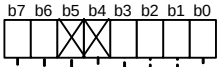
TXD2/SDA2 and SCL2 are N-channel open drain outputs. They cannot be set to CMOS output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
This function is used to set P-channel transistor of the COMS output buffer always off, but not to change pins TXDi/SDAi and SCLi to open drain output completely.
Check electrical characteristics for the input voltage range.

UFORM (Bit order select bit) (b7)

The UFORM bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), or 101b (UART mode, 8-bit character data).
Set the UFORM bit to 1 when bits SMD2 to SMD0 are 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are 100b (UART mode, 7-bit character data) or 110b (UART mode, 9-bit character data).

22.2.8 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 to 5)

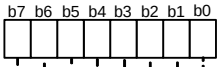
UARTi Transmit/Receive Control Register 1 (i = 0, 1)



Symbol	Address	After Reset
U0C1, U1C1	024Dh, 025Dh	00XX 0010b

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
— (b5-b4)	No register bits. If necessary, set to 0. Read as undefined value		—
UiLCH	Data logic select bit	0 : No reverse 1 : Reverse	RW
UiERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

UARTi Transmit/Receive Control Register 1 (i = 2 to 5)



Symbol	Address	After Reset
U2C1	026Dh	0000 0010b
U5C1, U4C1, U3C1	028Dh, 029Dh, 02ADh	0000 0010b

Bit symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
UiIRS	UARTi transmit interrupt source select bit	0 : UiTB register empty (TI = 1) 1 : Transmit completed (TXEPT = 1)	RW
UiRRM	UARTi continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
UiLCH	Data logic select bit	0 : No reverse 1 : Reverse	RW
UiERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

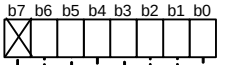
Bits UiIRS and UiRRM of UART0 and UART1 are bits in the UCON register.

UiLCH (Data logic select bit) (b6)

The UiLCH bit enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), 100b (UART mode, 7-bit character data), or 101b (UART mode, 8-bit character data). Set this bit to 0 when bits SMD2 to SMD0 are set to 010b (I^2C mode) or 110b (UART mode, 9-bit character data).

22.2.9 UART Transmit/Receive Control Register 2 (UCON)

UART Transmit/Receive Control Register 2



Symbol	Address	After Reset
UCON	0250h	X000 0000b

Bit symbol	Bit Name	Function	RW
U0IRS	UART0 transmit interrupt source select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U1IRS	UART1 transmit interrupt source select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U0RRM	UART0 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
U1RRM	UART1 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
CLKMD0	UART1CLK, CLKS select bit 0	Valid when CLKMD1 is 1 0 : Clock output from CLK1 1 : Clock output from CLKS1	RW
CLKMD1	UART1CLK, CLKS select bit 1	0 : CLK output is only from CLK1 1 : Transmit/receive clock output from multiple-pin output function selected	RW
RCSP	Separate UART0 $\overline{CTS}/\overline{RTS}$ bit	0 : $\overline{CTS}/\overline{RTS}$ shared pin 1 : $\overline{CTS}/\overline{RTS}$ separated	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

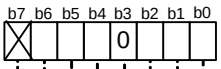
Bits UiIRS and UiRRM of UART2 to UART5 are bits in the UiC1 register.

CLKMD1 (UART1CLK, CLKS select bit 1) (b5)

When using multiple transmit/receive clock output pins, make sure the following condition is met:
the CKDIR bit in the U1MR register = 0 (internal clock)

22.2.10 UARTi Special Mode Register (UiSMR) (i = 0 to 5)

UARTi Special Mode Register (i = 0 to 5)



Symbol	Address	After Reset
U0SMR, U1SMR, U2SMR U5SMR, U4SMR, U3SMR	0247h, 0257h, 0267h 0287h, 0297h, 02A7h	X000 0000b X000 0000b

Bit Symbol	Bit Name	Function	RW
IICM	I^2C mode select bit	0 : Other than I^2C mode 1 : I^2C mode	RW
ABC	Arbitration lost detect flag control bit	0 : Update per bit 1 : Update per byte	RW
BBS	Bus busy flag	0 : Stop-condition detected 1 : Start-condition detected (busy)	RW
— (b3)	Reserved bit	Set to 0	RW
ABSCS	Bus collision detect sampling clock select bit	0 : Rising edge of transmit/receive clock 1 : Underflow signal of timer Aj	RW
ACSE	Auto clear function select bit of transmit enable bit	0 : No auto clear function 1 : Auto clear at occurrence of bus collision	RW
SSS	Transmit start condition select bit	0 : Not synchronized to RXDi 1 : Synchronized to RXDi	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

BBS (Bus busy flag) (b2)

The BBS bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

ABSCS (Bus collision detect sampling clock select bit) (b4)

When the ABSCS bit is 1, the combinations of UARTi and timer Aj are as follows:

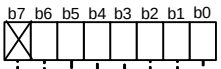
UART0, UART4: Underflow signal of timer A3
UART1, UART3: Underflow signal of timer A4
UART2, UART5: Underflow signal of timer A0

SSS (Transmit start condition select bit) (b6)

When a transmit starts, the SSS bit is set to 0 (not synchronized to RXDi).

22.2.11 UARTi Special Mode Register 2 (UiSMR2) (i = 0 to 5)

UARTi Special Mode Register 2 (i = 0 to 5)

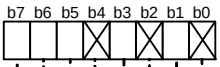


Symbol	Address	After Reset
U0SMR2, U1SMR2, U2SMR2 U5SMR2, U4SMR2, U3SMR2	0246h, 0256h, 0266h 0286h, 0296h, 02A6h	X000 0000b X000 0000b

Bit Symbol	Bit Name	Function	RW
IICM2	I^2C mode select bit 2	See table 23.18 "I^2C Mode Functions"	RW
CSC	Clock synchronization bit	0 : Disabled 1 : Enabled	RW
SWC	SCL wait output bit	0 : Disabled 1 : Enabled	RW
ALS	SDA output stop bit	0 : Disabled 1 : Enabled	RW
STAC	UARTi initialization bit	0 : Disabled 1 : Enabled	RW
SWC2	SCL wait output bit 2	0: Transmit/receive clock 1: Low-level output	RW
SDHI	SDA output disable bit	0: Enabled 1: Disabled (high-impedance)	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

22.2.12 UARTi Special Mode Register 3 (UiSMR3) (i = 0 to 5)

UARTi Special Mode Register 3 (i = 0 to 5)



Symbol	Address	After Reset
U0SMR3, U1SMR3, U2SMR3 U5SMR3, U4SMR3, U3SMR3	0245h, 0255h, 0265h 0285h, 0295h, 02A5h	000X 0X0Xb 000X 0X0Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value		—
CKPH	Clock phase set bit	0 : No clock delay 1 : With clock delay	RW
— (b2)	No register bit. If necessary, set to 0. Read as undefined value		—
NODC	Clock output select bit	0 : CLKi is CMOS output 1 : CLKi is N-channel open drain output	RW
— (b4)	No register bit. If necessary, set to 0. Read as undefined value		—
DL0	SDAi digital delay setup bit	b7 b6 b5 0 0 0 : No delay 0 0 1 : 1 to 2 cycle(s) of UiBRG count source 0 1 0 : 2 to 3 cycles of UiBRG count source 0 1 1 : 3 to 4 cycles of UiBRG count source 1 0 0 : 4 to 5 cycles of UiBRG count source 1 0 1 : 5 to 6 cycles of UiBRG count source 1 1 0 : 6 to 7 cycles of UiBRG count source 1 1 1 : 7 to 8 cycles of UiBRG count source	RW
DL1			RW
DL2			RW

DL2-DL0 (SDAi digital delay setup bit) (b7-b5)

Bits DL2 to DL0 are used to generate a delay in SDAi output by digital means in I^2C mode. Except for I^2C mode, set these bits to 000b (no delay).
The amount of delay varies with the load on pins SCLi and SDAi. Also, when using an external clock, the amount of delay increases by about 100 ns.

NODC (Clock output select bit) (b3)

This function is used to set P-channel transistor of the COMS output buffer always off, but not to change the CLKi pin to open drain output completely.
Check electrical characteristics for the input voltage range.

22.2.13 UARTi Special Mode Register 4 (UiSMR4) (i = 0 to 5)

UARTi Special Mode Register 4 (i = 0 to 5)

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
	U0SMR4, U1SMR4, U2SMR4	0244h, 0254h, 0264h	00h
	U5SMR4, U4SMR4, U3SMR4	0284h, 0294h, 02A4h	00h

Bit Symbol	Bit Name	Function	RW
STAREQ	Start condition generate bit	0 : Clear 1 : Start	RW
RSTAREQ	Restart condition generate bit	0 : Clear 1 : Start	RW
STPREQ	Stop condition generate bit	0 : Clear 1 : Start	RW
STSPSEL	SCL, SDA output select bit	0 : Start and stop conditions not output 1 : Start and stop conditions output	RW
ACKD	ACK data bit	0 : ACK 1 : NACK	RW
ACKC	ACK data output enable bit	0 : Serial interface data output 1 : ACK data output	RW
SCLHI	SCL output stop enable bit	0 : Disabled 1 : Enabled	RW
SWC9	SCL wait bit 3	0 : SCL low hold disabled 1 : SCL low hold enabled	RW

STAREQ (Start condition generate bit) (b0)

The STAREQ bit becomes 0 when the start condition is generated.

RSTAREQ (Restart condition generate bit) (b1)

The RSTAREQ bit becomes 0 when the restart condition is generated.

STPREQ (Stop condition generate bit) (b2)

The STPREQ bit becomes 0 when the stop condition is generated.

22.3 Operations

22.3.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transmit/receive clock to transmit/receive data. Table 22.5 lists the Clock Synchronous Serial I/O Mode Specifications.

Table 22.5 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Data format	Character bit length: 8 bits
Transmit/receive clock	• CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n = Setting value of UiBRG register 00h to FFh • CKDIR bit = 1 (external clock): Input from CLKi pin
Transmission and reception control	Selectable from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}/\overline{RTS}$ function disabled
Transmission start conditions	To start transmission, satisfy the following requirements (1) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in UiTB register) • If $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.
Reception start conditions	To start reception, satisfy the following requirements (1) • The RE bit in the UiC1 register = 1 (reception enabled) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in the UiTB register)
Interrupt request generation timing	Transmit interrupt: One of the following can be selected. • The UiIRS bit = 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit =1 (transmission completed): When the serial interface completed sending data from the UARTi transmit register Receive interrupt: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	Overrun error (2) This error occurs if the serial interface started receiving the next unit of data before reading the UiRB register and received the 7th bit of the next unit of data
Selectable functions	• CLK polarity selection Data input/output can be selected to occur synchronously with the rising or the falling edge of the transmit/receive clock • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register • Switching serial data logic This function reverses the logic value of the transmit/receive data • Transmit/receive clock output from multiple pins selection (UART1) The output pin can be selected by a program by setting two UART1 transmit/receive clock pins. • Separate $\overline{CTS}/\overline{RTS}$ pins (UART0) $\overline{CTS0}$ and $\overline{RTS0}$ are input/output from separate pins

i = 0 to 5

Notes:

1. When an external clock is selected, either of the following conditions must be met: If the CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register is 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transmit/receive clock), the external clock is in the low state.
2. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 22.6 lists Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transmit/Receive Clock Output Pin Function Not Selected). Table 22.7 lists P6_4 Pin Functions in Clock Synchronous Serial I/O Mode.
Note that for a period from when UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open drain output is selected, this pin is in high-impedance state.)

Table 22.6 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transmit/Receive Clock Output Pin Function Not Selected)

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(Outputs dummy data when performing reception only.)
RXDi	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits to 0. (can be used as an input port when performing transmission only)
CLKi	Output	Transmit/receive clock output	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bits sharing pins to 0.
$\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bits sharing pins to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	Input/ output	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 5

Table 22.7 P6_4 Pin Functions in Clock Synchronous Serial I/O Mode

Pin Function	Bit Set Value					
	U1C0 Register		UCON Register			PD6 Register
	CRD	CRS	RCSP	CLKMD1	CLKMD0	PD6_4
P6_4	1	-	0	0	-	Input: 0, Output: 1
$\overline{\text{CTS1}}$	0	0	0	0	-	0
$\overline{\text{RTS1}}$	0	1	0	0	-	-
$\overline{\text{CTS0}}$ (1)	0	0	1	0	-	0
CLKS1	-	-	-	1 (2)	1	-

- indicates either 0 or 1

Notes:

1. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS0}}$ selected).
2. When the CLKMD1 bit is 1 and the CLKMD0 bit is 0, the following logic levels are output.
   - High if the CLKPOL bit in the U1C0 register is 0
   - Low if the CLKPOL bit in the U1C0 register is 1

Table 22.8 and Table 22.9 list the registers used and settings in clock synchronous serial i/o mode.

Table 22.8 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1/2) (1)

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART5.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 7	Set transmission data
	8	- (does not need to be set) If necessary, set to 0.
UiRB	0 to 7	Reception data can be read.
	8, 11, 13 to 15	When read, the read value is undefined.
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
	4 to 6	Set to 0.
	IOPOL	Set to 0.
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function.
	NCH	Select TXDi pin output mode. (2)
	CKPOL	Select the transmit/receive clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS	Select source of UARTj transmit interrupt.
	UjRRM	Set to 1 to use continuous receive mode.
	UiLCH	Set to 1 to use inverted data logic.
	UiERE	Set to 0.
UiSMR	0 to 7	Set to 0.
UiSMR2	0 to 7	Set to 0.
UiSMR3	0 to 2	Set to 0.
	NODC	Select clock output mode.
	4 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.

i = 0 to 5 j = 2 to 5

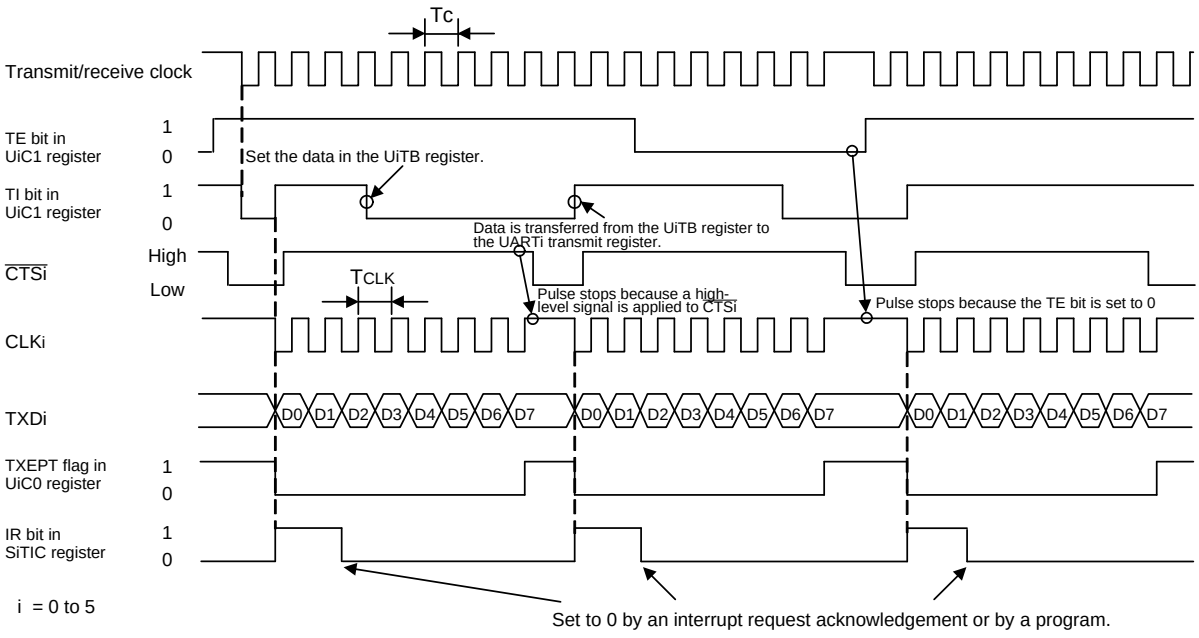
Notes:
1. This table does not describe a procedure.
2. The TXD2 pin is N channel open drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.

Table 22.9 Registers Used and Settings in Clock Synchronous Serial I/O Mode (2/2) (1)

UCON	U0IRS	Select source of UART0 transmit interrupt.
	U1IRS	Select source of UART1 transmit interrupt.
	U0RRM	Set to 1 to use continuous receive mode.
	U1RRM	Set to 1 to use continuous receive mode.
	CLKMD0	Select the transmit/receive clock output pin when CLKMD1 is 1.
	CLKMD1	Set to 1 to output UART1 transmit/receive clock from two pins.
	RCSP	Set to 1 to separate the $\overline{\text{CTS0}}$/$\overline{\text{RTS}}$ signal of UART0.
	7	Set to 0.

Note:
1. This table does not describe a procedure.

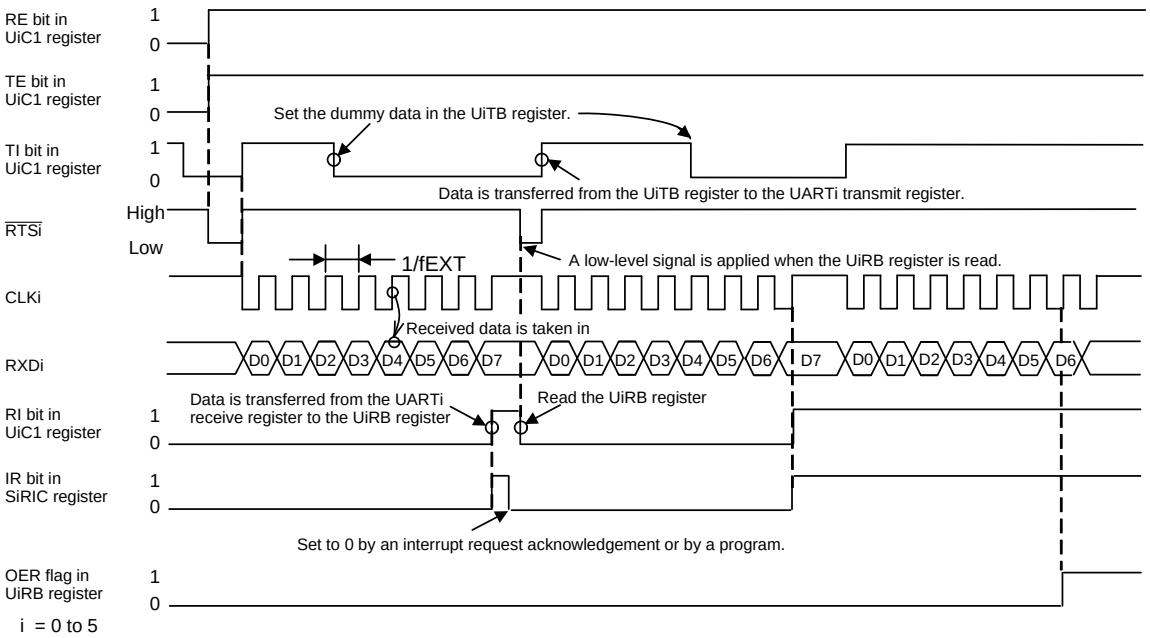
(1) Example of Transmit Timing (Internal Clock Selected)



The above timing diagram applies when the register bits are set as follows:
- The CKDIR bit in the UiMR register = 0 (internal clock)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled), the CRS bit = 0 (CTS selected)
- The CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transmit/receive clock)
- The UiIRS bit in the UiC1 register = 0 (an interrupt request occurs when the UiTB register becomes empty)

$T_C = T_{CLK} = 2(n + 1)/fj$
fj: Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
n: Value set to the UiBRG register

(2) Example of Receive Timing (External Clock Selected)



The above timing diagram applies to the case where the register bits are set as follows:
- The CKDIR bit in the UiMR register = 1 (external clock)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled), the CRS bit = 1 (RTS selected)
- The CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transmit/receive clock)

fEXT: Frequency of the external clock

Make sure the following conditions are met when input to the CLKi pin before receiving data is high:
- The TE bit in the UiC1 register = 1 (transmit enabled)
- The RE bit in the UiC1 register = 1 (receive enabled)
- Write dummy data to the UiTB register

Figure 22.5 Transmit/Receive Operation during Clock Synchronous Serial I/O Mode

22.3.1.1 Transmit/Receive Register Initialization

When the transmit/receive register needs to be initialized due to an interrupted transmission/reception, follow the procedures below.

- Initializing the UiRB register (i = 0 to 5)
  (1) Set the RE bit in the UiC1 register to 0 (reception disabled).
  (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
  (3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
  (4) Set the RE bit in the UiC1 register to 1 (reception enabled).

- Initializing the UiTB register (i = 0 to 5)
  (1) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
  (2) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
  (3) Write a 1 to the RE bit in the UiC1 register (transmission enabled), regardless of the value of the TE bit in the UiCi register.

22.3.1.2 CLK Polarity Select Function

Use the CKPOL bit in the UiC0 register (i = 0 to 5) to select the transmit/receive clock polarity. Figure 22.6 shows the Transmit/Receive Clock Polarity.

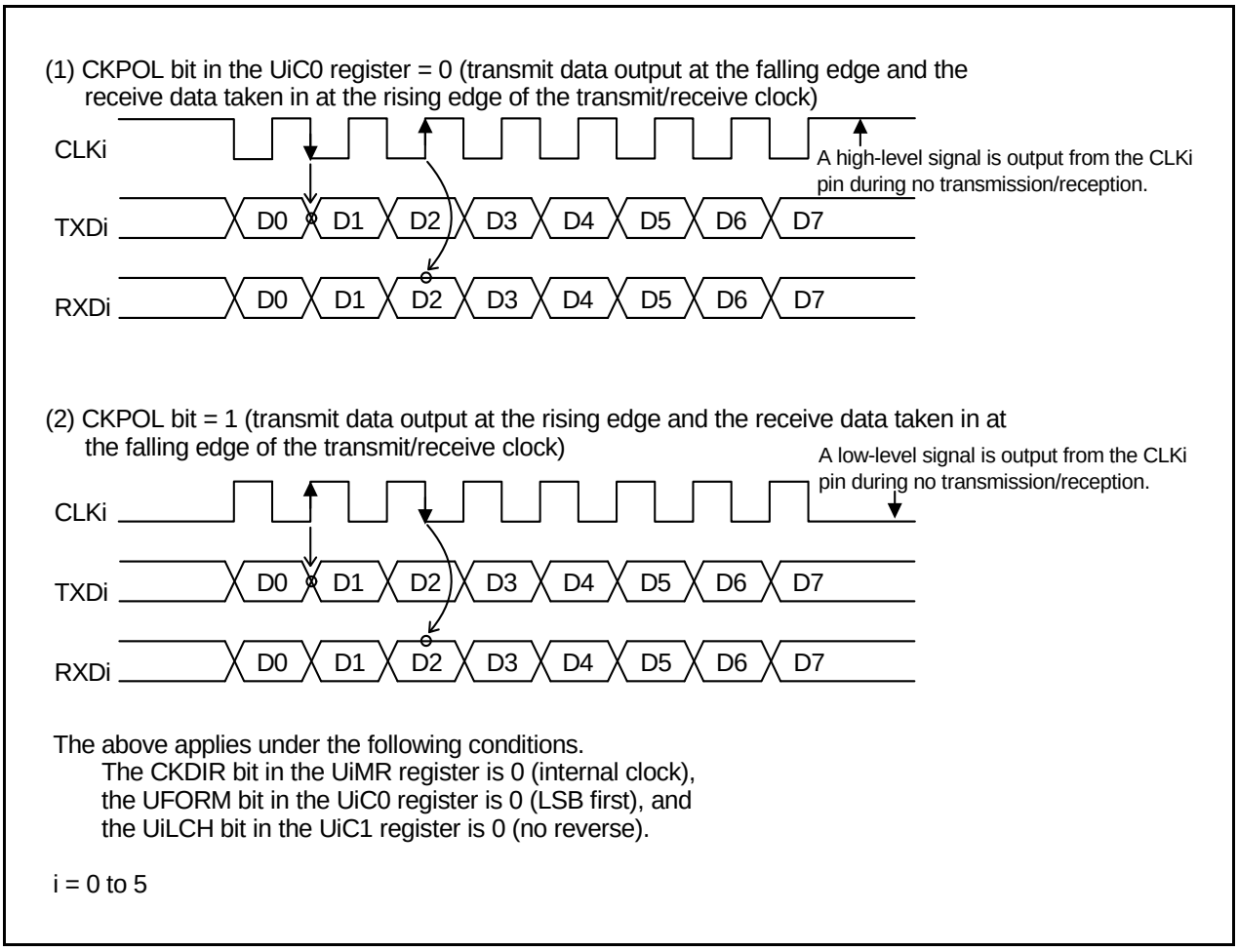
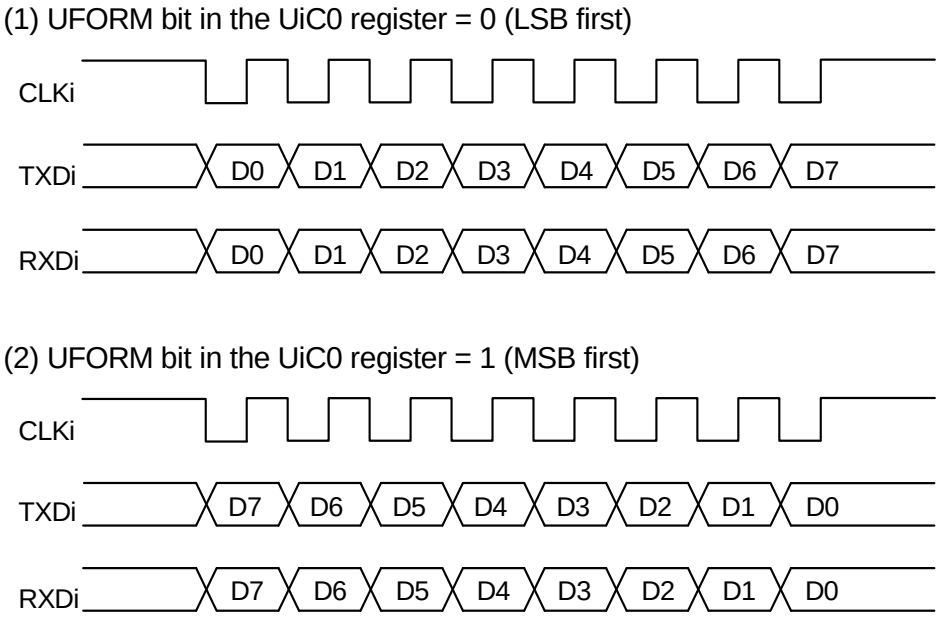


Figure 22.6 Transmit/Receive Clock Polarity

22.3.1.3 LSB First/MSB First Select Function

Use the UFORM bit in the UiC0 register (i = 0 to 5) to select the bit order. Figure 22.7 shows the Bit Order.



The above applies under the following conditions.
The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock), and the UiLCH bit in the UiC1 register is 0 (no reverse).

i = 0 to 5

Figure 22.7 Bit Order

22.3.1.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the UiRRM bit (i = 0 to 5) is 1 (continuous receive mode), the TI bit in the UiC1 register is set to 0 (data present in the UiTB register) by reading the UiRB register. In this case (UiRRM bit = 1), do not write dummy data to the UiTB register by a program.

When using an external clock, read the UiRB register between the eighth bit of data is received and the next transmission starts.

Figure 22.8 shows Operation Example in Continuous Receive Mode.

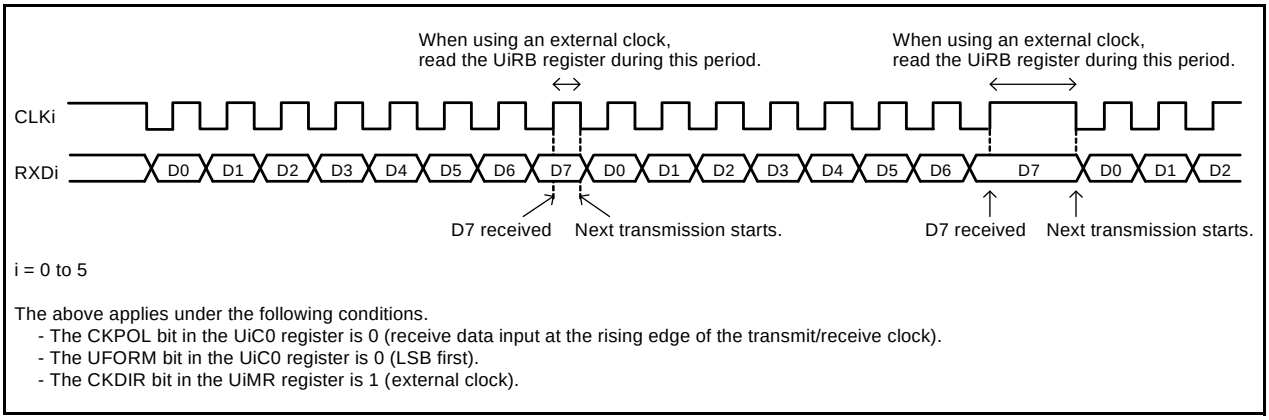


Figure 22.8 Operation Example in Continuous Receive Mode

22.3.1.5 Serial Data Logic Switching Function

When the UiLCH bit in the UiC1 register (i = 0 to 5) is 1 (reverse), the data written to the UiTB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the UiRB register. Figure 22.9 shows Serial Data Logic.

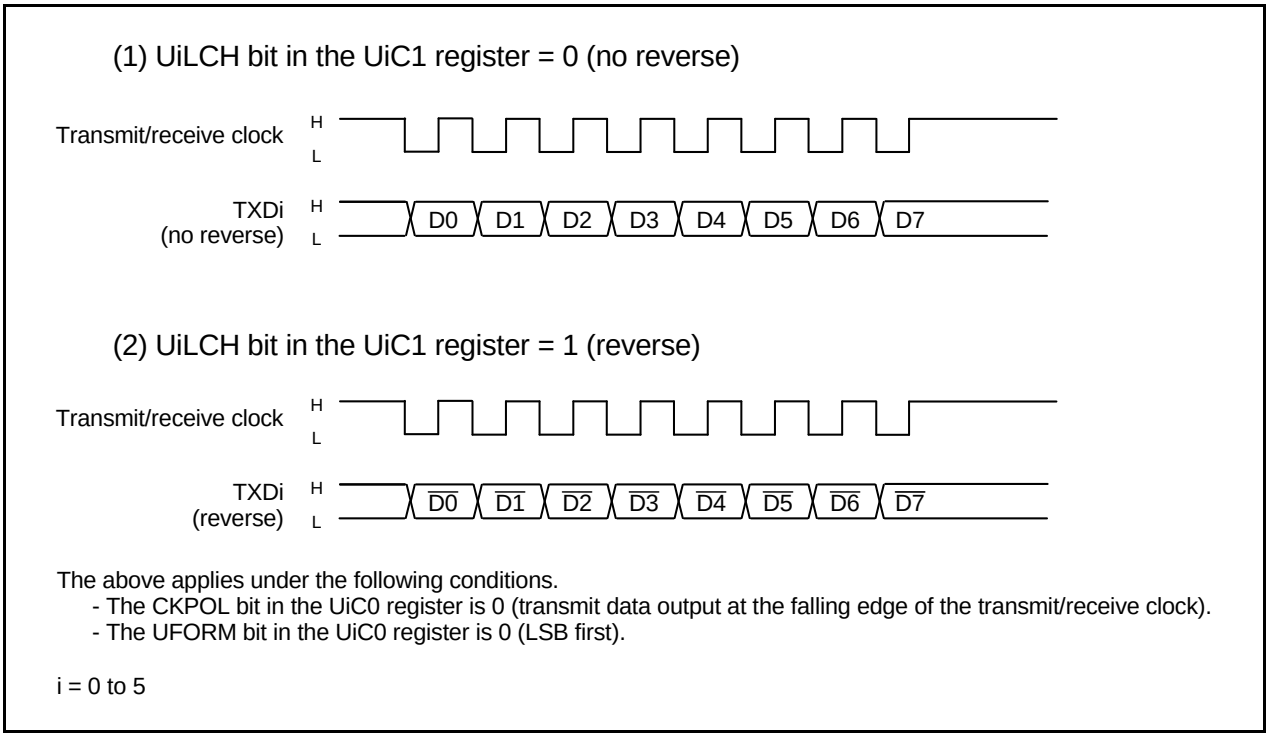


Figure 22.9 Serial Data Logic

22.3.1.6 Transmit/Receive Clock Output from Multiple Pins (UART1)

Use bits CLKMD1 to CLKMD0 in the UCON register to select one of the two transmit/receive clock output pins (see Figure 22.10). This function can be used when the selected transmit/receive clock for UART1 is an internal clock.

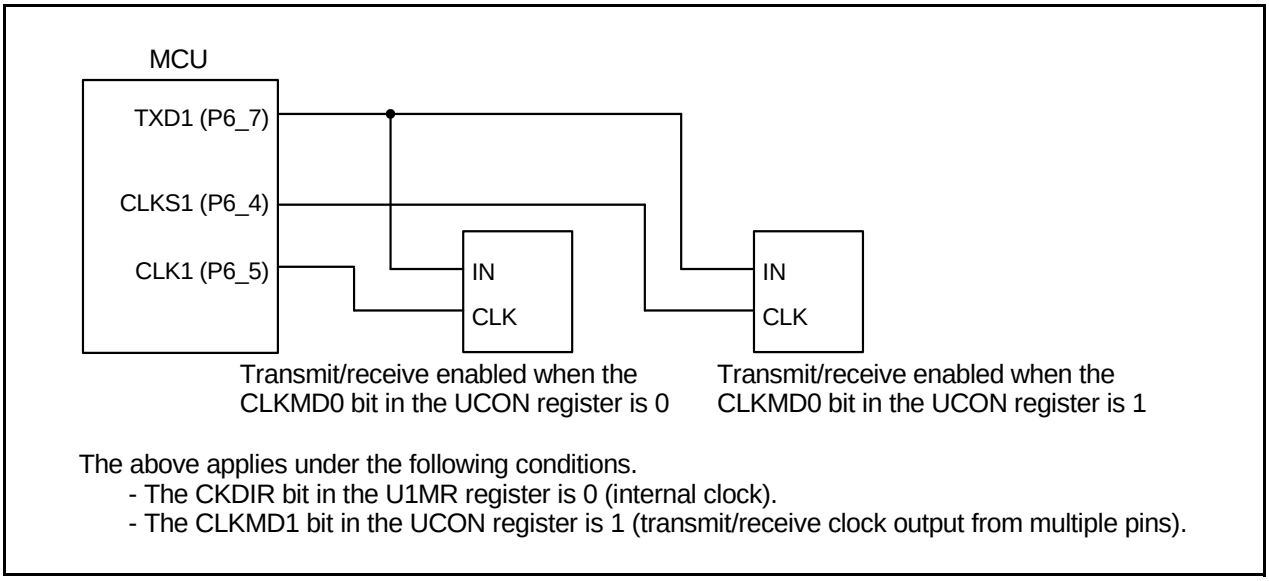


Figure 22.10 Transmit/Receive Clock Output from Multiple Pins

22.3.1.7 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit/receive operation when a low-level signal is applied to the $\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i (i = 0 to 5) pin. Transmit/receive operation begins when input to the $\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i pin becomes low. If the low-level signal is switched to high during a transmit or receive operation, the operation stops before the next data.

For the $\overline{\text{RTS}}$ function, the $\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i pin outputs a low-level signal when the MCU is ready to receive. The output level goes high on the first falling edge of the CLKi pin.

Refer to Table 22.6 “Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transmit/Receive Clock Output Pin Function Not Selected)”.

22.3.1.8 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Separate Function (UART0)

This function separates $\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and inputs $\overline{\text{CTS0}}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register= 0 (enable $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ of UART0)
- The CRS bit in the U0C0 register= 1 (output $\overline{\text{RTS}}$ of UART0)
- The CRD bit in the U1C0 register= 0 (enable $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ of UART1)
- The CRS bit in the U1C0 register= 0 (input $\overline{\text{CTS}}$ of UART1)
- The RCSP bit in the UCON register= 1 (inputs $\overline{\text{CTS0}}$ from the P6_4 pin)
- The CLKMD1 bit in the UCON register= 0 (CLKS1 not used)

Note that when using the $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ separate function, $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ of UART1 function cannot be used.

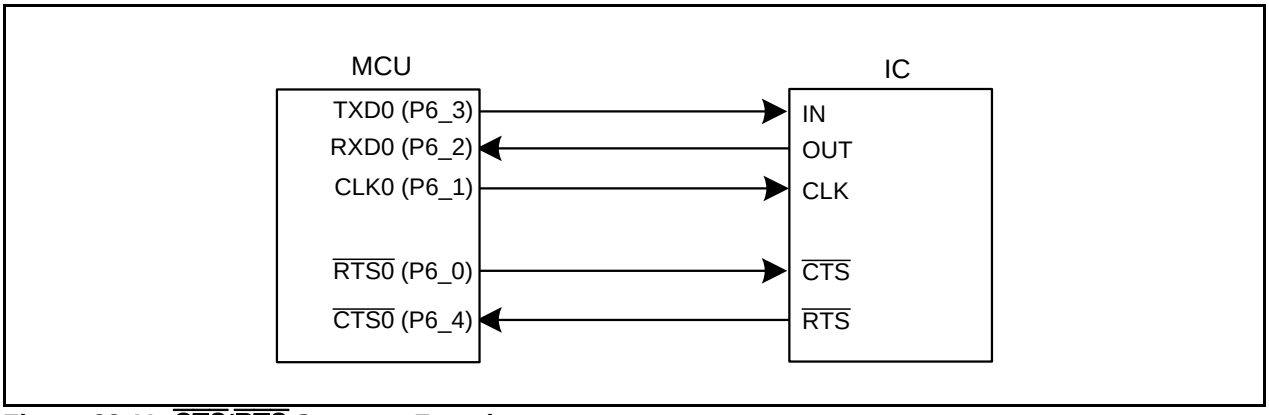


Figure 22.11 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Separate Function

22.3.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows transmitting and receiving data after setting the desired bit rate and bit order. Table 22.10 lists the UART Mode Specifications.

Table 22.10 UART Mode Specifications

Item	Specification
Data format	• Character bits : Selectable from 7, 8, or 9 bits • Start bit : 1 bit • Parity bit : Selectable from odd, even, or none • Stop bit : Selectable from 1 bit or 2 bits
Transmit/receive clock	• The CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{16(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh • CKDIR bit = 1 (external clock): $\frac{fEXT}{16(n+1)}$ fEXT: Input from CLKi pin n: Setting value of UiBRG register 00h to FFh
Transmission and reception control	Selectable from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}$/$\overline{RTS}$ function disabled
Transmission start conditions	To start transmission, satisfy the following requirements. • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in the UiTB register) • If $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.
Reception start conditions	To start reception, satisfy the following requirements. • The RE bit in the UiC1 register = 1 (reception enabled) • Start bit detection
Interrupt request generation timing	Transmit interrupt: One of the following can be selected. • The UiIRS bit = 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit =1 (transmission completed): When the serial interface completes sending data from the UARTi transmit register Receive interrupt: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the number of stop bits set is not detected • Parity error This error occurs when the number of 1s of the parity bit and character bit does not match the set value of the PRY bit in the UiMR register. • Error sum flag This flag is set to 1 when an overrun, framing, or parity error occurs.
Selectable functions	• LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Serial data logic switch This function reverses the logic of the transmit/receive data. The start and stop bits are not reversed. • TXD, RXD I/O polarity switch This function reverses the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are reversed. • Separate $\overline{CTS}$/$\overline{RTS}$ pins (UART0) $\overline{CTS0}$ and $\overline{RTS0}$ are input/output from separate pins.

i = 0 to 5

Note:

1. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 22.11 lists I/O Pin Functions in UART Mode. Table 22.12 lists the P6_4 Pin Functions in UART Mode. Note that for a period from when the UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open drain output is selected, this pin is in high-impedance state.)

Table 22.11 I/O Pin Functions in UART Mode

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(High-level output when performing reception only.)
RXDi	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits sharing pins to 0. (can be used as an input port when performing transmission only)
CLKi	Input/ output	Input/output port	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bits sharing pins to 0.
$\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bits sharing pins to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	Input/ output	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 5

Table 22.12 P6_4 Pin Functions in UART Mode

Pin Function	Bit Set Value				
	U1C0 Register		UCON Register		PD6 Register
	CRD	CRS	RCSP	CLKMD1	PD6_4
P6_4	1	-	0	0	Input: 0, Output: 1
$\overline{\text{CTS1}}$	0	0	0	0	0
$\overline{\text{RTS1}}$	0	1	0	0	-
$\overline{\text{CTS0}}$ (1)	0	0	1	0	0

– indicates either 0 or1.

Note:

1. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS0}}$ selected).

Table 22.13 and Table 22.14 list the registers used and settings in uart mode.

Table 22.13 Registers Used and Settings in UART Mode (1/2) (1)

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART5.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 8	Set transmission data. (2)
UiRB	0 to 8	Reception data can be read. (2, 4)
	OER, FER, PER, SUM	Error flag
	11	When read, the read value is undefined.
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 100b when character bit length is 7 bits.
		Set to 101b when character bit length is 8 bits.
		Set to 110b when character bit length is 9 bits.
	CKDIR	Select the internal clock or external clock.
	STPS	Select number of stop bits.
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the TXD/RXD input/output polarity.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function.
	NCH	Select TXDi pin output mode. (3)
	CKPOL	Set to 0.
	UFORM	LSB first or MSB first can be selected when character bit length is 8 bits. Set to 0 when character bit length is 7 or 9 bits.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS	Select source of UARTj transmit interrupt.
	UjRRM	Set to 0.
	UiLCH	Set to 1 to use reversed data logic.
	UiERE	Set to 0.
UiSMR	0 to 7	Set to 0.
UiSMR2	0 to 7	Set to 0.
UiSMR3	0 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.

i = 0 to 5 j = 2 to 5

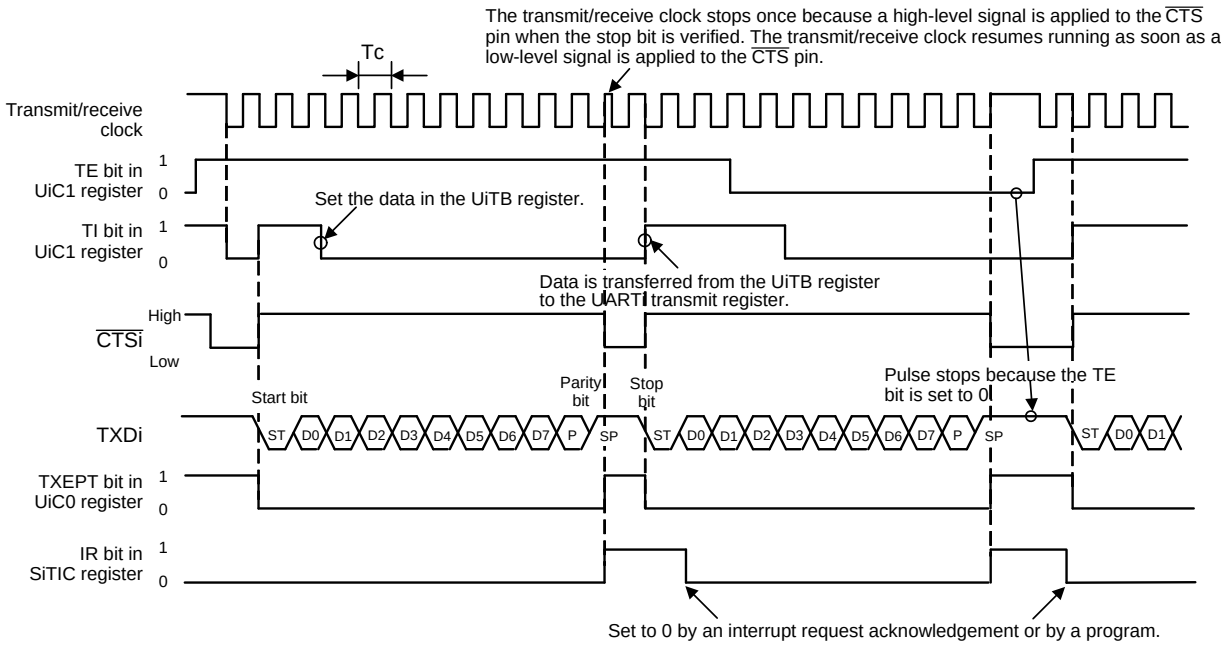
Notes:
1. This table does not describe a procedure.
2. The bits used for transmit/receive data are as follows: Bits 0 to 6 when character bit length is 7 bits; bits 0 to 7 when character bit length is 8 bits; bits 0 to 8 when character bit length is 9 bits.
3. TXD2 pin is N-channel open drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
4. The contents of bits 7 and 8 are undefined when character bit length is 7 bits. The contents of bit 8 is undefined when character bit length is 8 bits.

Table 22.14 Registers Used and Settings in UART Mode (2/2) (1)

UCON	U0IRS	Select source of UART0 transmit interrupt.
	U1IRS	Select source of UART1 transmit interrupt.
	U0RRM	Set to 0.
	U1RRM	Set to 0.
	CLKMD0	Invalid because CLKMD1 is 0
	CLKMD1	Set to 0.
	RCSP	Set to 1 to input $\overline{\text{CTS0}}$ signal of UART0 from the P6_4 pin.
	7	Set to 0.

Note:
1. This table does not describe a procedure.

(1) 8-bit Data Transmit Timing (with a Parity and 1 Stop Bit)

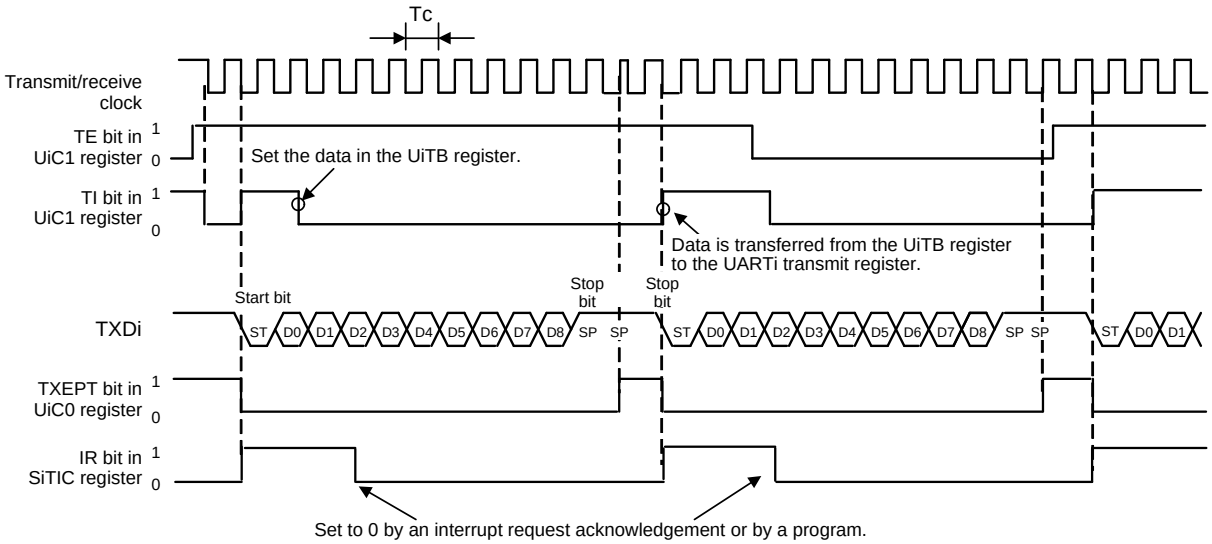


i = 0 to 5

The above timing diagram applies when the register bits are set as follows:
- The PRYE bit in the UiMR register = 1 (parity enabled)
- The STPS bit in the UiMR register = 0 (1 stop bit)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled)
- The CRS bit in the UiC0 register = 0 (CTS selected)
- The UiIRS bit in the UiC1 register = 1 (an interrupt request occurs when transmit completed)

Tc = 16(n + 1)/fj or 16(n + 1)/fEXT
fj : Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT : Frequency of UiBRG count source (external clock)
n : Value set to UiBRG

(2) 9-bit Data Transmit Timing (with No Parity and 2 Stop Bits)



i = 0 to 5

The above timing diagram applies when the register bits are set as follows:
- The PRYE bit in the UiMR register = 0 (parity disabled)
- The STPS bit in the UiMR register = 1 (2 stop bits)
- The CRD bit in the UiC0 register = 1 (CTS/RTS disabled)
- The UiIRS bit in the UiC1 register = 0 (an interrupt request occurs when transmit buffer becomes empty)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj : Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: Frequency of UiBRG count source (external clock)
n : Value set to UiBRG

Figure 22.12 Transmit Timing in UART Mode

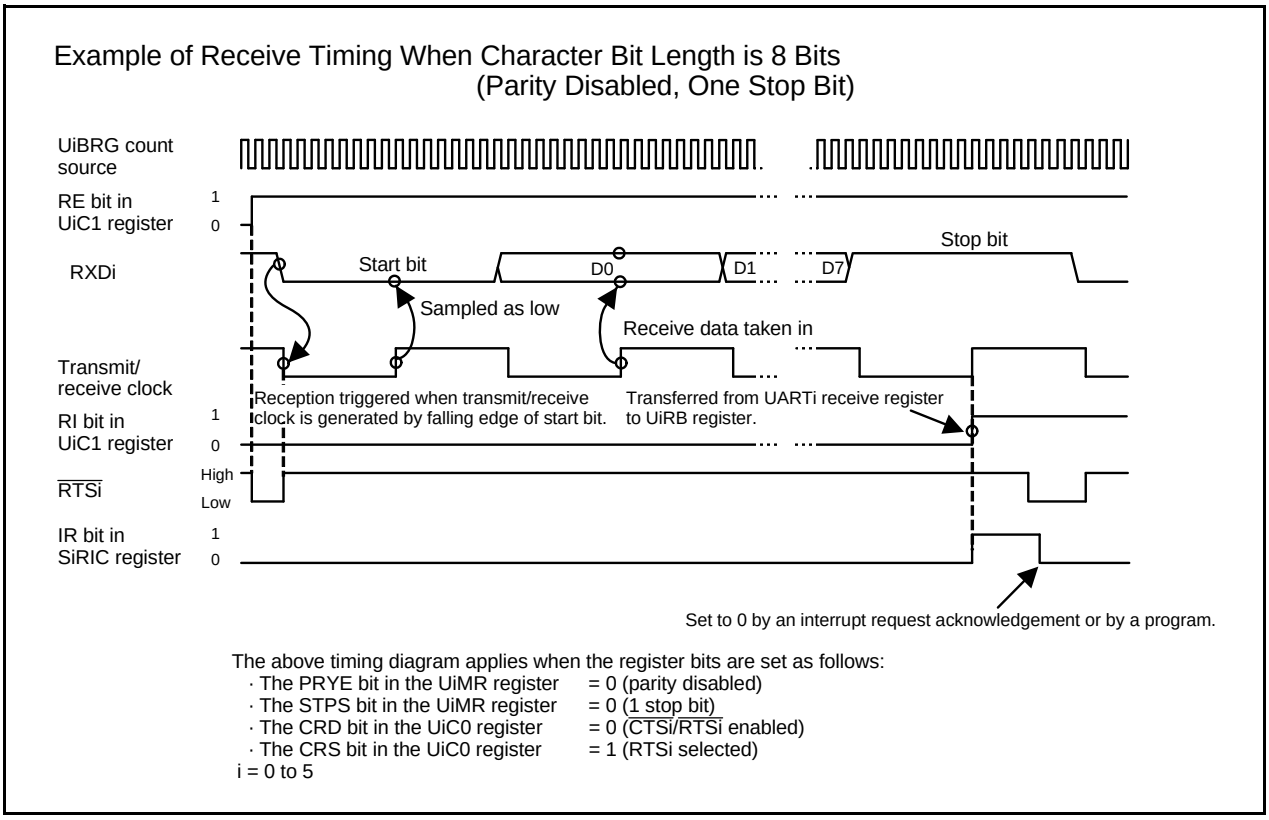


Figure 22.13 Receive Timing in UART Mode

22.3.2.1 Bit Rate

In UART mode, the frequency set by the UiBRG register (i = 0 to 5) divided by 16 become the bit rate. The setting value (n) of the UiBRG register is calculated by the following formula.

$$n = \frac{fj}{bitrate(bps) \times 16} - 1$$

fj = f1SIO, f2SIO, f8SIO, f32SIO

n = 00h to FFh

Table 22.15 lists Example Bit Rates and Settings.

Table 22.15 Example Bit Rates and Settings

Bit Rate (bps)	Count Source of UiBRG	Peripheral Function Clock f1: 16 MHz		Peripheral Function Clock f1: 24 MHz	
		Set Value of UiBRG: n	Bit Rate (bps)	Set value of UiBRG: n	Bit Rate (bps)
1200	f8SIO	103 (67h)	1202	155 (9Bh)	1202
2400	f8SIO	51 (33h)	2404	77 (4Dh)	2404
4800	f8SIO	25 (19h)	4808	38 (26h)	4808
9600	f1SIO	103 (67h)	9615	155 (9Bh)	9615
14400	f1SIO	68 (44h)	14493	103 (67h)	14423
19200	f1SIO	51 (33h)	19231	77 (4Dh)	19231
28800	f1SIO	34 (22h)	28571	51 (33h)	28846
31250	f1SIO	31 (1Fh)	31250	47 (2Fh)	31250
38400	f1SIO	25 (19h)	38462	38 (26h)	38462
51200	f1SIO	19 (13h)	50000	28 (1Ch)	51724

Note:

1. This applies when the OCOSEL0 bit or OCOSEL1 bit in the UCLKSEL0 register is 0 (f1).

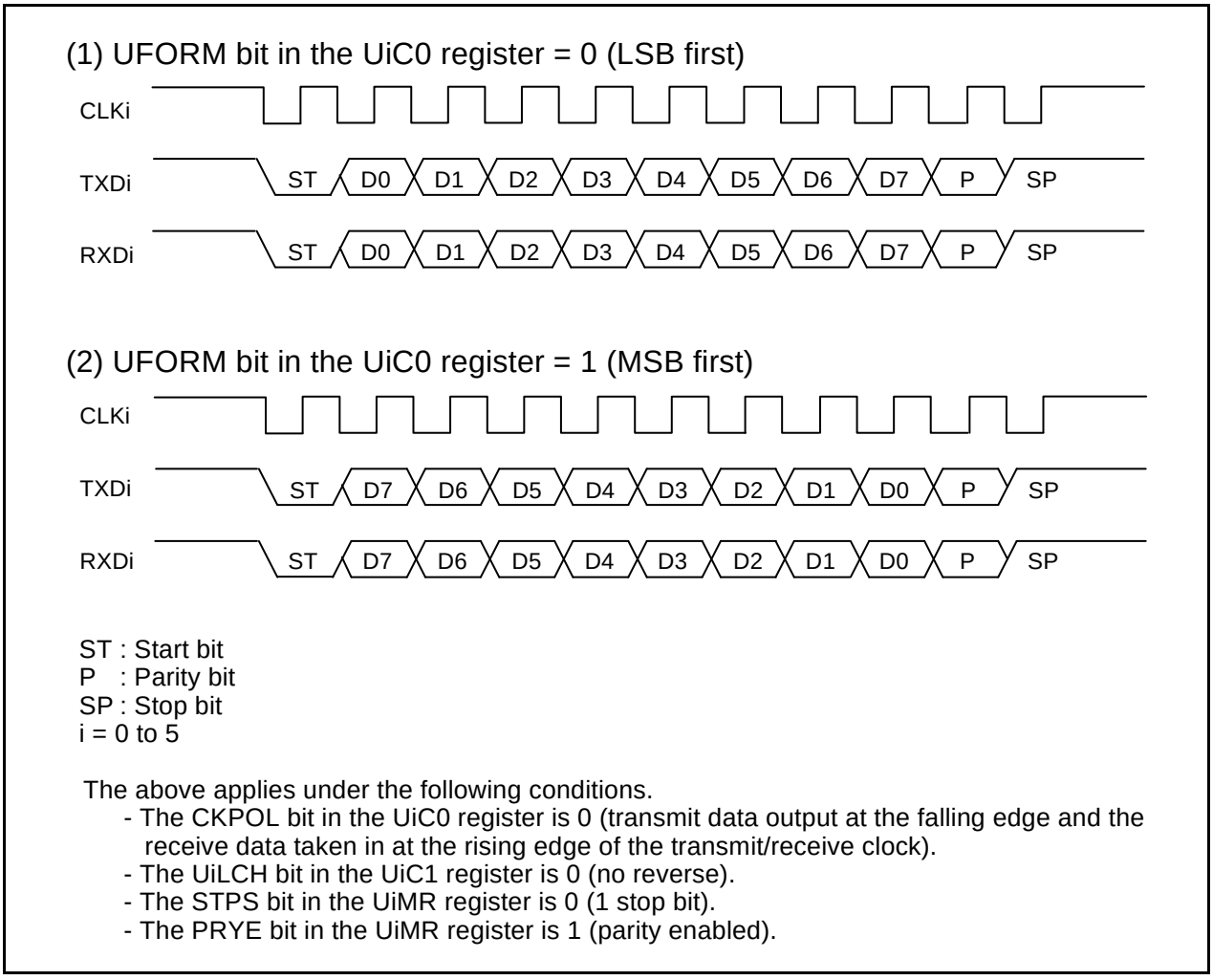
22.3.2.2 Transmit/Receive Register Initialization

When the transmit/receive register needs to be initialized due to an interrupted transmission/reception, follow the procedures below.

- Initializing the UiRB register (i = 0 to 5)
  (1) Set the RE bit in the UiC1 register to 0 (reception disabled).
  (2) Set the RE bit in the UiC1 register to 1 (reception enabled).
- Initializing the UiTB register
  (1) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
  (2) Reset bits SMD2 to SMD0 in the UiMR register to 001b, 101b, and 110b.
  (3) Set 1 (transmission enabled), regardless of the set value of the TE bit in the UiC1 register.

22.3.2.3 LSB First/MSB First Select Function

As shown in Figure 22.14, the bit order can be selected by using the UFORM bit in the UiC0 register. This function is valid when the character bit length is 8 bits.



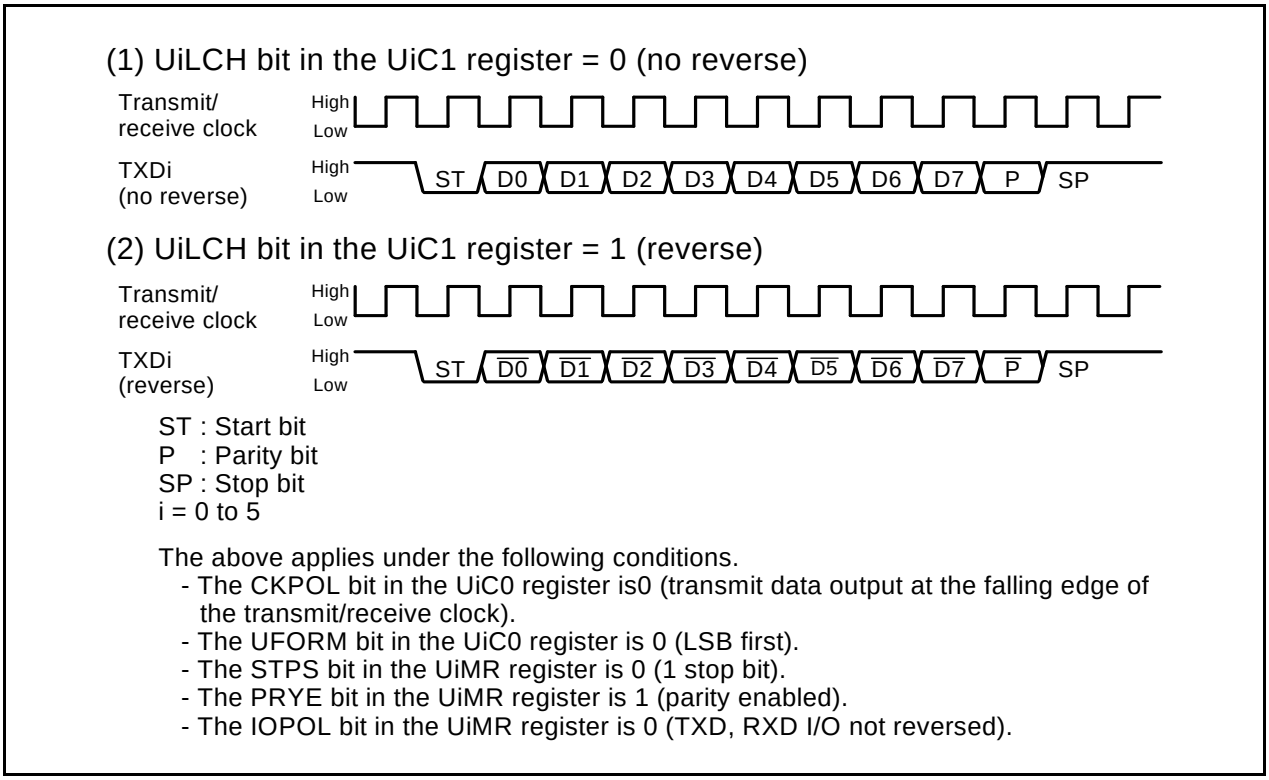
ST : Start bit
P : Parity bit
SP : Stop bit
i = 0 to 5

The above applies under the following conditions.
- The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock).
- The UiLCH bit in the UiC1 register is 0 (no reverse).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).

Figure 22.14 Bit Order

22.3.2.4 Serial Data Logic Switching Function

The logic of the data written to the UiTB register is reversed and then transmitted. Similarly, the reversed logic of the received data is read when the UiRB register is read. Figure 22.15 shows Serial Data Logic.



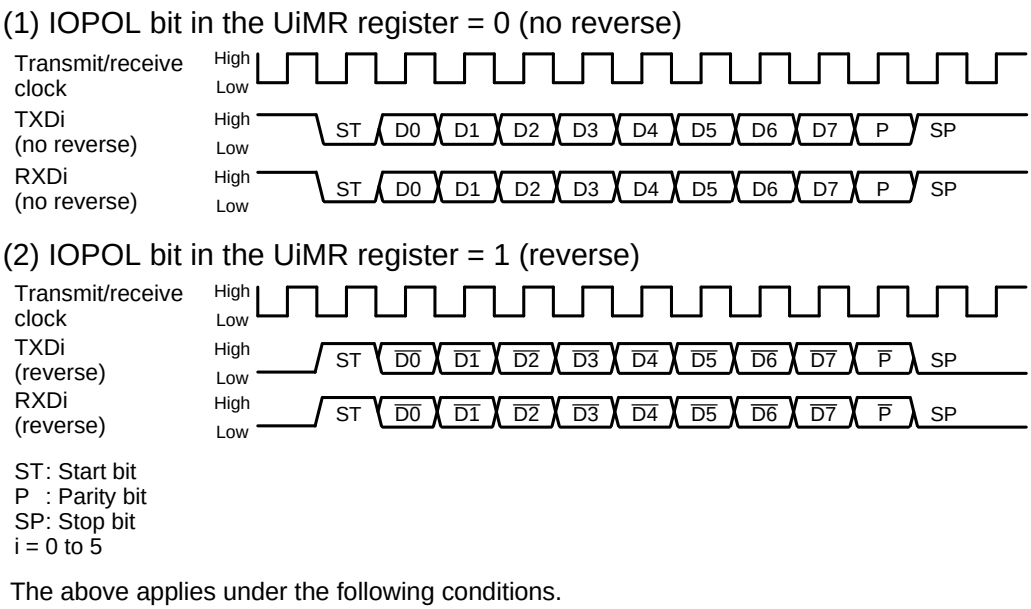
ST : Start bit
P : Parity bit
SP : Stop bit
i = 0 to 5

The above applies under the following conditions.
- The CKPOL bit in the UiC0 register is0 (transmit data output at the falling edge of the transmit/receive clock).
- The UFORM bit in the UiC0 register is 0 (LSB first).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).
- The IOPOL bit in the UiMR register is 0 (TXD, RXD I/O not reversed).

Figure 22.15 Serial Data Logic

22.3.2.5 TXD and RXD I/O Polarity Reverse Function

This function reverses the polarities of the TXDi pin output and RXDi pin input. The logic levels of all input/output data (including bits for start, stop, and parity) are reversed. Figure 22.16 shows TXD and RXD I/O Polarity Reversal.



ST: Start bit
P : Parity bit
SP: Stop bit
i = 0 to 5

The above applies under the following conditions.
- The UFORM bit in the UiC0 register is 0 (LSB first).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).
- The UiLCH bit in the UiC1 register is 0 (serial data logic not reversed).

Figure 22.16 TXD and RXD I/O Polarity Reversal

22.3.2.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when a low-level signal is applied to the $\overline{\text{CTSi}}/\overline{\text{RTSi}}$ (i = 0 to 5) pin. Transmit operation begins when input to the $\overline{\text{CTSi}}/\overline{\text{RTSi}}$ pin becomes low. If the low-level signal is switched to high during a transmit operation, the operation stops after the ongoing transmit/receive operation is completed.

When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTSi}}/\overline{\text{RTSi}}$ pin outputs a low-level signal when the MCU is ready to receive. The output level goes high when a start bit is detected.

Refer to Table 22.11 “I/O Pin Functions in UART Mode”.

22.3.2.7 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Separate Function (UART0)

This function separates $\overline{\text{CTS0}}$ and $\overline{\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and inputs $\overline{\text{CTS0}}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register= 0 (enable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART0)
- The CRS bit in the U0C0 register= 1 (output $\overline{\text{RTS}}$ of UART0)
- The CRD bit in the U1C0 register= 0 (enable $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART1)
- The CRS bit in the U1C0 register= 0 (input $\overline{\text{CTS}}$ of UART1)
- The RCSP bit in the UCON register= 1 (inputs $\overline{\text{CTS0}}$ from the P6_4 pin)
- The CLKMD1 bit in the UCON register= 0 (CLKS1 not used)

Note that when using the $\overline{\text{CTS}}/\overline{\text{RTS}}$ separate function, $\overline{\text{CTS}}/\overline{\text{RTS}}$ of UART1 function cannot be used.

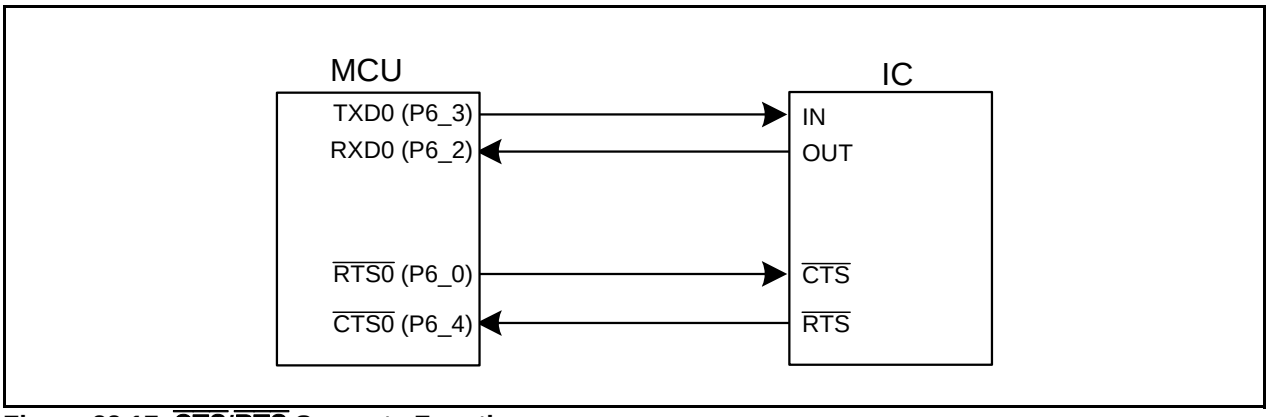


Figure 22.17 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Separate Function

22.3.3 Special Mode 1 (I^2C Mode)

I^2C mode supports the simplified I^2C interface. Table 22.16 lists the specifications of I^2C mode. Table 22.18 and Table 22.19 list the registers used in I^2C mode and the register settings. Table 22.20 lists the I^2C Mode Specifications. Figure 22.18 shows I^2C Mode Block Diagram. Figure 22.19 shows Transfer to UiRB Register and Interrupt Timing.

As shown in Table 22.20, the MCU is placed in I^2C mode by setting bits SMD2 to SMD0 to 010b and the IICM bit to 1. Because SDAi transmit output has a delay circuit attached, SDAi output changes its state after SCLi goes low and remains stably low.

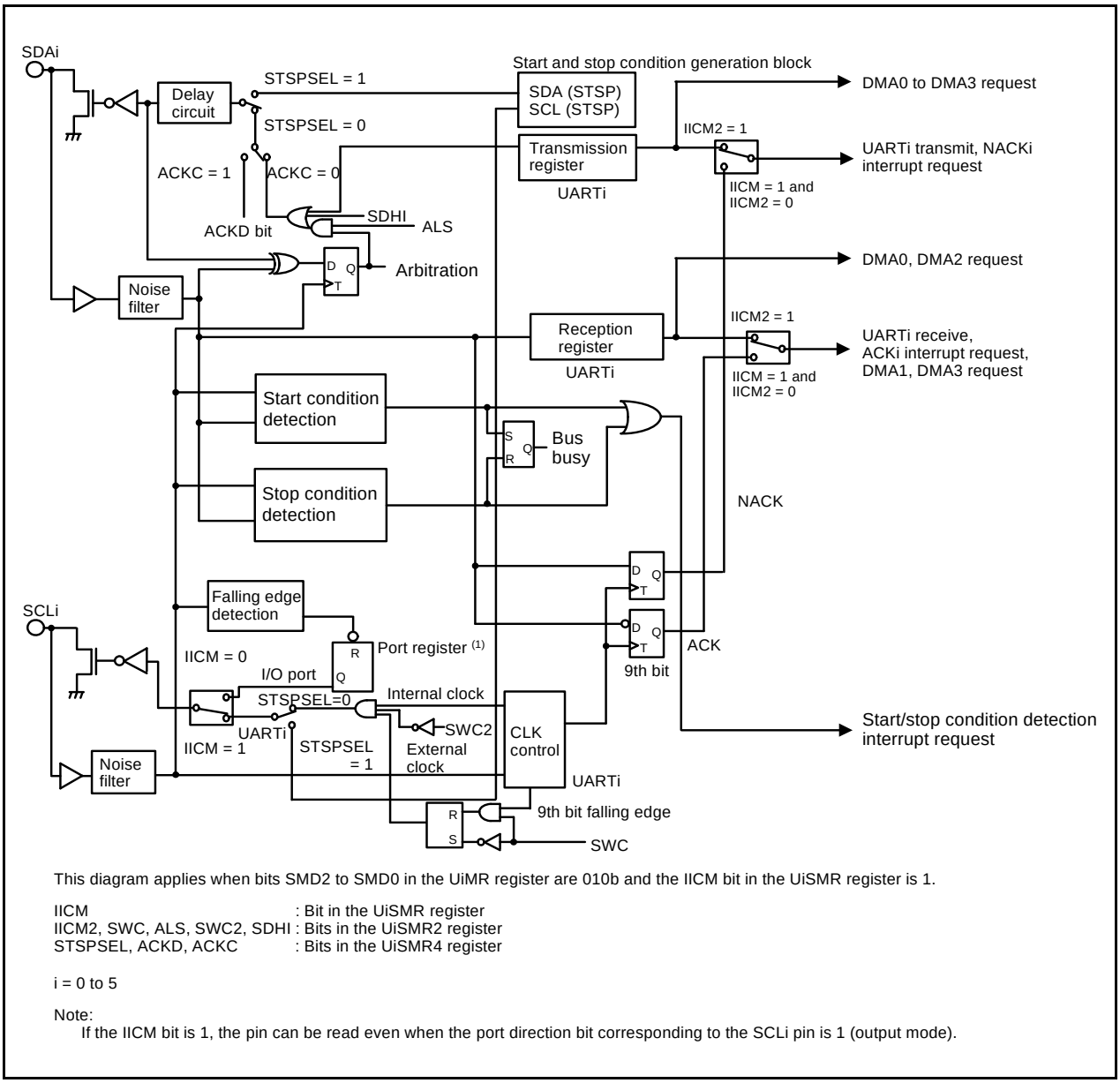
Table 22.16 I^2C Mode Specifications

Item	Specification
Data format	Character bit length: 8 bits
Transmit/receive clock	• Master mode CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n = setting value of the UiBRG register 00h to FFh • Slave mode CKDIR bit = 1 (external clock): Input from the SCLi pin
Transmission start conditions	To start transmission, satisfy the following requirements. (1) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in UiTB register)
Reception start conditions	To start reception, satisfy the following requirements. (1) • The RE bit in the UiC1 register = 1 (reception enabled) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in the UiTB register)
Interrupt request generation timing	Transmission interrupt • Acknowledge undetected or transmit Reception interrupt • Acknowledge undetected or receive Start/stop condition detect interrupt • Start or stop condition detected
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 8th bit of the unit of next data.
Selectable functions	• Arbitration lost Timing that the ABT bit in the UiRB register is updated can be selected. • SDAi digital delay No digital delay or a delay of 2 to 8 UiBRG count source clock cycles can be selected. • Clock phase setting With or without clock delay can be selected.

i = 0 to 5

Notes:

1. When an external clock is selected, the conditions must be met while the external clock is in the high state.
2. If an overrun error occurs, the received data of the UiRB register will be undefined.



This diagram applies when bits SMD2 to SMD0 in the UiMR register are 010b and the IICM bit in the UiSMR register is 1.

IICM : Bit in the UiSMR register
IICM2, SWC, ALS, SWC2, SDHI : Bits in the UiSMR2 register
STSPSEL, ACKD, ACKC : Bits in the UiSMR4 register

i = 0 to 5

Note:
If the IICM bit is 1, the pin can be read even when the port direction bit corresponding to the SCLi pin is 1 (output mode).

Figure 22.18 I²C Mode Block Diagram

Table 22.17 I/O Pin Functions in I²C Mode

Pin Name	I/O	Function
SCLi	Input/output	Clock input or output
SDAi	Input/output	Data input or output

i = 0 to 5

Note:
1. Pins CLKi and $\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$ are not used (they can be used as I/O ports).

Table 22.18 Registers Used and Settings in I²C Mode (1/2) (1)

Register	Bits	Function	
		Master	Slave
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART5.	Select clock prior to division for UART3 to UART5.
PCLKR	PCLK1	Select the count source for the UiBRG register.	Select the count source for the UiBRG register.
UiTB	0 to 7	Set transmission data.	Set transmission data.
	8	- (does not need to be set)	- (does not need to be set)
UiRB	0 to 7	Reception data can be read.	Reception data can be read.
	8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	ABT	Arbitration lost detection flag	Invalid
	OER	Overrun error flag	Overrun error flag
	13 to 15	When read, the read value is undefined.	When read, the read value is undefined.
UiBRG	0 to 7	Set a bit rate.	Invalid
UiMR	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	4 to 6	Set to 0.	Set to 0.
	IOPOL	Set to 0.	Set to 0.
UiC0	CLK1, CLK0	Select the count source for the UiBRG register.	Invalid
	CRS	Invalid because CRD is 1	Invalid because CRD is 1
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD (3)	Set to 1.	Set to 1.
	NCH	Set to 1. (2)	Set to 1. (2)
	CKPOL	Set to 0.	Set to 0.
	UFORM	Set to 1.	Set to 1.
UiC1	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Reception complete flag	Reception complete flag
	UjIRS	Set to 1.	Set to 1.
	UjRRM, UiLCH, UiERE	Set to 0.	Set to 0.
UiSMR	IICM	Set to 1.	Set to 1.
	ABC	Select the timing that arbitration lost is detected.	Invalid
	BBS	Bus busy flag	Bus busy flag
	3 to 7	Set to 0.	Set to 0.

i = 0 to 5 j = 2 to 5

Notes:
1. This table does not describe a procedure.
2. The TXD2 pin is N-channel open drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
3. When using UART1 in I²C mode, to enable the $\overline{CTS}/\overline{RTS}$ separate function of UART0, set the CRD bit in the U1C0 register to 0 ($\overline{CTS}/\overline{RTS}$ enabled) and the CRS bit to 0 ($\overline{CTS}$ input).

Table 22.19 Registers Used and Settings in I²C Mode (2/2) (1)

UiSMR2	IICM2	See Table 22.20 “I²C Mode Functions”.	See Table 22.20 “I²C Mode Functions”.
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCLi output to low at the falling edge of the 9th bit of clock.	Set to 1 to fix SCLi output to low at the falling edge of the 9th bit of clock.
	ALS	Set to 1 to stop SDAi output when arbitration lost is detected.	Set to 0.
	STAC	Set to 0.	Set to 1 to initialize UARTi at start condition detection.
	SWC2	Set to 1 to forcibly pull SCLi output low.	Set to 1 to forcibly pull SCLi output low.
	SDHI	Set to 1 to disable SDAi output.	Set to 1 to disable SDAi output.
	7	Set to 0.	Set to 0.
UiSMR3	0, 2, 4 NODC	Set to 0.	Set to 0.
	CKPH	See Table 22.20 “I²C Mode Functions”.	See Table 22.20 “I²C Mode Functions”.
	DL2 to DL0	Set the amount of SDAi digital delay.	Set the amount of SDAi digital delay.
UiSMR4	STAREQ	Set to 1 to generate start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate restart condition.	Set to 0.
	STPREQ	Set to 1 to generate stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCLi output when stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to set the SCLi to remain low at the falling edge of the 9th bit of clock.
UCON	U0IRS	Set to 1.	Set to 1.
	U1IRS	Set to 1.	Set to 1.
	U0RRM	Set to 0.	Set to 0.
	U1RRM	Set to 0.	Set to 0.
	CLKMD0	Set to 0.	Set to 0.
	CLKMD1	Set to 0.	Set to 0.
	RCSP	Set to 0.	Set to 0.
	7	Set to 0.	Set to 0.

i = 0 to 5

Note:

1. This table does not describe a procedure.

In I^2C mode, the functions and timings vary depending on the combination of the IICM2 bit in the UiSMR2 register and CKPH bit in the UiSMR3 register. Figure 22.19 shows Transfer to UiRB Register and Interrupt Timing. Refer to Figure 22.19 for the timing of transferring to the UiRB register, the bit position of the data stored in the UiRB register, types of interrupts, interrupt requests and DMA request generation timing.

Table 22.20 "I^2C Mode Functions" lists comparison of other functions in clock synchronous serial I/O mode with I^2C mode.

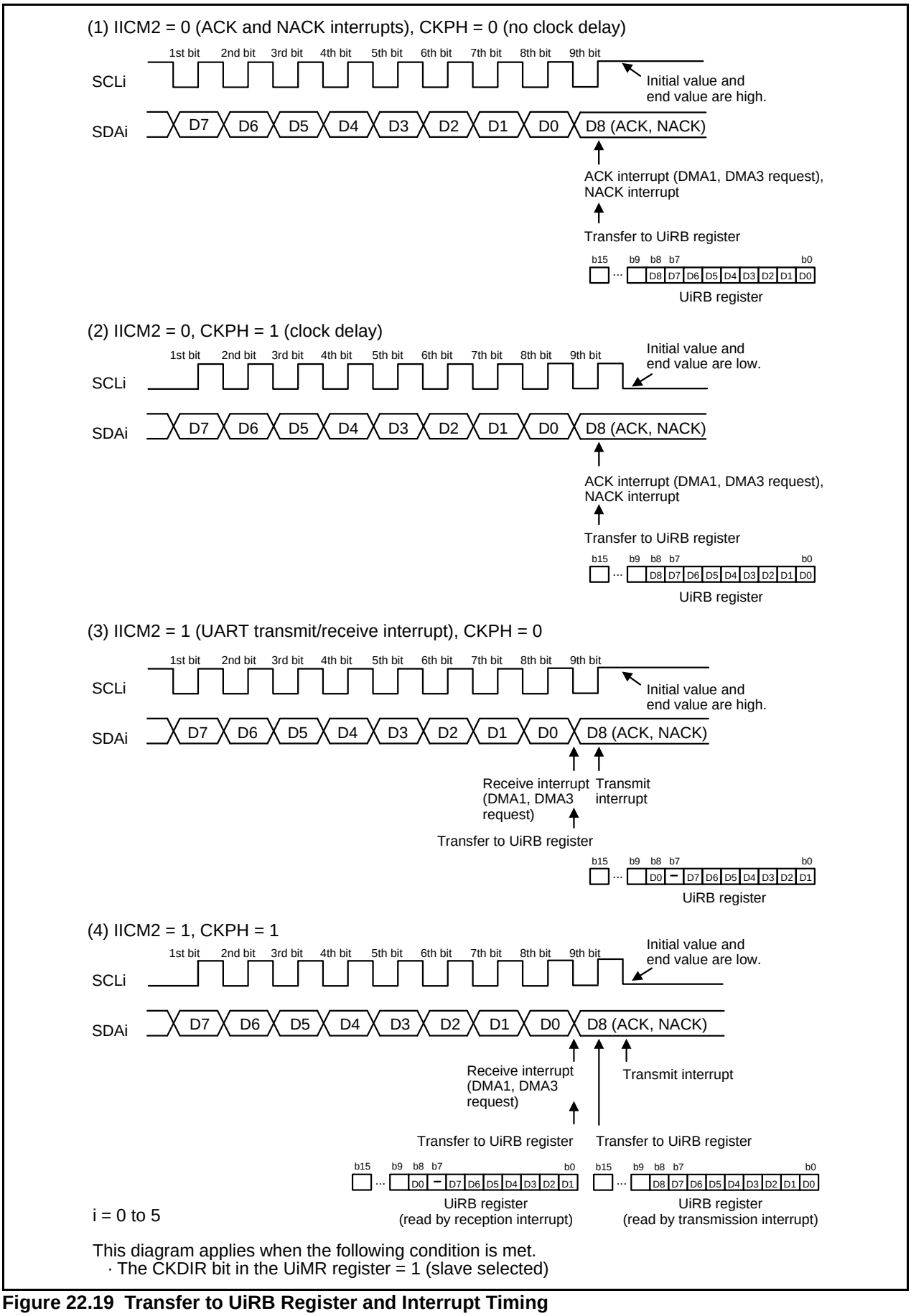
Table 22.20 I^2C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I^2C Mode (SMD2 to SMD0 = 010b, IICM = 1)			
		IICM2 = 0 (NACK/ACK Interrupt)		IICM2 = 1 (UART Transmit/Receive Interrupt)	
		CKPH = 0 (No clock delay)	CKPH = 1 (Clock delay)	CKPH = 0 (No clock delay)	CKPH = 1 (Clock delay)
Start and stop condition detect interrupts	-	Start condition detection or stop condition detection (See Figure 22.21 "STSPSEL Bit Functions")			
Transmission, NACK interrupt (2)	UARTi transmission Transmission started or completed (selected by UiIRS)	No acknowledgment detection (NACK) Rising edge of SCLi 9th bit		UARTi transmission Rising edge of SCLi 9th bit	UARTi transmission Falling edge of SCLi next to the 9th bit
Reception, ACK interrupt (2)	UARTi reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of SCLi 9th bit		UARTi reception Falling edge of SCLi 9th bit	
Timing for transferring data from UART reception shift register to UiRB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of SCLi 9th bit		Falling edge of SCLi 9th bit	Falling and rising edges of SCLi 9th bit
UARTi transmission output delay	Not delayed	Delayed			
Noise filter width	15 ns	200 ns			
Read RXDi and SCLi pin levels	Possible when the corresponding port direction bit = 0	Always possible no matter how the corresponding port direction bit is set			
Initial value of TXDi and SDAi outputs	CKPOL = 0 (high) CKPOL = 1 (low)	The value set in the port register before setting I^2C mode (1)			
Initial and end values of SCLi	-	High	Low	High	Low
DMA1, DMA3 Factor (2)	UARTi reception	Acknowledgment detection (ACK)		UARTi reception Falling edge of SCLi 9th bit	
Read received data	1st to 8th bits of the received data are stored in bits 0 to 7 in the UiRB register.	1st to 8th bits of the received data are stored in bits 7 to 0 in the UiRB register.		1st to 7th bits of the received data are stored in bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register.	When reading by reception interrupt, 1st to 7th bits of the received data are stored in bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register. When reading by transmission interrupt, 1st to 8th bits are stored into bits 7 to 0 in the UiRB register.

i = 0 to 5

Notes:

1. Set the initial value of SDAi output while bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
2. See Figure 22.19 "Transfer to UiRB Register and Interrupt Timing".



This diagram applies when the following condition is met.
· The CKDIR bit in the UiMR register = 1 (slave selected)

Figure 22.19 Transfer to UiRB Register and Interrupt Timing

22.3.3.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDAi pin changes state from high to low while the SCLi pin is in the high state. A stop condition detect interrupt request is generated when the SDAi pin changes state from low to high while the SCLi pin is in the high state.
Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the UiSMR register to determine which interrupt source is requesting the interrupt.

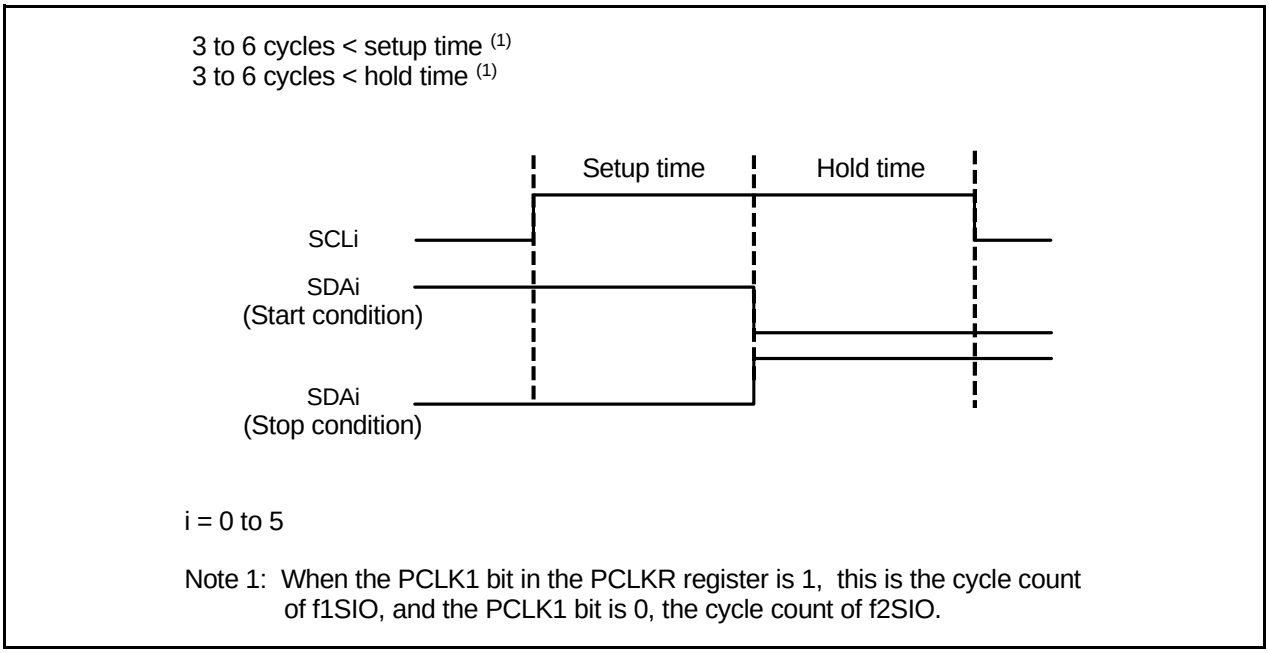


Figure 22.20 Detection of Start and Stop Conditions

22.3.3.2 Output of Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the UiSMR4 register (i = 0 to 5) to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the UiSMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the UiSMR4 register to 1 (start).
The output procedure is as follows.

(1) Set the STAREQ bit, RSTAREQ bit, or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the UiSMR4 register to 1 (output).

The functions of the STSPSEL bit are shown in Table 22.21 and Figure 22.21.

Table 22.21 STSPSEL Bit Functions

Function	STSPSEL = 0	STSPSEL = 1
Output of pins SCLi and SDAi	Output of transmit/receive clock and data Output of start/stop condition is accomplished by a program using ports (not automatically generated in hardware).	Output of a start/stop condition according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition interrupt request generation timing	Detection of start/stop condition	Completion of start/stop condition generation

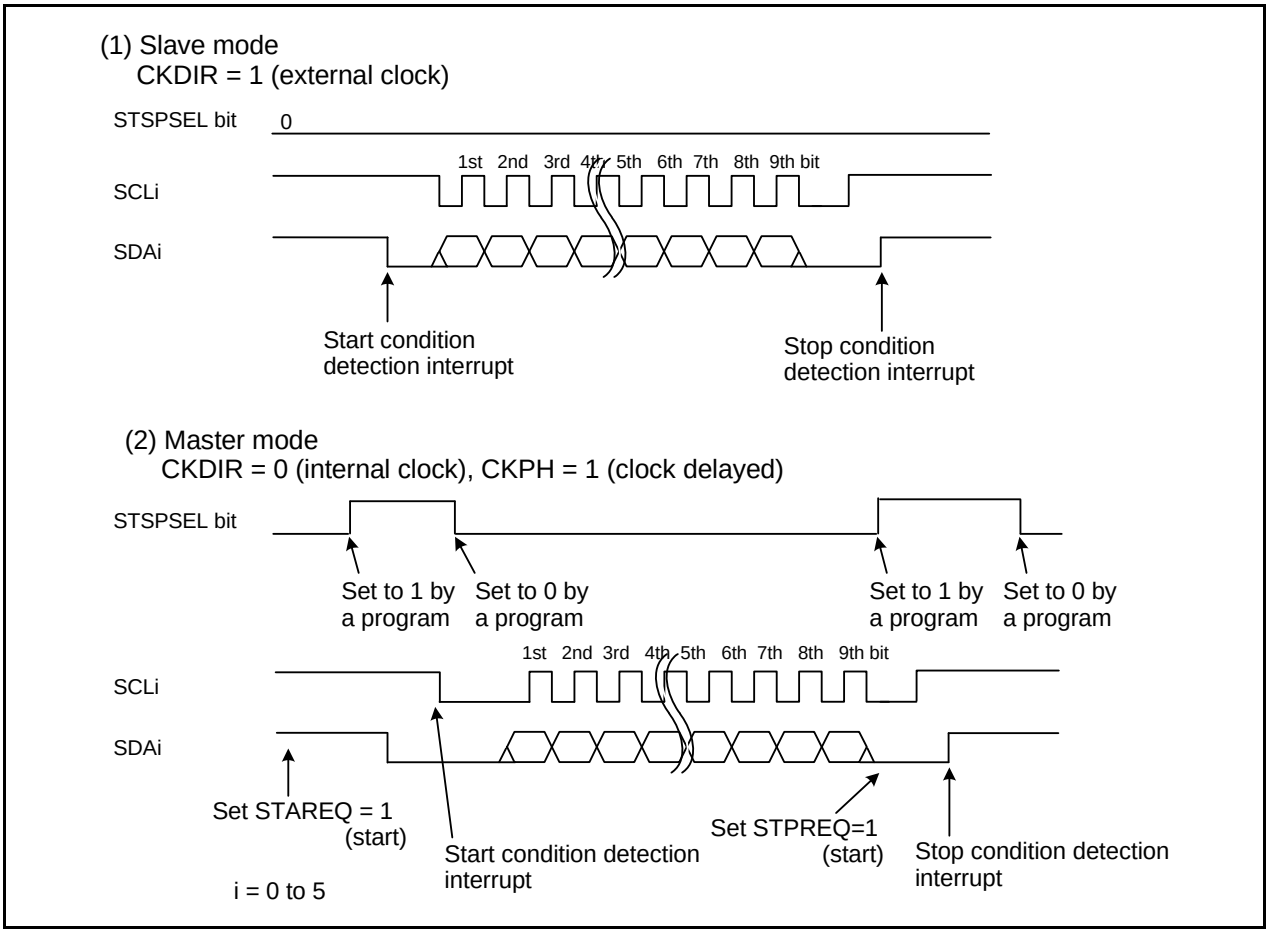


Figure 22.21 STSPSEL Bit Functions

22.3.3.3 Arbitration

Unmatching of the transmit data and SDAi pin input data is checked in synchronization with the rising edge of SCLi. Use the ABC bit in the UiSMR register to select the point at which the ABT bit in the UiRB register is updated. If the ABC bit is 0 (update per bit), the ABT bit is set to 1 at the same time unmatching is detected during check, and is set to 0 when not detected. If the ABC bit is set to 1, if unmatching is ever detected, the ABT bit is set to 1 (unmatching detected) at the falling edge of the clock pulse of the 9th bit. If the ABT bit needs to be updated per byte, set the ABT bit to 0 (undetected) after detecting acknowledge for the first byte, before transmitting/receiving the next byte.

Setting the ALS bit in the UiSMR2 register to 1 (SDA output stop enabled) causes an arbitration-lost to occur, in which case the SDAi pin is placed in the high-impedance state at the same time the ABT bit is set to 1 (unmatching detected).

22.3.3.4 Transmit/Receive Clock

The transmit/receive clock is used to transmit/receive data as is shown in Figure 22.19.

The CSC bit in the UiSMR2 register is used to synchronize an internally generated clock (internal SCLi) and an external clock supplied to the SCLi pin. If the CSC bit is set to 1 (clock synchronization enabled), if a falling edge on the SCLi pin is detected while the internal SCLi is high, the internal SCLi goes low, at which time the value of the UiBRG register is reloaded with and starts counting the low-level intervals. If the internal SCLi changes state from low to high while the SCLi pin is low, counting stops, and when the SCLi pin goes high, counting restarts.

In this way, the UARTi transmit/receive clock is equivalent to AND of the internal SCLi and the clock signal applied to the SCLi pin. The transmit/receive clock works from a half cycle before the falling edge of the internal SCLi 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transmit/receive clock.

The SWC bit in the UiSMR2 register determines whether the SCLi pin is fixed low or freed from low-level output at the falling edge of the 9th clock pulse.

If the SCLHI bit in the UiSMR4 register is set to 1 (enabled), SCLi output is turned off (placed in the high-impedance state) when a stop condition is detected.

When the SWC2 bit in the UiSMR2 register is set to 1 (0 output), a low-level signal can be forcibly output from the SCLi pin even while transmitting or receiving data. When the SWC2 bit is set to 0 (transmit/receive clock), a low-level signal output from the SCLi pin is cancelled, and the transmit/receive clock is input and output.

If the SWC9 bit in the UiSMR4 register is set to 1 (SCL hold low enabled) when the CKPH bit in the UiSMR3 register is 1, the SCLi pin is fixed low at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit to 0 (SCL hold low disabled) frees the SCLi pin from low-level output.

22.3.3.5 SDA Output

The data written to bits 7 to 0 (D7 to D0) in the UiTB register is output in descending order from D7. The 9th bit (D8) is ACK or NACK.

Set the initial value of SDAi transmit output when IICM is 1 (I^2C mode) and bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).

Bits DL2 to DL0 in the UiSMR3 register allow addition of no delays or a delay of 2 to 8 UiBRG count source clock cycles to the SDAi output.

Setting the SDHI bit in the UiSMR2 register to 1 (SDA output disabled) forcibly places the SDAi pin in the high-impedance state. Do not write to the SDHI bit at the rising edge of the UARTi transmit/receive clock. This is because the ABT bit may inadvertently be set to 1 (detected).

22.3.3.6 SDA Input

When the IICM2 bit is 0, the 1st to 8th bits (D7 to D0) of received data are stored in bits 7 to 0 in the UiRB register. The 9th bit (D8) is ACK or NACK.

When the IICM2 bit is 1, the 1st to 7th bits (D7 to D1) of received data are stored in bits 6 to 0 in the UiRB register and the 8th bit (D0) is stored in bit 8 in the UiRB register. Even when the IICM2 bit is 1, the same data as when the IICM2 bit is 0 can be read, provided the CKPH bit is 1. To read the data, read the UiRB register after the rising edge of 9th bit of the clock.

22.3.3.7 ACK and NACK

If the STSPSEL bit in the UiSMR4 register is set to 0 (start and stop conditions not generated) and the ACKC bit in the UiSMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the UiSMR4 register is output from the SDAi pin.

If the IICM2 bit is 0, a NACK interrupt request is generated if the SDAi pin remains high at the rising edge of the 9th bit of transmit clock pulse. An ACK interrupt request is generated if the SDAi pin is low at the rising edge of the 9th bit of the transmit clock.

If ACKi is selected to generate a DMA1 or DMA3 request source, a DMA transfer can be activated by detection of an acknowledge.

22.3.3.8 Initialization of Transmission/Reception

If a start condition is detected while the STAC bit is 1 (UARTi initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the UiTB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UARTi output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCLi pin is pulled low at the falling edge of the 9th clock pulse.

Note that when UARTi transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transmit/receive clock to start UARTi transmission/reception with this setting.

22.3.4 Special Mode 2

Special mode 2 supports serial communication between one or multiple master devices and multiple slaves devices. The transmit/receive clock polarity and phase are selectable. Table 22.22 lists the Special Mode 2 Specifications.

Table 22.22 Special Mode 2 Specifications

Item	Specification
Data format	Character data length: 8 bits
Transmit/receive clock	• Master mode The CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh • Slave mode The CKDIR bit = 1 (external clock selected): Input from the CLKi pin
Transmit/receive control	Controlled by I/O ports
Transmission start Conditions	To start transmission, satisfy the following requirements. (1) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in UiTB register)
Reception start Conditions	To start reception, satisfy the following requirements. (1) • The RE bit in the UiC1 register = 1 (reception enabled) • The TE bit = 1 (transmission enabled) • The TI bit = 0 (data present in the UiTB register)
Interrupt request generation timing	Transmit interrupt: One of the following can be selected. • The UiIRS bit in the UiC1 register= 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit =1 (transmission completed): When the serial interface completed sending data from the UARTi transmit register Receive interrupt: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Data input/output can be chosen to occur synchronously with the rising or the falling edge of the transmit/receive clock. • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register. • Switching serial data logic This function reverses the logic value of the transmit/receive data. • Clock phase setting Selectable from four combinations of transmit/receive clock polarities and phases

i = 0 to 5

Notes:

1. When an external clock is selected, either of the following conditions must be met. If the CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock), the external clock is in high state; if the CKPOL bit is 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transmit/receive clock), the external clock is in low state.
2. If an overrun error occurs, the received data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

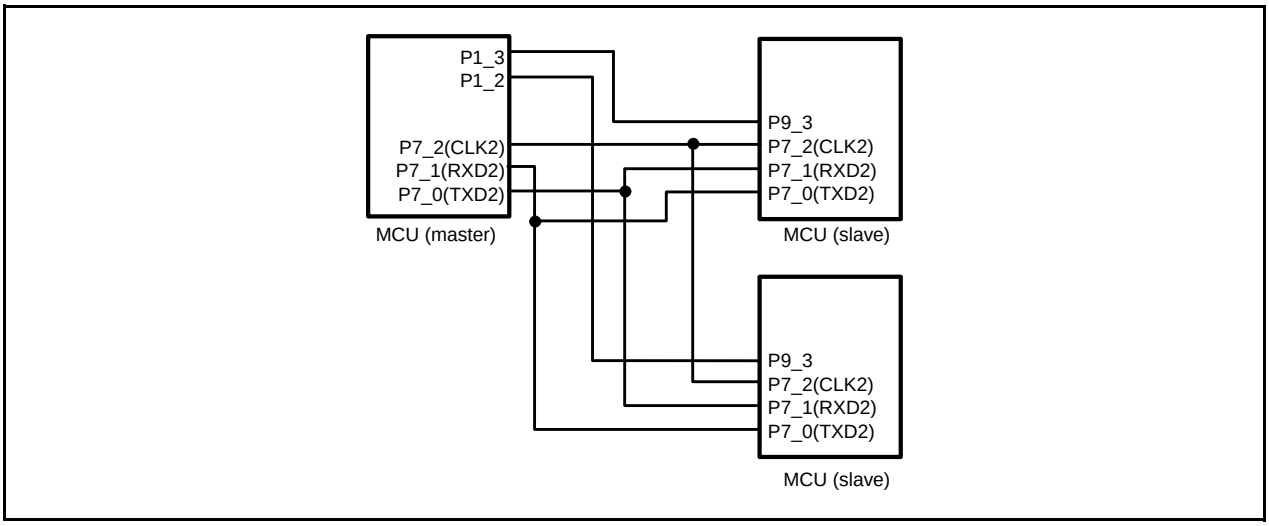


Figure 22.22 Serial Bus Communication Control Example (UART2)

Table 22.23 I/O Pin Functions in Special Mode 2

Pin Name	I/O	Function	Method of Selection
CLKi	Output	Clock output	The CKDIR bit in the UiMR register = 0
	Input	Clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bits sharing pins to 0.
TXDi	Output	Serial data output	(Dummy data output when performing reception only.)
RXDi	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits sharing pins to 0. (can be used as an input port when performing transmission only)

i = 0 to 5

Pins CLKi and $\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$ are not used. (They can be used as I/O ports.)

Table 22.24 Registers Used and Settings in Special Mode 2 (1)

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART5.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 7	Set transmission data.
	8	- (does not need to be set) If necessary, set to 0.
UiRB	0 to 7	Reception data can be read.
	OER	Overrun error flag
	8, 11, 13 to 15	When read, the read value is undefined.
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Set to 0 in master mode or 1 in slave mode.
	4 to 6	Set to 0.
	IOPOL	Set to 0.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	CRS	Invalid because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXDi pin output format. (2)
	CKPOL	Clock phases can be set in combination with the CKPH bit in the UiSMR3 register.
	UFORM	Select the LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS	Select UARTj transmit interrupt source.
	UjRRM	Set to 1 to use continuous receive mode.
	UiLCH	Set to 1 to use inverted data logic.
	UiERE	Set to 0.
UiSMR	0 to 7	Set to 0.
UiSMR2	0 to 7	Set to 0.
UiSMR3	CKPH	Clock phases can be set in combination with the CKPOL bit in the UiC0 register.
	NODC	Set to 0.
	0, 2, 4 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.
UCON	U0IRS	Select UART0 transmit interrupt source.
	U1IRS	Select UART1 transmit interrupt source.
	U0RRM	Set to 1 to use continuous receive mode.
	U1RRM	Set to 1 to use continuous receive mode.
	CLKMD0	Invalid because CLKMD1 is 0
	CLKMD1, RCSP, 7	Set to 0.

i = 0 to 5 j = 2 to 5

Notes:

1. This table does not describe a procedure.
2. The TXD2 pin is N-channel open drain output. No NCH bit in the U2C0 register is assigned. Only write 0 to this bit.

22.3.4.1 Clock Phase Setting Function

One of four combinations of transmit/receive clock phases and polarities can be selected using the CKPH bit in the UiSMR3 register and the CKPOL bit in the UiC0 register.

Make sure the transmit/receive clock polarity and phase are the same for the master and salve devices to be used for communication.

Figure 22.23 shows the Transmission and Reception Timing in Master Mode (Internal Clock).

Figure 22.24 shows the Transmission and Reception Timing (CKPH = 0) in Slave Mode (External Clock) while Figure 22.25 shows the Transmission and Reception Timing (CKPH = 1) in Slave Mode (External Clock).

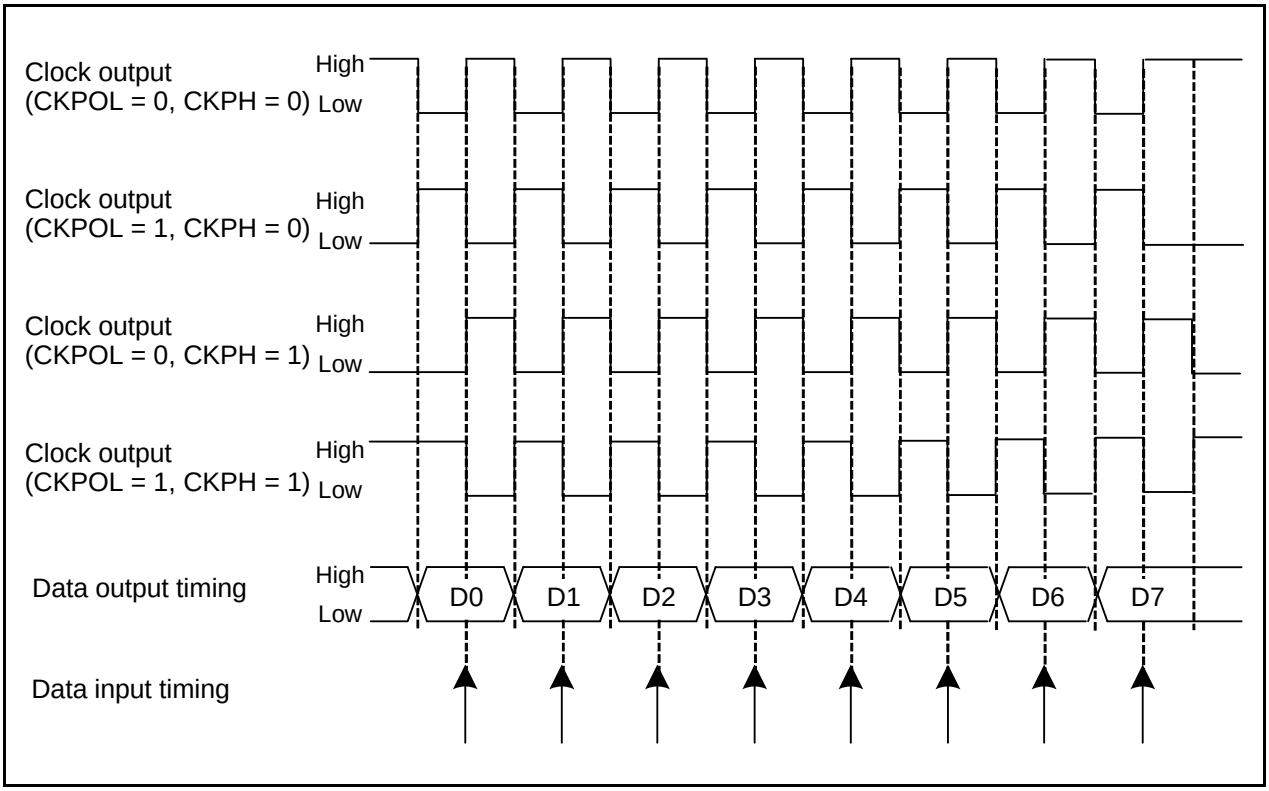
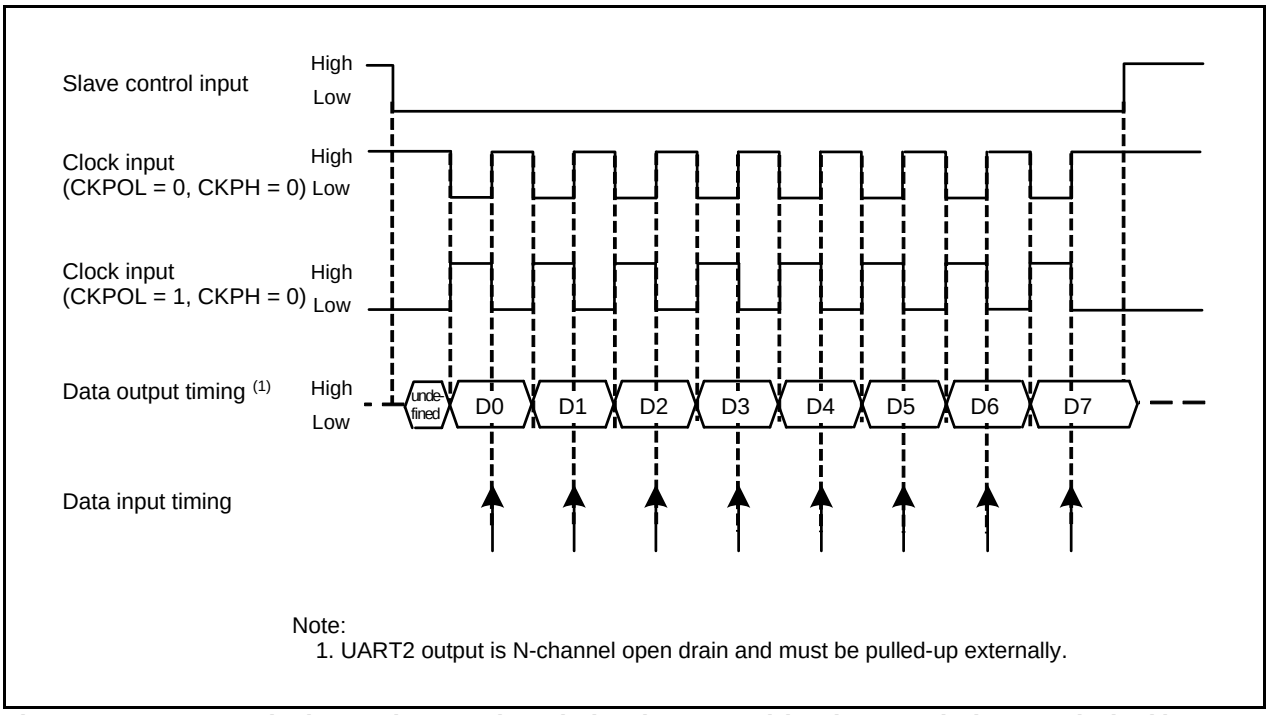
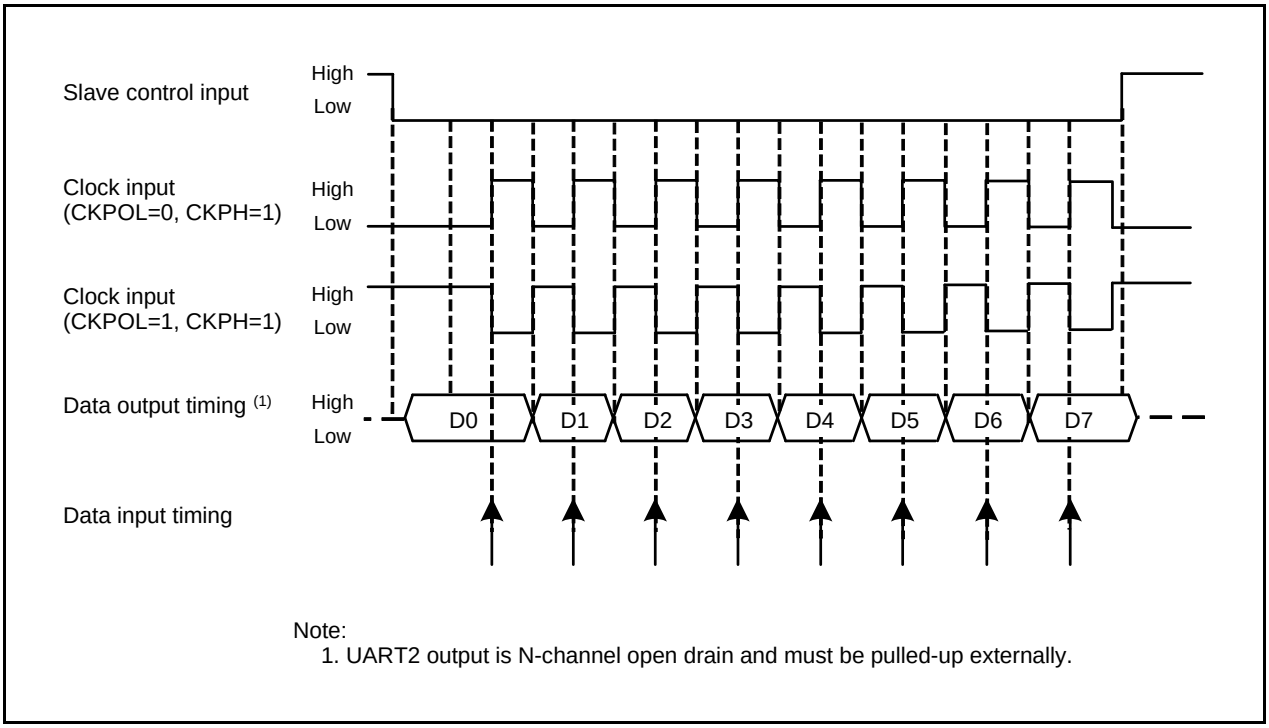


Figure 22.23 Transmission and Reception Timing in Master Mode (Internal Clock)



Note:
1. UART2 output is N-channel open drain and must be pulled-up externally.

Figure 22.24 Transmission and Reception Timing (CKPH = 0) in Slave Mode (External Clock)



Note:
1. UART2 output is N-channel open drain and must be pulled-up externally.

Figure 22.25 Transmission and Reception Timing (CKPH = 1) in Slave Mode (External Clock)

22.3.5 Special Mode 3 (IE Mode)

In this mode, one bit of IEBus is approximated by one byte of UART mode waveform.

Table 22.25 lists the Registers Used and Settings in IE Mode (1). Figure 22.26 shows the Bus Collision Detect Function-Related Bits.

If the TXDi pin (i = 0 to 5) output level and RXDi pin input level do not match, a UARTi bus collision detect interrupt request is generated.

Use bits IFSR26 and IFSR27 in the IFSR2A register to enable the UART0/UART1 bus collision detect function.

Table 22.25 Registers Used and Settings in IE Mode (1)

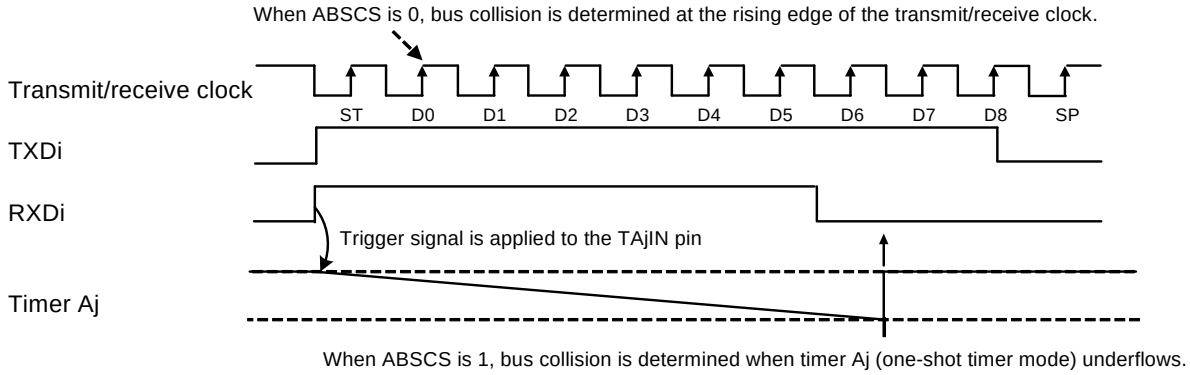
Register	Bits	Function
UiTB	0 to 8	Set transmission data.
UiRB (4)	0 to 8	Reception data can be read.
	OER, FER, PER, SUM	Error flag
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 110b.
	CKDIR	Select internal clock or external clock.
	STPS	Set to 0.
	PRY	Invalid because PRYE is 0
	PRYE	Set to 0.
	IOPOL	Select the TXD and RXD input/output polarity.
UiC0	CLK1, CLK0	Select the count source for the UiBRG register.
	CRS	Invalid because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXDi pin output format. (3)
	CKPOL	Set to 0.
	UFORM	Set to 0.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS (2)	Select the source of UARTj transmit interrupt.
	UjRRM (2), UiLCH, UiERE	Set to 0.
UiSMR	0 to 3, 7	Set to 0.
	ABSCS	Select the sampling timing to detect a bus collision.
	ACSE	Set to 1 to use the auto clear function of transmit enable bit.
	SSS	Select the transmit start condition.
UiSMR2	0 to 7	Set to 0.
UiSMR3	0 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt.
	U0RRM, U1RRM	Set to 0.
	CLKMD0	Invalid because CLKMD1 is 0
	CLKMD1, RCSP, 7	Set to 0.

i = 0 to 5

Notes:

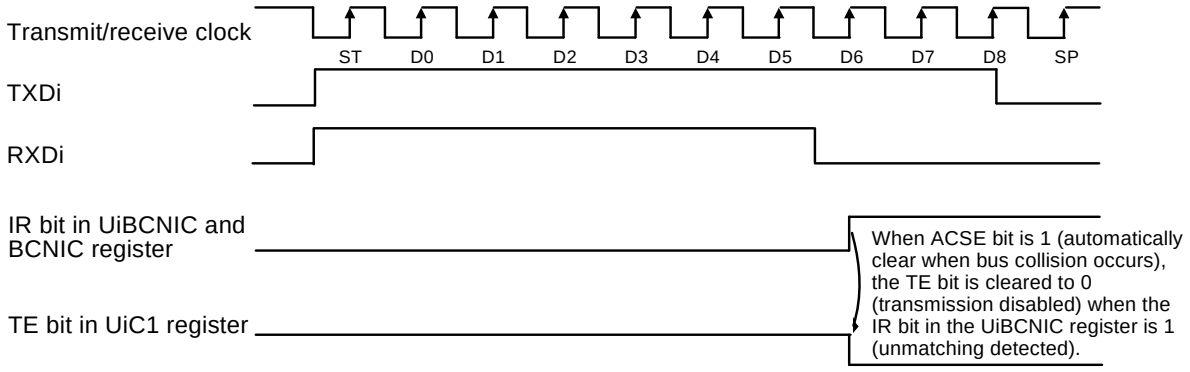
1. This table does not describe a procedure.
2. Set bits 4 and 5 in registers U0C0 and U1C1 to 0. Bits U0IRS, U1IRS, U0RRM, and U1RRM are in the UCON register.
3. The TXD2 pin is N-channel open drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
4. Set the bits not listed above to 0 when writing to the registers in IE mode.

(1) ABSCS bit in UiSMR register (bus collision detect sampling clock select) (i = 0 to 5)



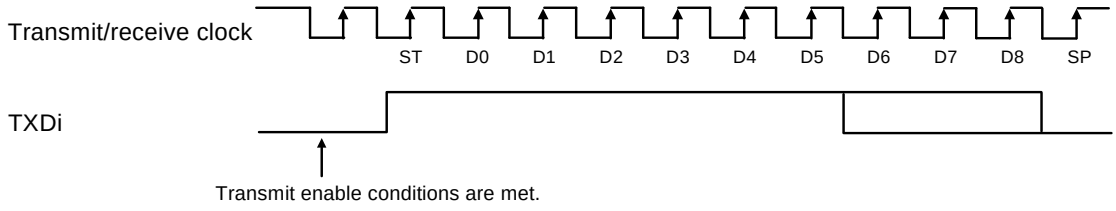
Timer Aj: Timer A3 in UART0; timer A4 in UART1; timer A0 in UART2
timer A0 in UART5; timer A3 in UART4; timer A4 in UART3

(2) ACSE bit in UiSMR register (auto clear of transmit enable bit)

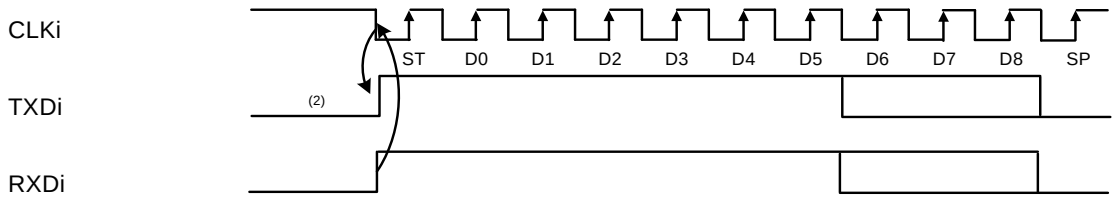


(3) SSS bit in the UiSMR register (transmit start condition select)

When SSS bit is 0, the serial interface starts sending data one transmit/receive clock cycle after the transmission enable condition is met.



When SSS bit is 1, the serial interface starts sending data at the rising edge of RXDi. (1)



Notes :
1. The falling edge of RXDi when IOPOL is 0; the rising edge of RXDi when IOPOL is 1.
2. The transmit conditions must be met before the falling edge of RXD.

The above diagram applies when IOPOL is 1 (reversed). i = 0 to 5

Figure 22.26 Bus Collision Detect Function-Related Bits

22.3.6 Special Mode 4 (SIM Mode) (UART2)

SIM interface devices can communicate in UART mode. Both direct and inverse formats are available. The TXD2 pin outputs a low-level signal when a parity error is detected.
Table 22.26 lists the SIM Mode Specifications. Table 22.27 lists the Registers Used and Settings in SIM Mode (1).

Table 22.26 SIM Mode Specifications

Item	Specification
Data formats	• Direct format • Inverse format
Transmit/receive clock	• The CKDIR bit in the U2MR register = 0 (internal clock): fi/(16(n + 1)) fi = f1SIO, f2SIO, f8SIO, f32SIO n = Setting value of the U2BRG register 00h to FFh • The CKDIR bit = 1 (external clock): fEXT/(16(n + 1)) fEXT = input from the CLK2 pin n = Setting value of the U2BRG register 00h to FFh
Transmission start conditions	To start transmission, satisfy the following requirements. • The TE bit in the U2C1 register = 1 (transmission enabled) • The TI bit in the U2C1 register = 0 (data present in the U2TB register)
Reception start conditions	To start reception, satisfy the following requirements. • The RE bit in the U2C1 register = 1 (reception enabled) • Start bit detection
Interrupt request generation timing (2)	• Transmission When the serial interface completed sending data from the UART2 transmit register (the U2IRS bit =1) • Reception When transferring data from the UART2 receive register to the U2RB register (at completion of reception)
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data. • Framing error (3) This error occurs when the number of stop bits set is not detected. • Parity error (3) During reception, if a parity error is detected, parity error signal is output from the TXD2 pin. During transmission, a parity error is detected by the level of input to the RXD2 pin when a transmission interrupt occurs. • Error sum flag This flag is set to 1 when an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the received data of the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.
2. After reset, a transmit interrupt request is generated by setting the U2IRS bit to 1 (transmission completed) and the U2ERE bit to 1 (error signal output) in the U2C1 register. Therefore, when using SIM mode, set the IR bit to 0 (interrupt not requested) after setting the bits.
3. The timing that the framing error flag and the parity error flag are set is detected when data is transferred from the UART2 receive register to the U2RB register.

Table 22.27 Registers Used and Settings in SIM Mode (1)

Register	Bits	Function
U2TB (2)	0 to 7	Set transmission data.
U2RB (2)	0 to 7	Reception data can be read.
	OER,FER,PER,SUM	Error flag
U2BRG	0 to 7	Set bit rate.
U2MR	SMD2 to SMD0	Set to 101b.
	CKDIR	Select the internal clock or external clock.
	STPS	Set to 0.
	PRY	Set to 1 in direct format or 0 in inverse format.
	PRYE	Set to 1.
	IOPOL	Set to 0.
U2C0	CLK0,CLK1	Select the count source for the U2BRG register.
	CRS	Invalid because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Set to 0.
	CKPOL	Set to 0.
	UFORM	Set to 0 in direct format or 1 in inverse format.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Set to 1.
	U2RRM	Set to 0.
	U2LCH	Set to 0 in direct format or 1 in inverse format.
	U2ERE	Set to 1.
U2SMR (2)	0 to 3	Set to 0.
U2SMR2	0 to 7	Set to 0.
U2SMR3	0 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

Notes:
1. This table does not describe a procedure.
2. Set the bits not listed above to 0 when writing to the registers in SIM mode.

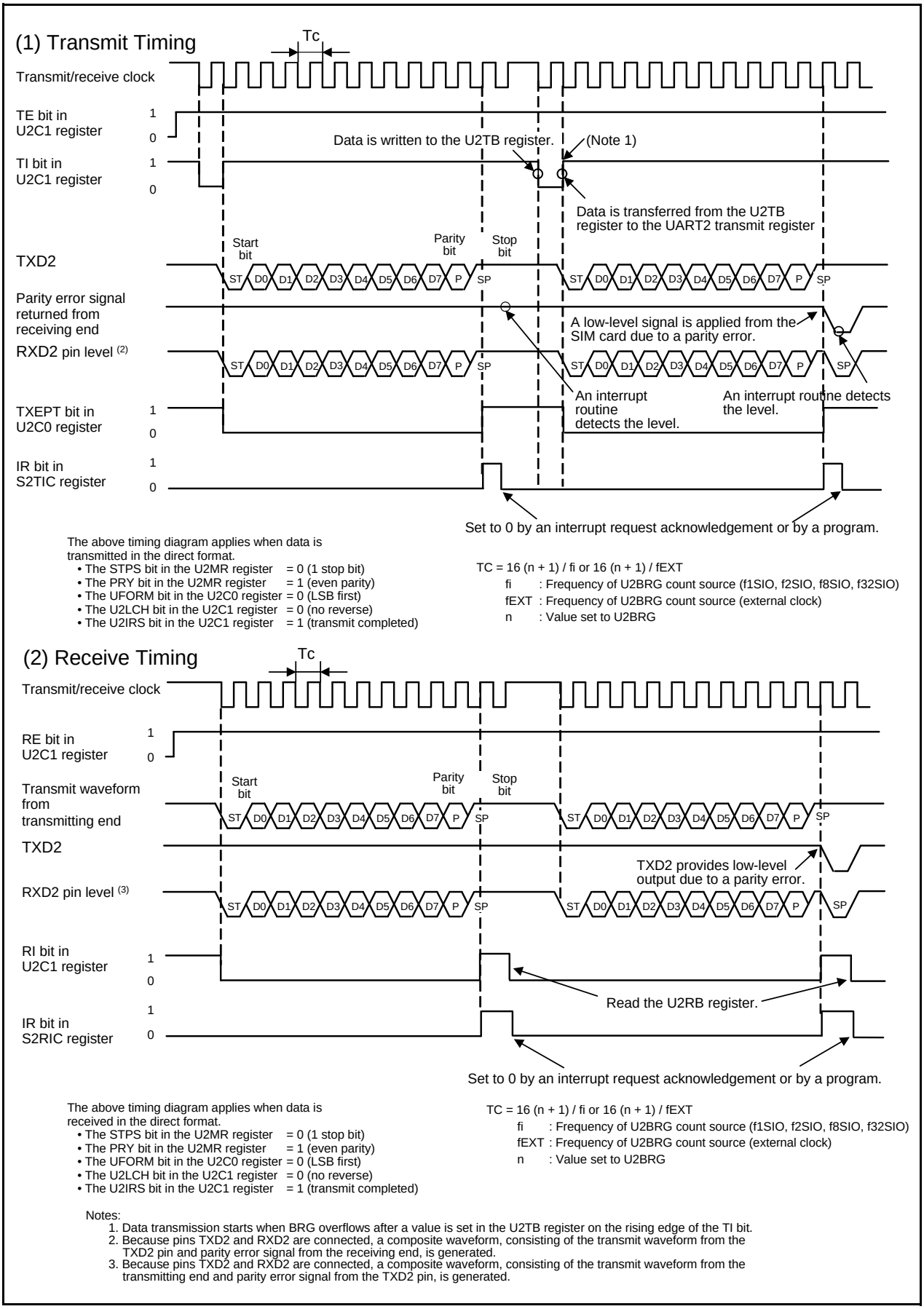


Figure 22.27 Transmit/Receive Timing in SIM Mode

Figure 22.28 shows an Example of SIM Interface Connection. Connect TXD2 and RXD2, and then connect a pull-up resistor.

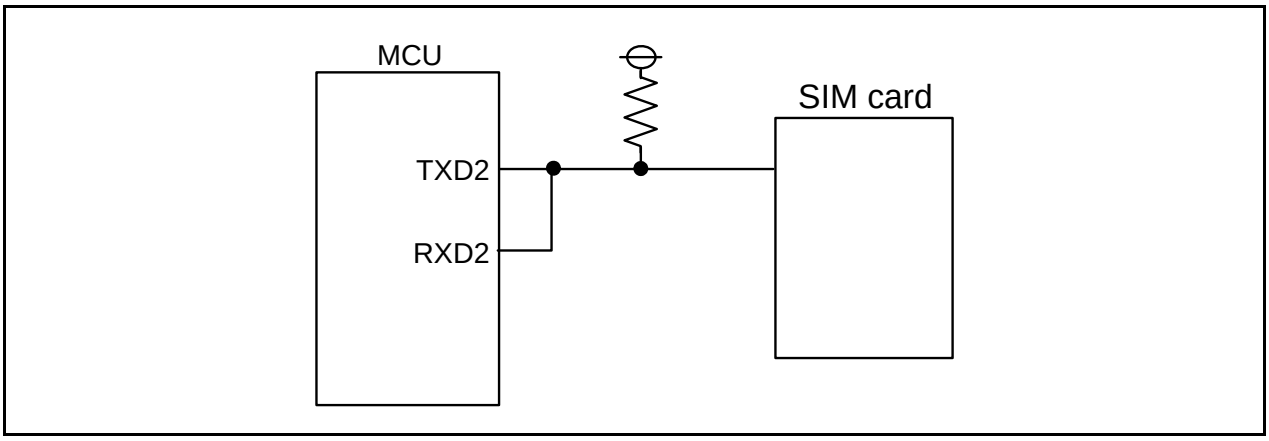


Figure 22.28 Example of SIM Interface Connection

22.3.6.1 Parity Error Signal Output

The parity error signal is enabled by setting the U2ERE bit in the U2C1 register to 1 (error signal output).

The parity error signal is output when a parity error is detected while receiving data. A low-level signal is output from the TXD2 pin in the timing shown in Figure 22.29. If the U2RB register is read while outputting a parity error signal, the PER bit is cleared to 0 (no parity error) and at the same time the TXD2 output again goes high.

When transmitting, a transmission complete interrupt request is generated at the falling edge of the transmit/receive pulse that immediately follows the stop bit. Therefore, whether or not a parity error signal has been returned can be determined by reading the port that shares the RXD2 pin in a transmission complete interrupt routine.

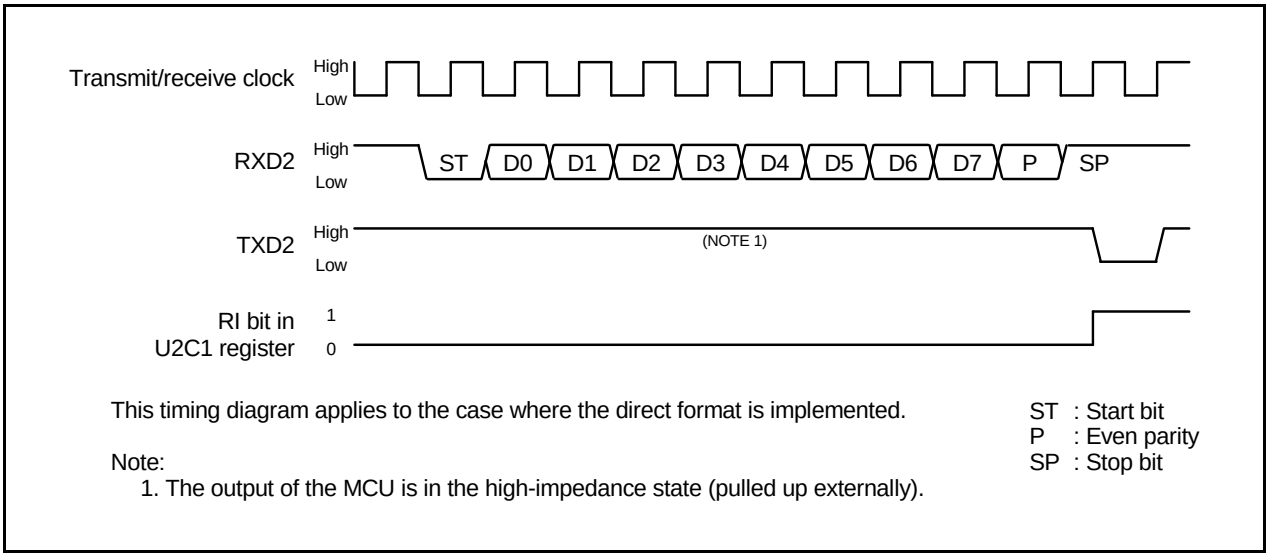


Figure 22.29 Parity Error Signal Output Timing

22.3.6.2 Format

Two formats are available: direct format and inverse format.

For direct format, set the PRYE bit in the U2MR register to 1 (parity enabled), the PRY bit to 1 (even parity), the UFORM bit in the U2C0 register to 0 (LSB first) and the U2LCH bit in the U2C1 register to 0 (not inverted). When data is transmitted, the contents of the U2TB register are transmitted with the even-numbered parity, starting from D0. When data is received, the receive data are stored in the U2RB register, starting from D0. The even-numbered parity is used to determine when a parity error occurs.

For inverse format, set the PRYE bit to 1, the PRY bit to 0 (odd parity), the UFORM bit to 1 (MSB first), and the U2LCH bit to 1 (inverted). When data is transmitted, the contents of the U2TB register are logically inverted and are transmitted with odd-numbered parity, starting from D7. When data is received, the receive data is logically inverted and stored in the U2RB register, starting from D7. The odd-numbered parity is used to determine when a parity error occurs.

Figure 22.30 shows SIM Interface Format.

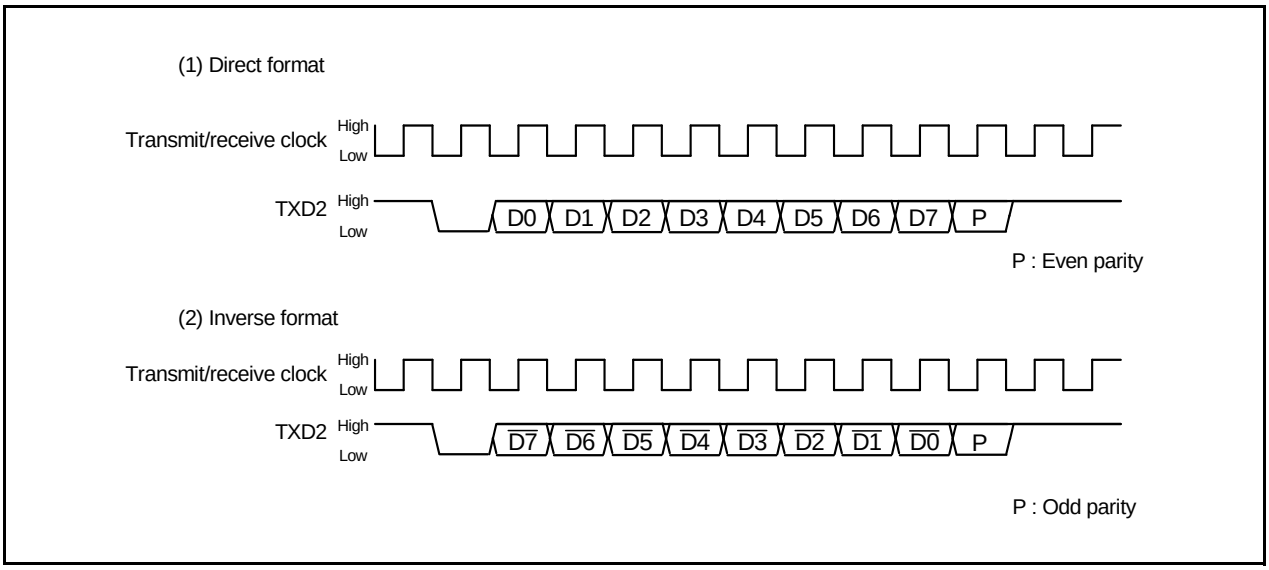


Figure 22.30 SIM Interface Format

22.4 Interrupts

UART0 to UART5 include interrupts by transmission, reception, ACK, NACK, start/stop condition detection, and bus collision detection.

22.4.1 Interrupt Related Registers

Refer to operation examples in each mode for interrupt sources and interrupt request generation timing. For the details of interrupt control, refer to 14.7 “Interrupt Control”. Table 22.28 lists UART0 to UART5 Interrupt Related Registers.

Table 22.28 UART0 to UART5 Interrupt Related Registers

Address	Register	Symbol	Reset Value
0046h	UART1 Bus Collision Detection Interrupt Control Register	U1BCNIC	XXXX X000b
0047h	UART0 Bus Collision Detection Interrupt Control Register	U0BCNIC	XXXX X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register	U5BCNIC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register	S5TIC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART4 Bus Collision Detection Interrupt Control Register	U4BCNIC	XXXX X000b
006Fh	UART4 Transmit Interrupt Control Register	S4TIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	UART3 Bus Collision Detection Interrupt Control Register	U3BCNIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h

Some interrupts of UART0 to UART5 share interrupt vectors and interrupt control registers with other peripheral functions. When using these interrupts, select them by interrupt source select registers. Table 22.29 lists Interrupt Select in UART0 to UART5.

Table 22.29 Interrupt Select in UART0 to UART5

Interrupt Source	Interrupt Source Select Register Settings		
	Register	Bit	Setting Value
UART0 start/stop condition detection, bus collision detection	IFSR2A	IFSR26	1
UART1 start/stop condition detection, bus collision detection	IFSR2A	IFSR27	1
UART4 start/stop condition detection, bus collision detection	IFSR3A	IFSR35	0
UART4 transmission, NACK	IFSR3A	IFSR36	0

An interrupt request may be generated by bit contents change in the following modes.

- Special mode 1 (I^2C mode)
  Set the IR bit in the interrupt control register of UARTi to 0 (interrupt not requested), when the following bits are changed:
  Bits SMD2 to SMD0 in the UiMR register, the IICM bit in the UiSMR register, the IICM2 bit in the UiSMR2 register, the CKPH bit in the UiSMR3 register
- Special mode 4 (SIM mode)
  After reset, when bits U2IRS and U2ERE in the U2C1 register are set to 1 (transmission completed) and 1 (interrupt not requested) respectively, a transmission interrupt request is generated. In SIM mode, set these bits first, and then set the IR bit in the S2TIC register to 0 (interrupt not requested).

22.4.2 Reception Interrupt

- The case that bits SMD2 to SMD0 in the UiMR register are not set to 010b (I^2C mode)
  When the RI bit in the UiC1 register is changed from 0 (no data in the UiRB register) to 1 (data present in the UiRB register), the IR bit in the SiRIC register is automatically set to 1 (interrupt requested).
  If an overrun error occurs (when the RI bit is 1, the next data is received), the RI bit remains 1, and therefore, the IR bit in the SiRIC register remains unchanged.
- The case that bits SMD2 to SMD0 in the UiMR register are set to 010b (I^2C mode)
  When the RI bit in the UiC1 register is changed from 0 (no data in the UiRB register) to 1 (data present in the UiRB register), the IR bit in the SiRIC register is automatically set to 1 (interrupt requested).
  When an overrun error occurs, the IR bit in the SiRIC register also becomes 1.

22.5 Notes on Serial Interface UARTi (i=0 to 5)

22.5.1 Common Notes on Multiple Modes

22.5.1.1 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins go to high-impedance state:
P7_2/CLK2/TA1OUT/V, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$, P7_4/TA2OUT/W, P7_5/TA2IN/$\overline{W}$, P8_0/TA4OUT/RXD5/SCL5/U, P8_1/TA4IN/$\overline{CTS5}$/$\overline{RTS5}$/$\overline{U}$

22.5.1.2 Register Setting

Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART5. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART5 again.

22.5.1.3 CLKi Output

(Technical update number: TN-M16C-A178A/E)

When using the N-channel open drain output as an output mode of the CLKi pin, use following procedure to change the pin function:

When changing the pin function from the port to CLKi.
(1) Set bits SMD2 to SMD0 in the UiMR register to a value other than 000b to select serial interface mode.
(2) Set the NODC bit in the UiSMR3 register to 1.

When changing the pin function from CLKi to the port.
(1) Set the NODC bit to 0.
(2) Set bits SMD2 to SMD0 to 000b to disable the serial interface.

22.5.2 Clock Synchronous Serial I/O

22.5.2.1 Transmission/Reception

When the $\overline{RTS}$ function is used with an external clock, $\overline{RTSi}$ pin (i = 0 to 5) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{RTSi}$ pin outputs a high-level signal when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{RTSi}$ pin to the $\overline{CTSi}$ pin of the transmitting side. The $\overline{RTS}$ function is disabled when an internal clock is selected.

22.5.2.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the UiC0 register (i = 0 to 5) is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transmit and receive clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transmit and receive clock).

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.

22.5.2.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating a transmitter. Set the UARTi-associated registers for a transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXDi pin (i = 0 to 5) while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the UiTB register, and input an external clock to the CLKi pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is set to 1 (data present in the UiRB register) and the next receive data is received in the UARTi receive register. And then, the OER bit in the UiRB register is set to 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register per each receive operation.

When an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is 0 (transmit data output at the falling edge and receive data input at the rising edge of the serial clock), or while the external clock is held low when the CKPOL bit is 1 (transmit data output at the rising edge and receive data input at the falling edge of the serial clock).

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

22.5.3 UART (Clock Asynchronous Serial I/O) Mode

22.5.3.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTSi}}$ pin (i = 0 to 5) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTSi}}$ pin outputs a high-level signal when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTSi}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

22.5.3.2 Transmission

When an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the UiC0 register (i = 0 to 5) is 0 (transmit data output at the falling edge and receive data input at the rising edge of the transmit and receive clock), or while the external clock is held low when the CKPOL bit is 1 (transmit data output at the rising edge and receive data input at the falling edge of the transmit and receive clock).

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTSi}}$ pin is low.

22.5.4 Special Mode 1 (I^2C Mode)

22.5.4.1 Generation of Start and Stop Conditions

When generating start, stop and restart conditions, set the STSPSEL bit in the UiSMR4 register (i = 0 to 5) to 0 and wait for more than half cycle of the transmit and receive clock. Then set each condition generation bit (STAREQ, RSTAREQ and STPREQ) from 0 to 1.

22.5.4.2 IR Bit

Set the following bits first, and then set the IR bit in the UARTi interrupt control registers to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the UiMR register, the IICM bit in the UiSMR register,
the IICM2 bit in the UiSMR2 register, the CKPH bit in the UiSMR3 register

22.5.5 Special Mode 4 (SIM Mode)

After reset, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed) and 1 (error signal output), respectively. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.