M16C/65 Group

External Buses

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1. Abstract

This document introduces the external bus.

2. Introduction

This application note applies to the M16C/65 Group microcomputer (MCU).

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. External Buses

3.1 Overview

Memory and I/O external expansion can be connected to the MCU easily using external buses. When memory expansion mode or microprocessor mode is selected for the processor mode, some of the pins function as the address bus, the data bus, and as control signals, which makes the external buses operational.

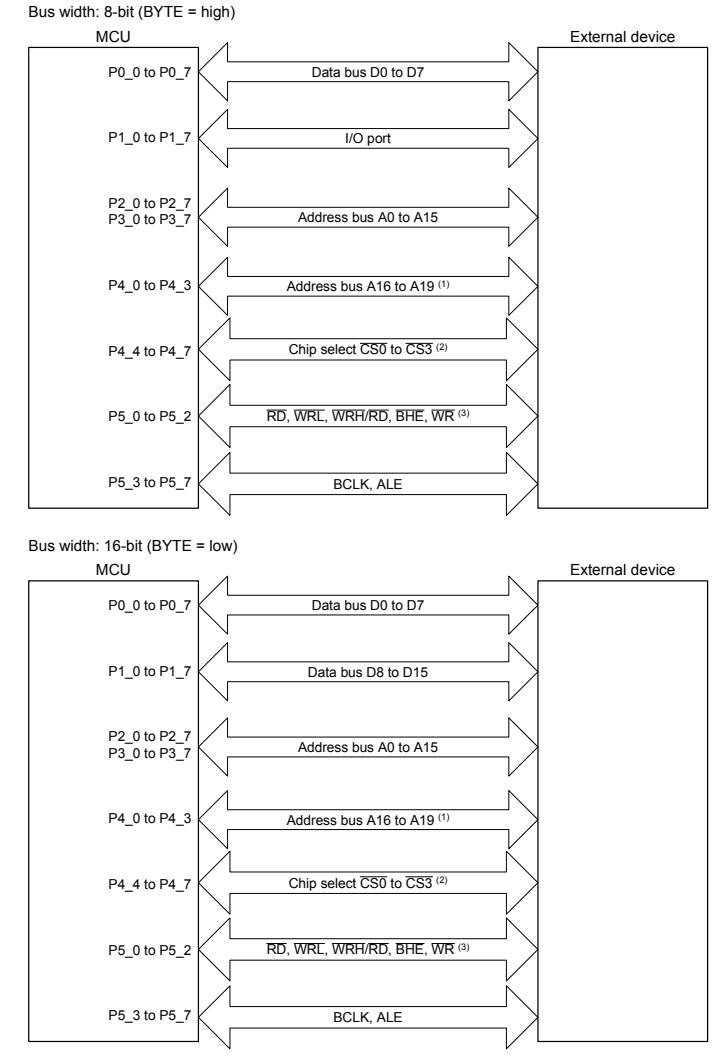
When accessing an external area, an 8-bit data bus width or 16-bit data bus width can be selected based on the BYTE pin level. The 16-bit width is used to access internal areas regardless of the BYTE pin level. Fix the BYTE pin either high or low. 8-bit and 16-bit data bus widths cannot be used together in an external area.

3.2 Data Access

3.2.1 Data Bus Width

When the voltage level input to the BYTE pin is high, the external data bus width becomes 8 bits, and P1_0 (/D8) through P1_7 (/D15) can be used as I/O ports (see Figure 3.1 for details).

When the voltage level input to the BYTE pin is low, the external data bus width becomes 16 bits, and P1_0 (/D8) through P1_7 (/D15) operate as a data bus (D8 through D15) (see Figure 3.1 for details).



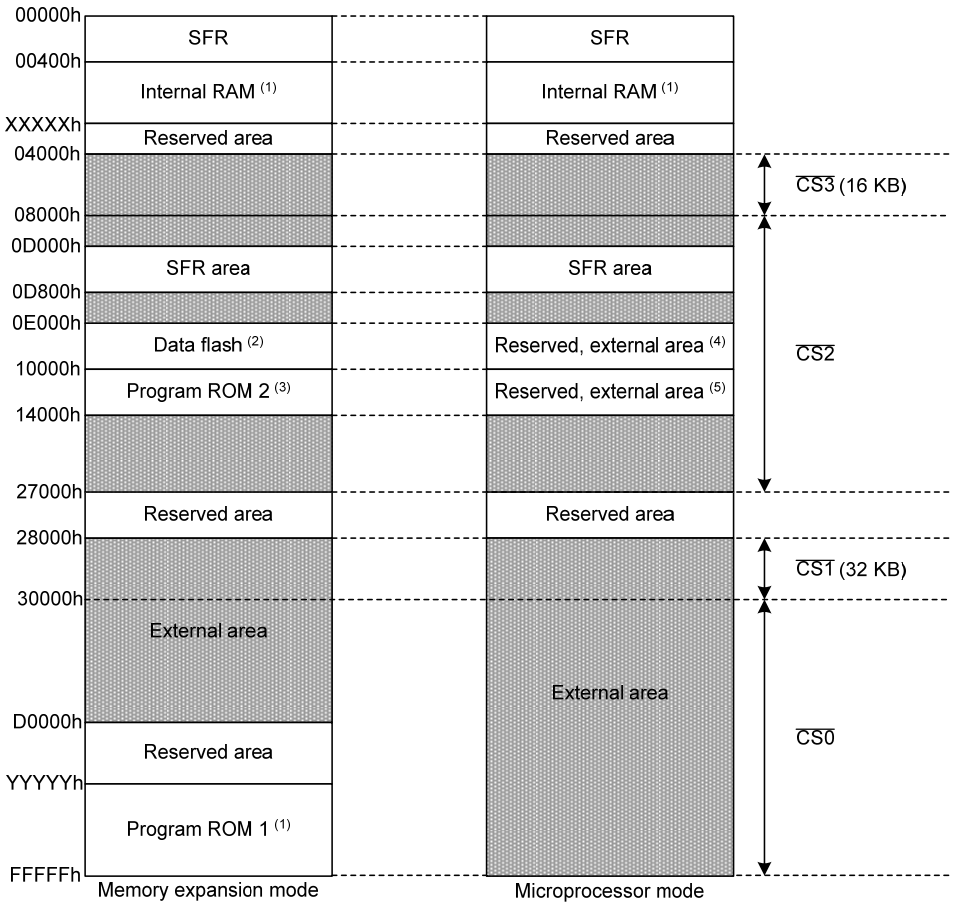
Notes:
1. Can be switched to I/O port using the port P4_0 to P4_3 function select bits of processor mode register 0 (address 0004h).
2. When reset, only CS0 outputs a chip select signal. CS1 through CS3 become input ports. I/O ports can be switched using the CSi output enable bit of the chip select control register (address 0008h).
3. The feature can be switched using the R/W mode select bit of processor mode register 0 (address 0004h).

Figure 3.1 BYTE Pin Level and External Data Bus Width

3.2.2 Chip Select and Address Bus

Chip select signals (pins P4_4/$\overline{CS0}$ through P4_7/$\overline{CS3}$) are output in areas resulting from dividing a 1-MB memory space into four. This document does not explain the 4-MB memory space (refer to the hardware manual for details). To output a chip select signal, the chip select output must be enabled by setting the chip select control register. Figure 3.2 shows addresses where chip select signals become active low.

Since the internal area and external area in memory expansion mode are different from those in microprocessor mode, there is a difference between areas for which $\overline{CS0}$ is output. When an internal ROM/RAM area is being accessed, no chip select signal is output, and the address bus does not change (the address of the external area that was accessed previously is held).



Notes:

1. When the PM13 bit in the PM1 register is 0, 15 KB of the internal RAM and 192 KB of the internal ROM can be used. See the table below for addresses XXXXXh and YYYYYh.

Internal RAM		Program ROM 1	
Capacity	Address XXXXXh	Capacity	Address YYYYYh
12 KB	033FFh	128 KB	E0000h
20 KB	033FFh	256 KB	D0000h
31 KB	033FFh	384 KB	D0000h
47 KB	033FFh	512 KB	D0000h
		640 KB	D0000h
		768 KB	D0000h

2. When the PM10 bit is 0, this area is used as an external area; when the bit is 1, the area is used as internal ROM (data flash).
3. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when the bit is 0, the area is used as internal ROM (program ROM 2).
4. When the PM10 bit is 0, this area is used as an external area; when the bit is 1, the area is used as a reserved area.
5. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when the bit is 0, the area is used as a reserved area.

Figure 3.2 Addresses in which Chip Select Signals Become Active Low

Chip Select Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	Reset Value
CSR	0008h	01h

Bit Symbol	Bit Name	Function	RW
CS0	$\overline{CS0}$ output enable bit	0: Chip select out disabled (functions as I/O port) 1: Chip select output enabled	RW
CS1	$\overline{CS1}$ output enable bit		RW
CS2	$\overline{CS2}$ output enable bit		RW
CS3	$\overline{CS3}$ output enable bit		RW
CS0W	$\overline{CS0}$ wait bit	0: Wait state 1: No wait state	RW
CS1W	$\overline{CS1}$ wait bit		RW
CS2W	$\overline{CS2}$ wait bit		RW
CS3W	$\overline{CS3}$ wait bit		RW

Figure 3.3 Chip Select Control Register

3.2.3 Bus Types

The M16C/65 Group has two types of buses: a separate bus where separate pins are used for address output and data I/O and a multiplexed bus where pins are time-multiplexed and switched between address output and data I/O to save the number of pins used.

A separate bus is used to access devices such as ROM and RAM which have separate buses. The areas accessed via separate buses can be allocated for programs and data.

A multiplexed bus is used to access devices such as ASSPs which have multiplexed buses. The areas accessed via a multiplexed bus can only be allocated for data. Programs cannot be located in these areas.

The areas accessed via a multiplexed bus can be selected from the $\overline{CS2}$ area, $\overline{CS1}$ area, or entire space by setting the multiplexed bus select bits (bits 4 and 5) in the processor mode register 0 (address 0004h). However, the entire space cannot be selected when operating in microprocessor mode.

Areas not accessed via a multiplexed bus are accessed through separate buses.

When accessing an area set for a multiplexed bus, the BYTE pin is high, data bus D0 to D7 are multiplexed with address bus A0 to A7.

When the BYTE pin is low, data bus D0 to D7 are multiplexed with address bus A1 to A8. In either case, the bus is switched between data and address.

In the latter case, however, the addresses of the connected devices are mapped into even addresses (every other address) of the M16C/65. Therefore, be sure to access the M16C/65's even addresses in bytes when accessing a connected device.

3.2.4 R/W Modes

The read/write signal that is output when accessing an external area can be selected between $\overline{RD}$ / $\overline{BHE}$ / $\overline{WR}$ and the $\overline{RD}$ / $\overline{WRH}$ / $\overline{WRL}$ modes by setting the R/W mode select bit (bit 2) in processor mode register 0 (address 0004h). Use the $\overline{RD}$ / $\overline{BHE}$ / $\overline{WR}$ mode to access a 16-bit wide RAM and the $\overline{RD}$ / $\overline{WRH}$ / $\overline{WRL}$ mode to access an 8-bit wide RAM.

When the M16C/65 is reset, the $\overline{RD}$ / $\overline{BHE}$ / $\overline{WR}$ mode is selected by default. When changing modes, change the $\overline{RD}$ / $\overline{BHE}$ / $\overline{WR}$ to the $\overline{RD}$ / $\overline{WRH}$ / $\overline{WRL}$ mode before accessing external RAM.

Refer to the $\overline{RD}$ / $\overline{BHE}$ / $\overline{WR}$ and $\overline{RD}$ / $\overline{WRH}$ / $\overline{WRL}$ connection examples shown in section 3.3"Connection Examples".

3.3 Connection Examples

3.3.1 Connecting 16-bit Memory to a 16-bit Wide Data Bus Connecting 16-bit

Figure 3.4 shows an example of connecting HM6216514LTTI (SRAM). In this diagram, when reset, the MCU starts operating in single-chip mode. Change this mode to memory expansion mode in a program.

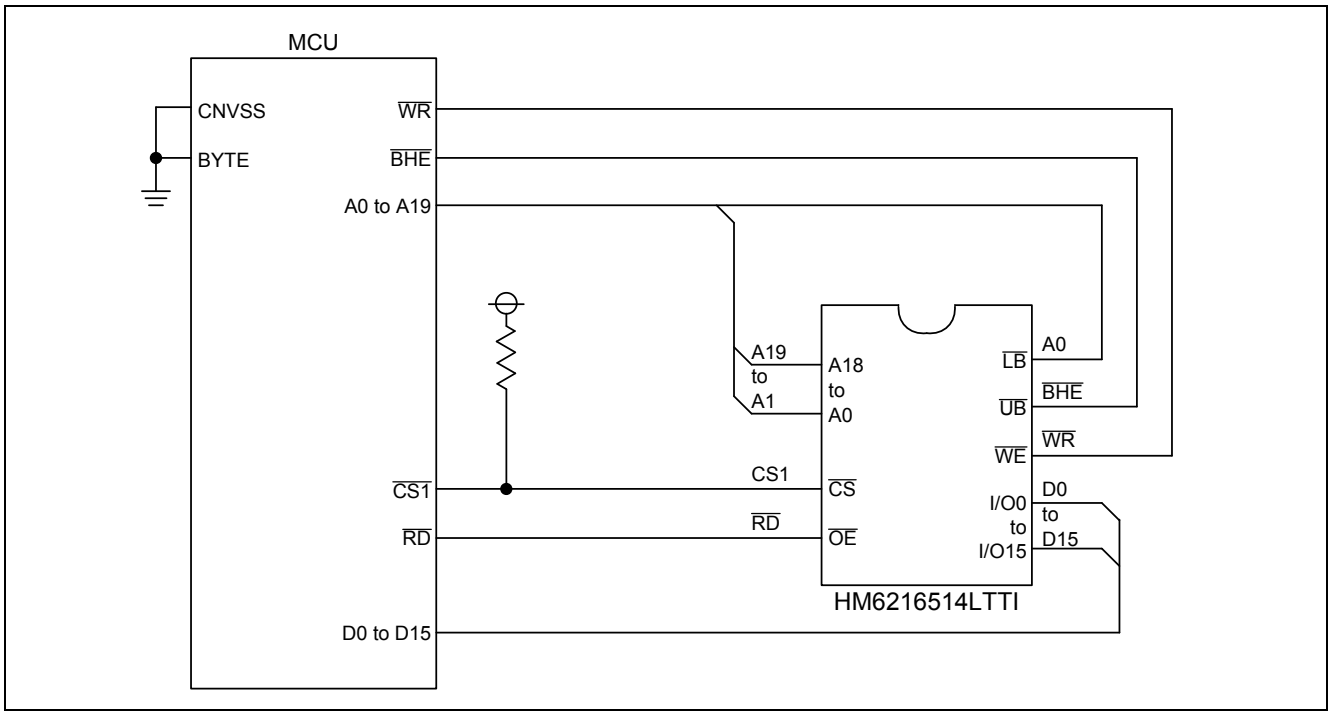


Figure 3.4 Connecting HM6216514LTTI to a 16-bit Wide Data Bus

3.3.2 Connecting 8-bit Memory to a 16-bit Wide Data Bus

Figure 3.5 shows an example of connecting two M5M5V108DVP's (SRAM) to a 16-bit data bus. In this diagram, when reset, the MCU starts operating in single-chip mode. Change this mode to memory expansion mode in a program.

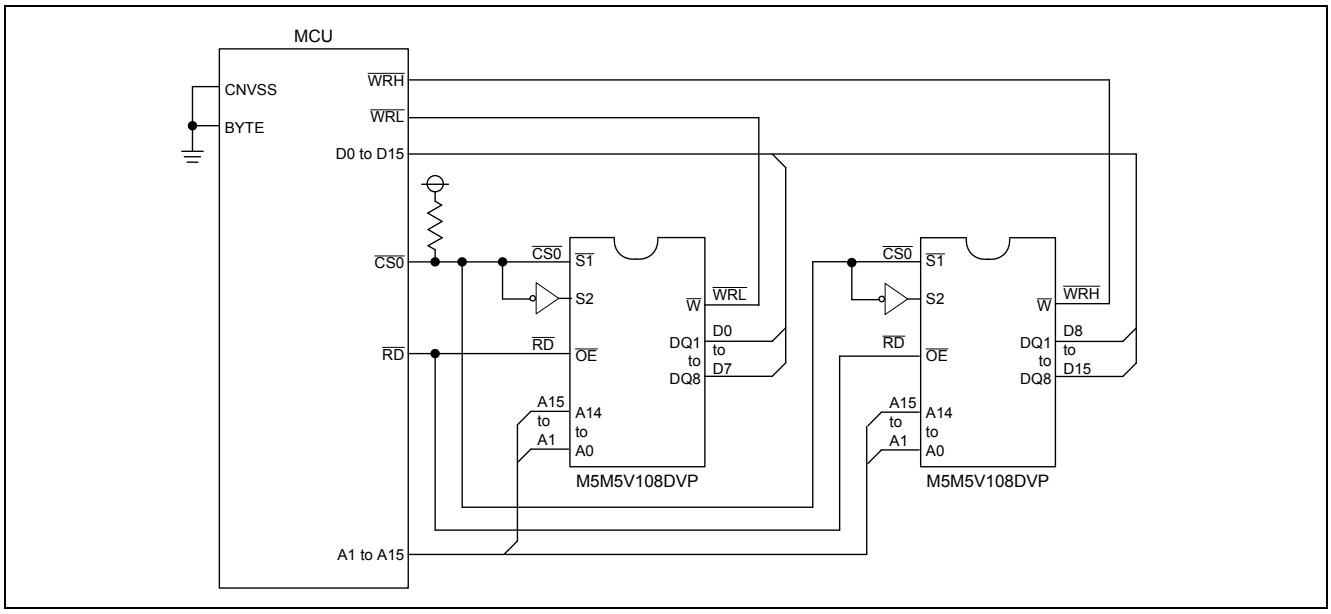


Figure 3.5 Connecting Two M5M5V108DVP's to a 16-bit Wide Data Bus

3.3.3 Connecting 8-bit Memory to an 8-bit Wide Data Bus

Figure 3.6 shows an example of connecting two M5M5V108DVP's (SRAM) to an 8-bit wide data bus. In this diagram, when reset, the MCU starts operating in single-chip mode. Change this mode to memory expansion mode in a program.

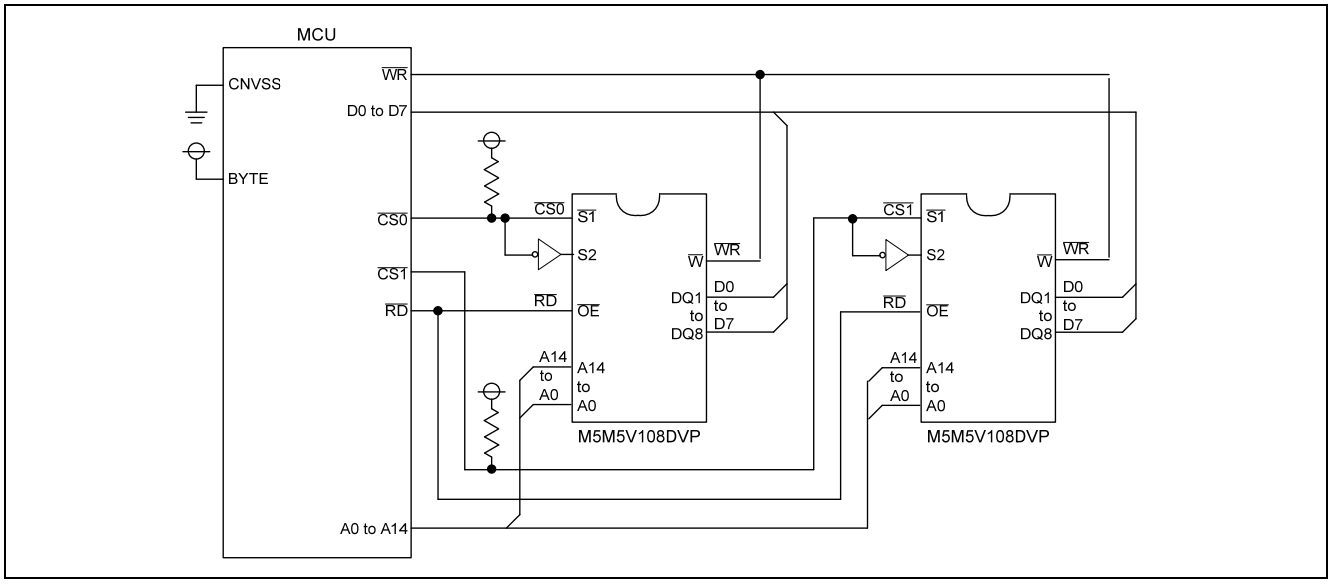


Figure 3.6 Connecting Two M5M5V108DVP's to an 8-bit Wide Data Bus

3.4 Connectable Memories

3.4.1 Operation Frequency and Access Time

Connectable memories depend upon the BCLK frequency f(BCLK). The frequency of f(BCLK) is equal to that of BCLK, and is contingent on the oscillator frequency and on the system clock select bit settings (bit 6 of CM0 register, and bits 6 and 7 of CM1 register).

(1) Read cycle time (tCR)/write cycle time (tCW)

tCR and tCW must satisfy the following conditional expressions:

• With the wait option cleared

$tCR < 10^9/f(BCLK)$ and $tCW < 10^9/f(BCLK)$

• With the wait option selected

$tCR < n \times 10^9/f(BCLK)$ and $tCW < (n+1) \times 10^9/f(BCLK)$

Note: For details on the value of n, refer to Table 3.1.

(2) Address access time [ta(A)]

ta(A) must satisfy the following conditional expressions:

(a) Vcc = 5 V

• With the wait option cleared

$ta(A) < 10^9/f(BCLK) - 65(ns)$*

• With the wait option selected

$ta(A) < n \times 10^9/f(BCLK) - 65(ns)$*

* 65(ns) = td(BCLK – AD) + tsu(DB – RD) – th(BCLK – RD)
= (address output delay time) + (data input setup time) – (RD signal output hold time)

(b) Vcc = 3 V

• With the wait option cleared

$ta(A) < 10^9/f(BCLK) - 80(ns)$*

• With the wait option selected

$ta(A) < n \times 10^9/f(BCLK) - 80(ns)$*

* 80(ns) = td(BCLK-AD) + tsu(DB – RD) – th(BCLK – RD)
= (address output delay time) + (data input setup time) – (RD signal output hold time)

Note: For details on the value of n, refer to Table 3.1.

(3) Chip select access time [ta(S)]

ta(S) must satisfy the following conditional expressions:

(a) Vcc = 5 V

• With the wait option cleared

$ta(S) < 10^9/f(BCLK) - 65(ns)$*

• With the wait option selected

$ta(S) < n \times 10^9/f(BCLK) - 65(ns)$*

* 65(ns) = td(BCLK – CS) + tsu(DB – RD) – th(BCLK – RD)
= (chip select output delay time) + (data input setup time) – (RD signal output hold time)

(b) Vcc = 3 V

• With the wait option cleared

$ta(S) < 10^9/f(BCLK) - 80(ns)$*

• With the wait option selected

$ta(S) < n \times 10^9/f(BCLK) - 80(ns)$*

* 80(ns) = td(BCLK – CS) + tsu(DB – RD) – th(BCLK – RD)
= (chip select output delay time) + (data input setup time) – (RD signal output hold time)

Note: For details on the value of n, refer to Table 3.1.

(4) Output enable time [ta(OE)]

ta(OE) must satisfy the following conditional expressions:

(a) Vcc = 5 V

• When no waits are inserted

ta(OE) < 0.5 $\times 10^9$/f(BCLK) – 45(ns) = tac1(RD-DB)

• When one to three waits are inserted

ta(OE) < (n + 0.5) $\times 10^9$/f(BCLK) – 45(ns) = tac2(RD-DB)

Note: n is 1 when inserting one wait, 2 when inserting two waits, and 3 when inserting three waits.

• When accessing a multiplexed bus area

ta(OE) < (n - 0.5) $\times 10^9$/f(BCLK) – 45(ns) = tac3(RD-DB)

Note: n is 2 when inserting two waits, and 3 when inserting three waits.

• When setting 2φ + 3φ or more

ta(OE) < n $\times 10^9$/f(BCLK) – 45(ns) = tac4(RD-DB)

Note: n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

(b) Vcc = 3 V

• When no waits are inserted

ta(OE) < 0.5 $\times 10^9$/f(BCLK) – 60(ns) = tac1(RD-DB)

• When one to three waits are inserted

ta(OE) < (n + 0.5) $\times 10^9$/f(BCLK) – 60(ns) = tac2(RD-DB)

Note: n is 1 when inserting one wait, 2 when inserting two waits, and 3 when inserting three waits.

• When accessing a multiplexed bus area

ta(OE) < (n - 0.5) $\times 10^9$/f(BCLK) – 60(ns) = tac3(RD-DB)

Note: n is 2 when inserting two waits, and 3 when inserting three waits.

• When setting 2φ + 3φ or more

ta(OE) < n $\times 10^9$/f(BCLK) – 60(ns) = tac4(RD-DB)

Note: n is 3 for 2φ + 3φ, 4 for 2φ + 4φ, 4 for 3φ + 4φ, and 5 for 4φ + 5φ.

(5) Data setup time [tsu(D)]

tsu(D) must satisfy the following conditional expressions:

(a) Vcc = 5 V

• With the wait option cleared

tsu(D) < 10^9/(f(BCLK)×2) – 40(ns)*

• With the wait option selected

tsu(D) < (n+1)×10^9/(f(BCLK)×2) – 40(ns)*

* 40(ns) = td(BCLK – DB) – th(BCLK – WR)
= (data output delay time) – (WR signal output hold time)

(b) Vcc = 3 V

• With the wait option cleared

tsu(D) < 10^9/(f(BCLK)×2) – 40(ns)*

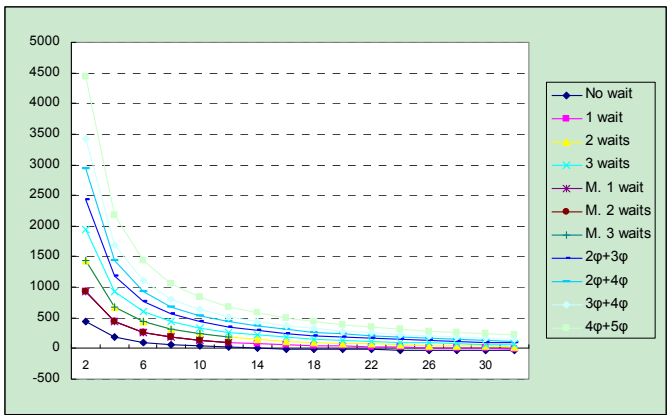
• With the wait option selected

tsu(D) < (n+1)×10^9/(f(BCLK)×2) – 40(ns)*

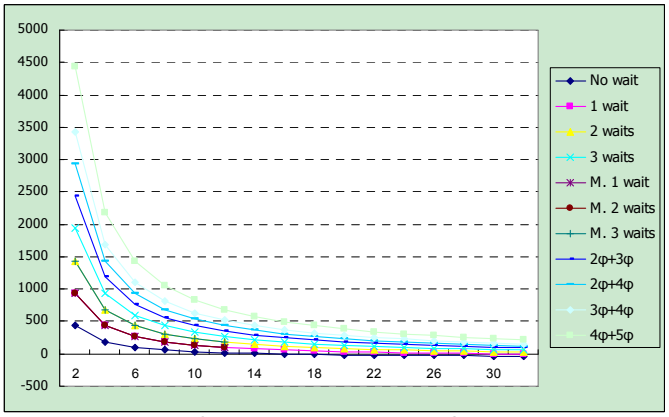
* 40(ns) = td(BCLK – DB) – th(BCLK – WR)
= (data output delay time) – (WR signal output hold time)

Note: n is 1 when inserting one wait, 2 when inserting two waits, and 3 when inserting three waits.

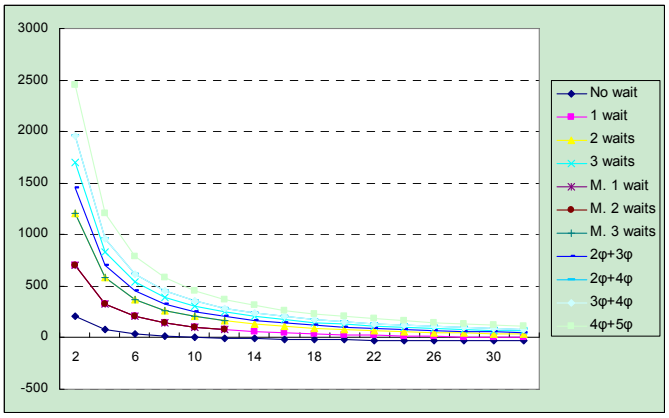
See Figure 3.7 and Figure 3.8 for details. In the figures below, "M." means "When Accessing with a Multiplexed Bus".



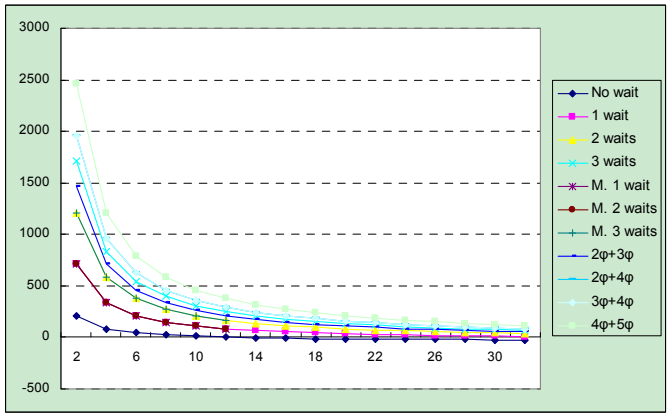
Address access time [ta(A)]



Chip select access time [ta(S)]

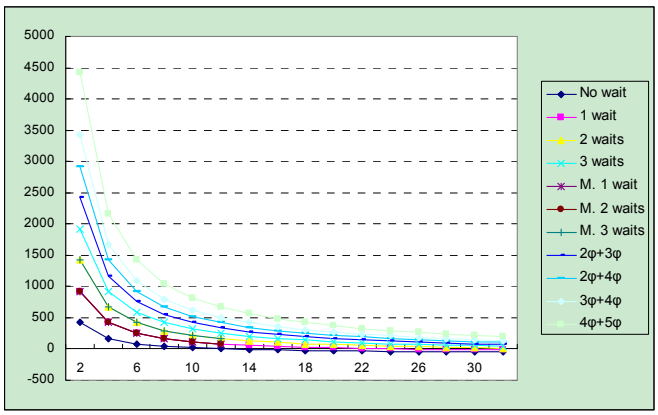


Output enable time [ta(OE)]

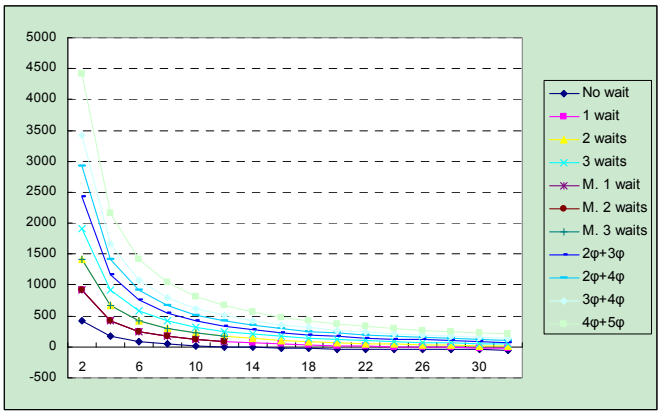


Data setup time [tsu(D)]

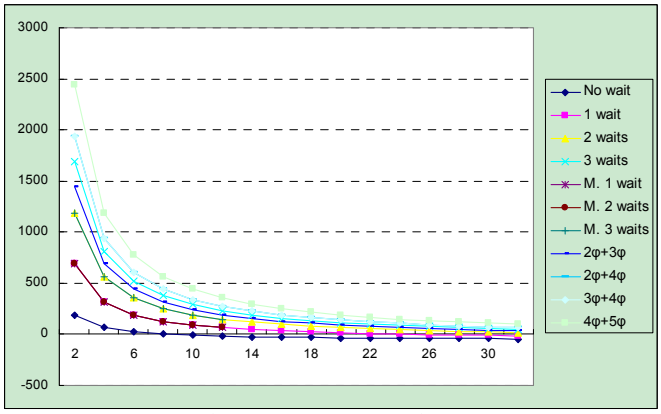
Figure 3.7 Relation between the BCLK Frequency and Memory When Vcc = 5 V



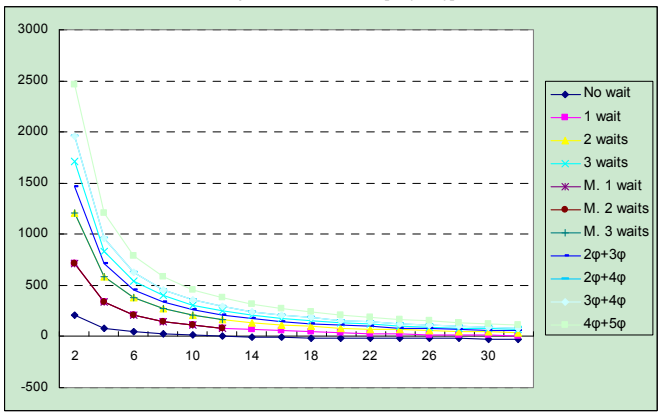
Address access time [ta(A)]



Chip select access time [ta(S)]



Output enable time [ta(OE)]



Data setup time [tsu(D)]

Figure 3.8 Relation between the BCLK Frequency and Memory When Vcc = 3 V

3.4.2 Connecting Low-Speed Memory

To connect memory with long address access time [ta(A)], either decrease the frequency of BCLK or insert a software wait. Use the $\overline{RDY}$ feature to connect memory having the timing that precludes connection though a software wait is inserted.

(1) Using software wait

The PM17 bit in the PM1 register, which is a software-wait-related bit, affects both the internal memory and the external area.

Software waits can be inserted to an external area by setting the PM17 bit in the PM1 register, setting the CSiW bit in the CSR register, and bits CSEi1W to CSEi0W in the CSE register for each $\overline{CSi}$ (i = 0 to 3). To use the $\overline{RDY}$ signal, set the corresponding CSiW bit to 0 (wait state). See Table 3.1 "Bits and Bus Cycles Related to Software Wait States (External Area)" for details.

Table 3.1 Bits and Bus Cycles Related to Software Wait States (External Area)

Area	Bus Mode	Setting of Software-Wait-Related Bits				Software Wait Cycles	Bus Cycles
		PM17	CSiW	CSEi1W to CSEi0W	EWCi1 to EWCi0		
External area	Separate bus	0	1	00b	-	None	1 BCLK cycle (read)
							2 BCLK cycles (write)
		-	0	00b	-	1 (1φ + 1φ)	2 BCLK cycles (4)
		-	0	01b	-	2 (1φ + 2φ)	3 BCLK cycles
		-	0	10b	-	3 (1φ + 3φ)	4 BCLK cycles
		-	0	11b	00b	(2φ + 3φ)	5 BCLK cycles
					01b	(2φ + 4φ)	6 BCLK cycles
					10b	(3φ + 4φ)	7 BCLK cycles
					11b	(4φ + 5φ)	9 BCLK cycles
		1	0 (3)	00b	-	1 (1φ + 1φ)	2 BCLK cycles
	Multiplexed bus	-	0 (2)	00b	-	1 (5)	3 BCLK cycles
		-	0 (2)	01b	-	2	3 BCLK cycles
		-	0 (2)	10b	-	3	4 BCLK cycles
		1	0 (2, 3)	00b	-	1 (5)	3 BCLK cycles

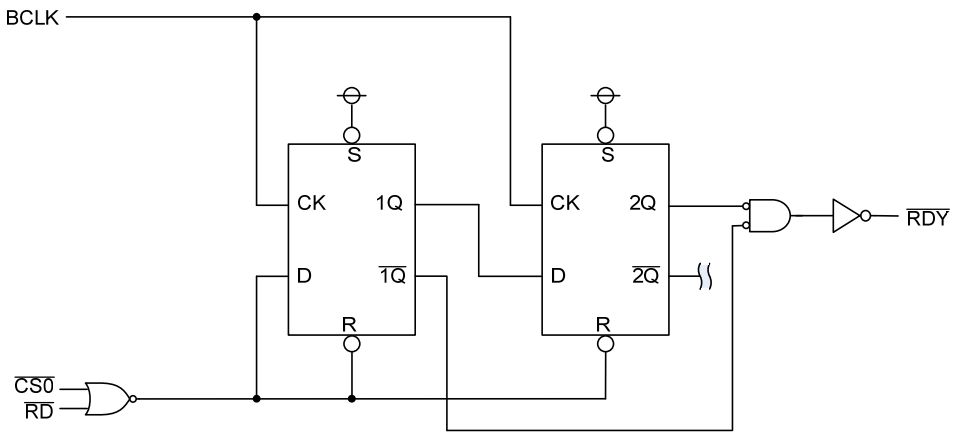
i = 0 to 3
− indicates that either 0 or 1 can be set.
PM17: Bit in the PM1 register
CSiW: Bits in the CSR register (1)
CSEi1W and CSEi0W: Bits in the CSE register
EWCi1 and EWCi0: Bits in the EWC register
Notes:
1. To use the $\overline{RDY}$ signal, set the CSiW bit to 0 (wait state).
2. When accessing with a multiplexed bus, set the CSiW bit to 0 (wait state).
3. To access an external area when the PM17 bit is 1, set the CSiW bit to 0 (wait state).
4. After reset, the PM17 bit is set to 0 (no wait state), bits CS0W to CS3W are set to 0 (wait state), and the CSE register is set to 00h (one wait state for $\overline{CS0}$ to $\overline{CS3}$). Therefore, all external areas are accessed with one wait state.
5. When setting one wait in the multiplexed bus, the bus cycle is the same as two waits.

(2) $\overline{RDY}$ function usage

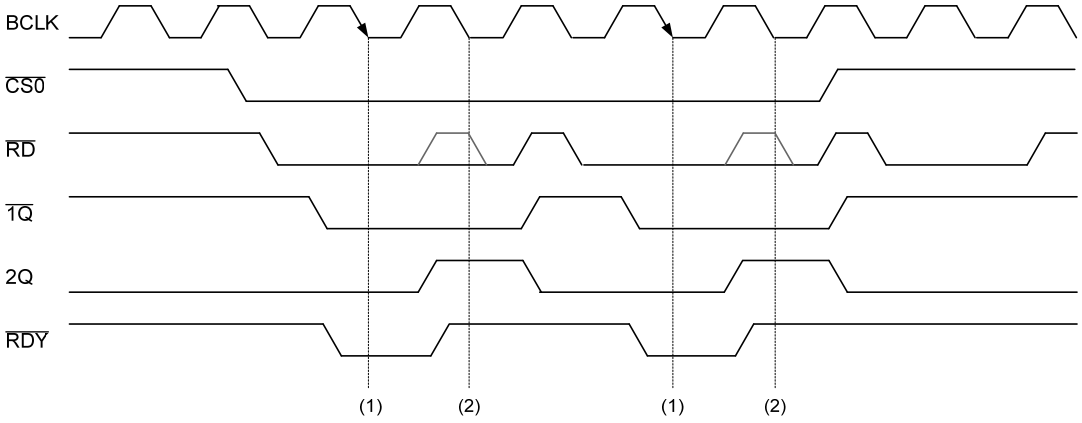
To use the $\overline{RDY}$ function, insert a software wait.

The $\overline{RDY}$ function operates when the BCLK signal falls while the $\overline{RDY}$ pin is low; the bus does not vary for one BCLK cycle, and the state at that moment is held.

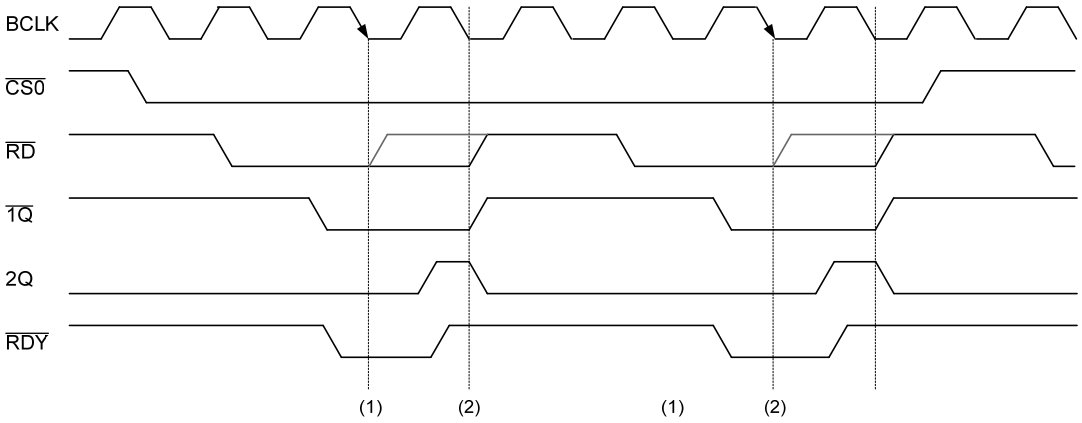
The $\overline{RDY}$ function holds the state of bus for the period in which the $\overline{RDY}$ pin is low, and releases it when the BCLK signal falls while the $\overline{RDY}$ pin is high. Figure 3.9 shows an example of the $\overline{RDY}$ circuit f(XIN)=10 MHz that holds the state of bus for one BCLK cycle.



• Separate bus



• Multiplexed bus



(1) $\overline{RDY}$ accepted
(2) $\overline{RDY}$ cleared
The state of data bus and that of address bus are held for the period between (1) and (2).

Figure 3.9 $\overline{RDY}$ Circuit Holding State of Bus for One BCLK f(XIN) = 10 MHz

3.4.3 Connectable Memories

Connectable memories and their maximum frequencies are below.

The maximum frequency for the M16C/65 Group is 32 MHz when Vcc = 2.7 to 5.5 V.

In the tables below, "M." means "When Accessing with a Multiplexed Bus".

(1) 5 V

(a) When no waits are inserted

Maximum Frequency (MHz)	Model No.
6	HM6216514LTTI-5SL

(b) When one to three waits are inserted

Maximum Frequency (MHz)			Model No.
1 wait	2 waits	3 waits	
16	25	– (1)	HM6216514LTTI-5SL

(c) When accessing a multiplexed bus area

Maximum Frequency (MHz)			Model No.
M. 1 wait	M. 2 waits	M. 3 waits	
12.5	12.5	12.5	HM6216514LTTI-5SL

(d) When setting 2φ + 3φ or more

Maximum frequency (MHz)				Model No.
2φ + 3φ	2φ + 4φ	3φ + 4φ	4φ + 5φ	
– (1)	– (1)	– (1)	– (1)	HM6216514LTTI-5SL

(2) 3 V

(a) When no waits are inserted

Maximum Frequency (MHz)	Model No.
5	M5M5V108DVP-70HI

(b) When one to three waits are inserted

Maximum Frequency (MHz)			Model No.
1 wait	2 waits	3 waits	
13	20	26	M5M5V108DVP-70HI

(c) When accessing a multiplexed bus area

Maximum Frequency (MHz)			Model No.
M. 1 wait	M. 2 waits	M. 3 waits	
12.5	12.5	12.5	M5M5V108DVP-70HI

(d) When setting 2φ + 3φ or more

Maximum Frequency (MHz)				Model No.
2φ + 3φ	2φ + 4φ	3φ + 4φ	4φ + 5φ	
31	– (1)	– (1)	– (1)	M5M5V108DVP-70HI

Note:
1. "-" means no limitation, the maximum frequency for the M16C/65 Group is 32 MHz.

Website and Support

Renesas Electronics Website
http://www.renesas.com/

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Revision History

Rev.	Date	Description	
		Page	Summary
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   - The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     - In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   - Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   - After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   - Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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