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M16C/64A,64C,65,65C,5LD,56D Groups

Procedure for Using PLL Clock as CPU Clock Source

APPLICATION NOTE

1. Abstract

This application note describes the procedure for changing the CPU clock source from the 125 kHz on-chip oscillator clock divided-by-8 to the PLL clock not divided. The examples are explained below using the M16C/64A and M16C/65 Groups.

The PLL clock is generated by the PLL frequency synthesizer (one of the four clock generators). Table 1.1 lists the Specifications of Main Clock Generator and PLL Frequency Synthesizer.

ltem	Main Clock generator	PLL Frequency Synthesizer
Application	CPU clock source Peripheral function clock source	CPU clock source Peripheral function clock source
Clock frequency	0 to 20 MHz	M16C/64A: 10 to 25 MHz M16C/65: 10 to 32 MHz
Connectable oscillators	Ceramic resonator Crystal resonator	— (See Note 1)
Pins connecting to oscillator	XIN, XOUT	— (See Note 1)
Oscillator stop/restart function	Yes	Enabled
Oscillator status after reset	Oscillating	Stopped
Other	An externally generated clock can be input.	— (See Note 1)

Table 1.1 Specifications of Main Clock Generator and PLL Frequency Synthesizer

Note:

1. The PLL frequency synthesizer uses the main clock oscillation circuit as a reference clock source. The items above are based on the main clock oscillation circuit.

2. Introduction

The application example presented in this document applies to the microcomputers (MCUs) listed below.

MCU(s): M16C/64A, M16C/64C, M16C/65, M16C/65C, M16C/5LD, M16C/56D Groups

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.



3. Description of the Application Example

The PLL clock is generated from the main clock by the PLL frequency synthesizer. Figure 3.1 shows the Relation between Main Clock and PLL Clock.

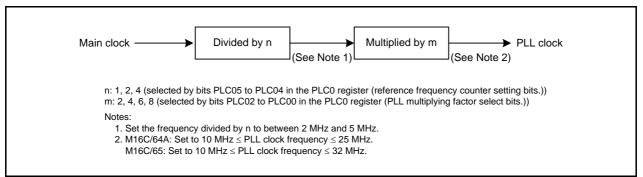


Figure 3.1 Relation between Main Clock and PLL Clock

Bits PLC05 to PLC04 and bits PLC02 to PLC00 can be set only once after reset. Table 3.1 lists the Example Settings for PLL Clock Frequencies.

 Table 3.1
 Example Settings for PLL Clock Frequencies

Main Clock (XIN)	Setting	PLL Clock		
	Bits PLC05 to PLC04	Bits PLC02 to PLC00		
10 MHz	01b (divide-by-2)	010b (multiply-by-4)	20 MHz	
5 MHz	00b (not divided)	010b (multiply-by-4)		
12 MHz	10b (divide-by-4)	100b (multiply-by-8)	24 MHz	
6 MHz	01b (divide-by-2)	100b (multiply-by-8)		
16 MHz	10b (divide-by-4)	100b (multiply-by-8)	32 MHz ⁽¹⁾	
8 MHz	01b (divide-by-2)	100b (multiply-by-8)		

Note:

1. This setting only applies to the M16C/65 Group.



Figure 3.2 shows the Procedure for Using PLL clock as CPU Clock Source.

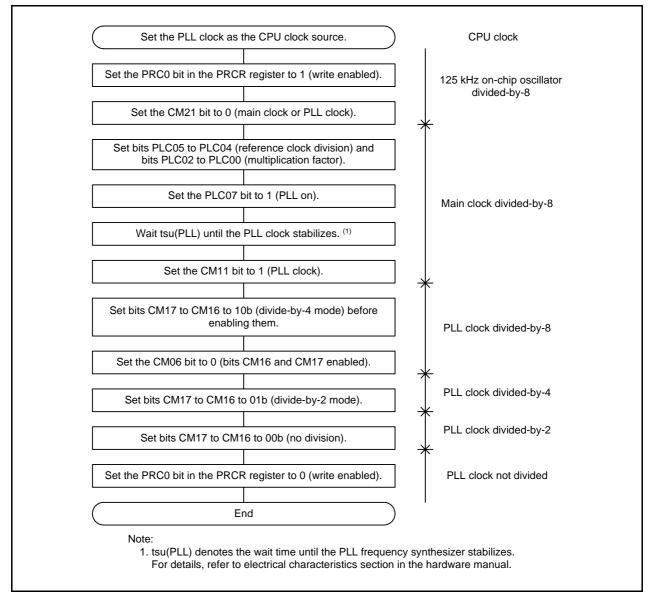


Figure 3.2 Procedure for Using PLL clock as CPU Clock Source



4. Settings

Figure 4.1 to Figure 4.2 show the setting procedure and setting values to execute "Procedure for Using PLL Clock as CPU Clock Source". Refer to the M16C/64A, M16C/65 Group User's Manual Hardware for each register and more details.

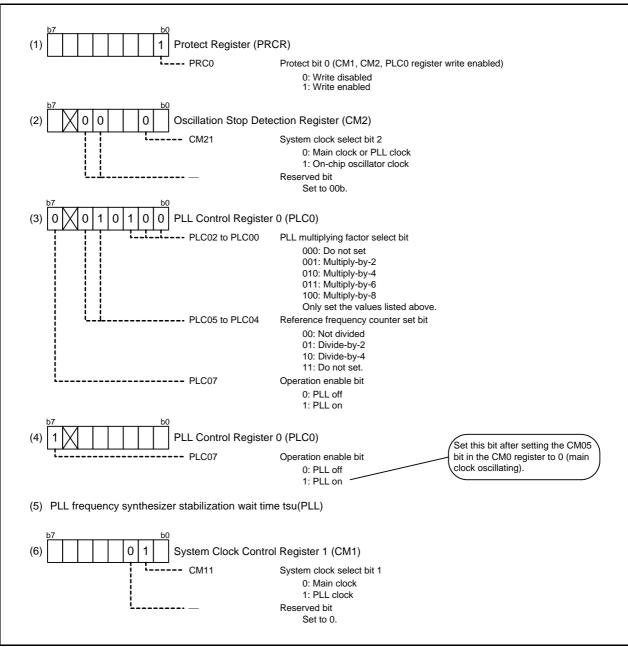


Figure 4.1 Procedure for Using PLL Clock as CPU Clock Source (1/2)

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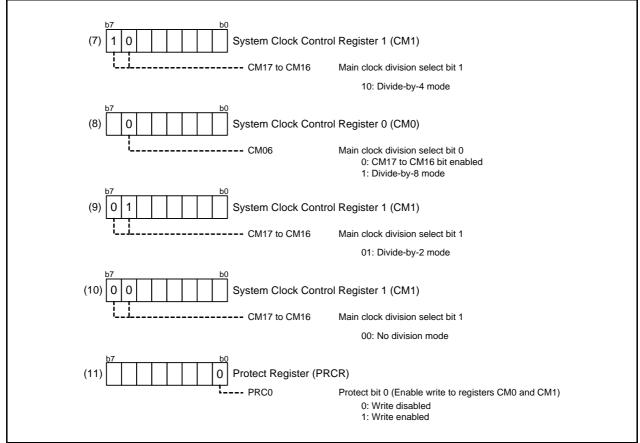


Figure 4.2 Procedure for Using PLL Clock as CPU Clock Source (2/2)



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

M16C/64A Group User's Manual: Hardware Rev.2.00 M16C/64C Group User's Manual: Hardware Rev.1.00 M16C/65 Group User's Manual: Hardware Rev.2.00 M16C/65C Group User's Manual: Hardware Rev.1.00 M16C/5LD Group, M16C/56D User's Manual: Hardware Rev.1.10 The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual M16C Series, R8C Family C Compiler Package V.5.45 C Compiler User's Manual Rev.2.00 The latest version can be downloaded from the Renesas Electronics website.

7. Website and Support

Renesas Electronics website http://www.renesas.com/

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Revision His

M16C/64A,64C,65,65C,5LD,56D Groups Procedure for Using PLL Clock as CPU Clock Source

Rev. Dat	Data		Description	
	Dale	Page	Summary	
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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