
M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups

Operation of Serial I/O (Transmission in UART Mode)

R01AN0542EC0101

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1. Abstract

In transmitting data in UART mode, choose functions from those listed in Table 3.1. Operations of the marked items are described below. The examples are explained below using the M16C/65 Group.

2. Introduction

This application note is applied to the following MCUs:

MCU(s): M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen Function

Table 3.1 Chosen Functions

Item	Set-up	Item	Set-up
Clock prior to division select	✓ f1	Transmission interrupt factor	Transmission buffer empty
	fOCO-F		✓ Transmission complete
Peripheral clock	✓ f1SIO	Data logic select function	✓ No reverse
	f2SIO		Reverse
Transfer clock source	✓ Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	TXD, RXD I/O polarity reverse bit	✓ No reverse
	External clock (CLKi pin)		Reverse
CTS function	✓ CTS function enabled	Separate CTS/RTS pins ⁽¹⁾	✓ Shared pin
	CTS function disable		Separated

Note:

1. This function separates $\overline{\text{CTS0}}/\overline{\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and inputs $\overline{\text{CTS0}}$ from the P6_4 pin. When this function is selected, UART1 $\overline{\text{CTS}}/\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit to "1".

4. Operation

- (1) Setting the transmit enable bit to "1" and writing transmission data to the UARTi transmit buffer register readies the data transmissible status.
- (2) When input to the $\overline{\text{CTS}}_i$ pin goes to "L", transmission starts (the $\overline{\text{CTS}}_i$ pin needs to be controlled on the reception side).
- (3) Transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the TxDi pin. Then, data is transmitted, bit by bit, in sequence: LSB, ..., MSB, parity bit, and stop bit(s).
- (4) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to "1", which indicates that transmission is completed. At this time, the UARTi transmit interrupt request bit goes to "1". The transfer clock stops at "H" level.
- (5) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.

Figure 4.1 shows the operation timing.

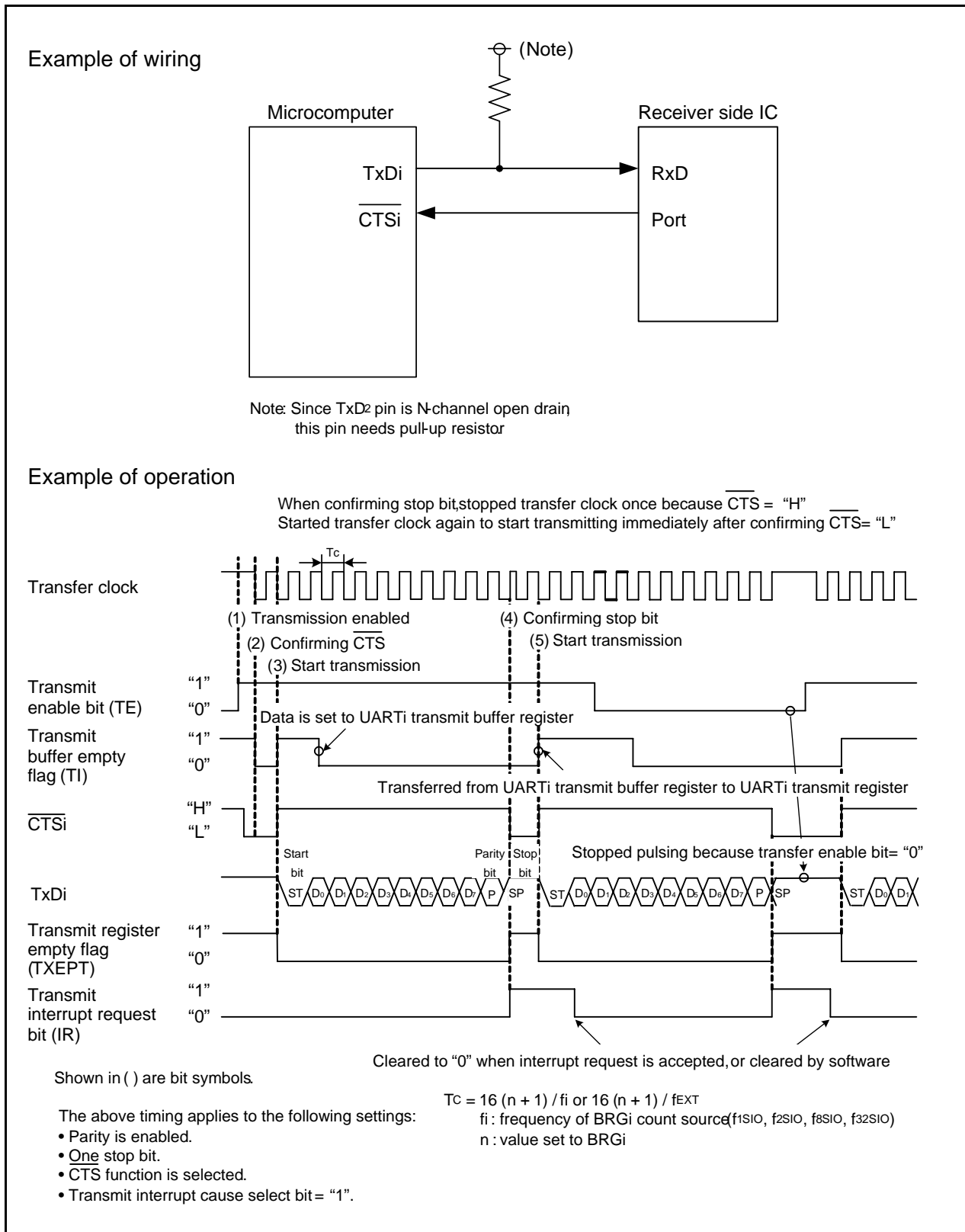
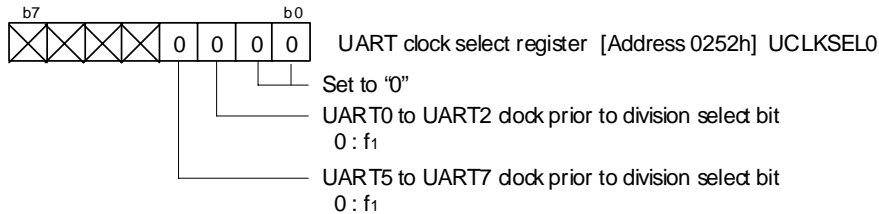


Figure 4.1 Operation Timing of Transmission in UART Mode

5. Set-up Procedure

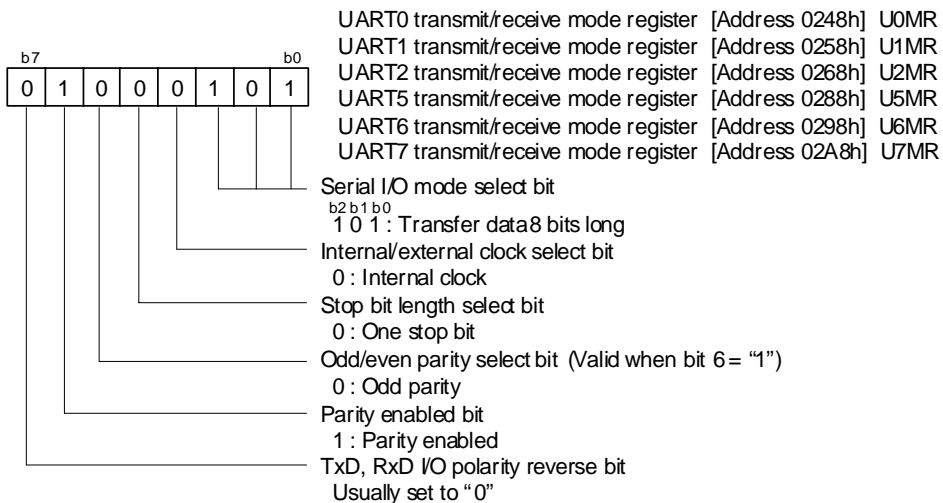
Setting UART clock select register

(Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.)

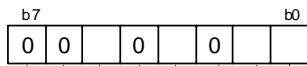


Note: Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.

Setting UART_i transmit/receive mode register (i = 0 to 2, 5 to 7)



Setting UART_i transmit/receive control register (i = 0 to 2, 5 to 7)



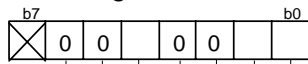
- UART0 transmit/receive control register [Address 024Ch] U0C0
- UART1 transmit/receive control register [Address 025Ch] U1C0
- UART2 transmit/receive control register [Address 026Ch] U2C0
- UART5 transmit/receive control register [Address 028Ch] U5C0
- UART6 transmit/receive control register [Address 029Ch] U6C0
- UART7 transmit/receive control register [Address 02ACh] U7C0

- UIBRG count source select bit
 - b1 b0
 - 0 0 : f_{1SIO} or f_{2SIO} is selected (Note1)
 - 0 1 : f_{8SIO} is selected
 - 1 0 : f_{32SIO} is selected
 - 1 1 : Do not set to this value
- CTS/RTS function select bit (Valid when bit4 = "0")
 - 0 : CTS function is selected (Note2)
- Transmit register empty flag
 - 0 : Data present in transmit register (during transmission)
 - 1 : No data present in transmit register (transmission completed)
- CTS/RTS disable bit
 - 0 : CTS/RTS function enabled
- Data output select bit
 - 0 : Pins TxDi/SDAi and SCLi are CMOS output
 - 1 : Pins TxDi/SDAi and SCLi are N-channel open-drain output
- Must always be "0" in UART mode
- Transfer format select bit
 - 0 : LSB first

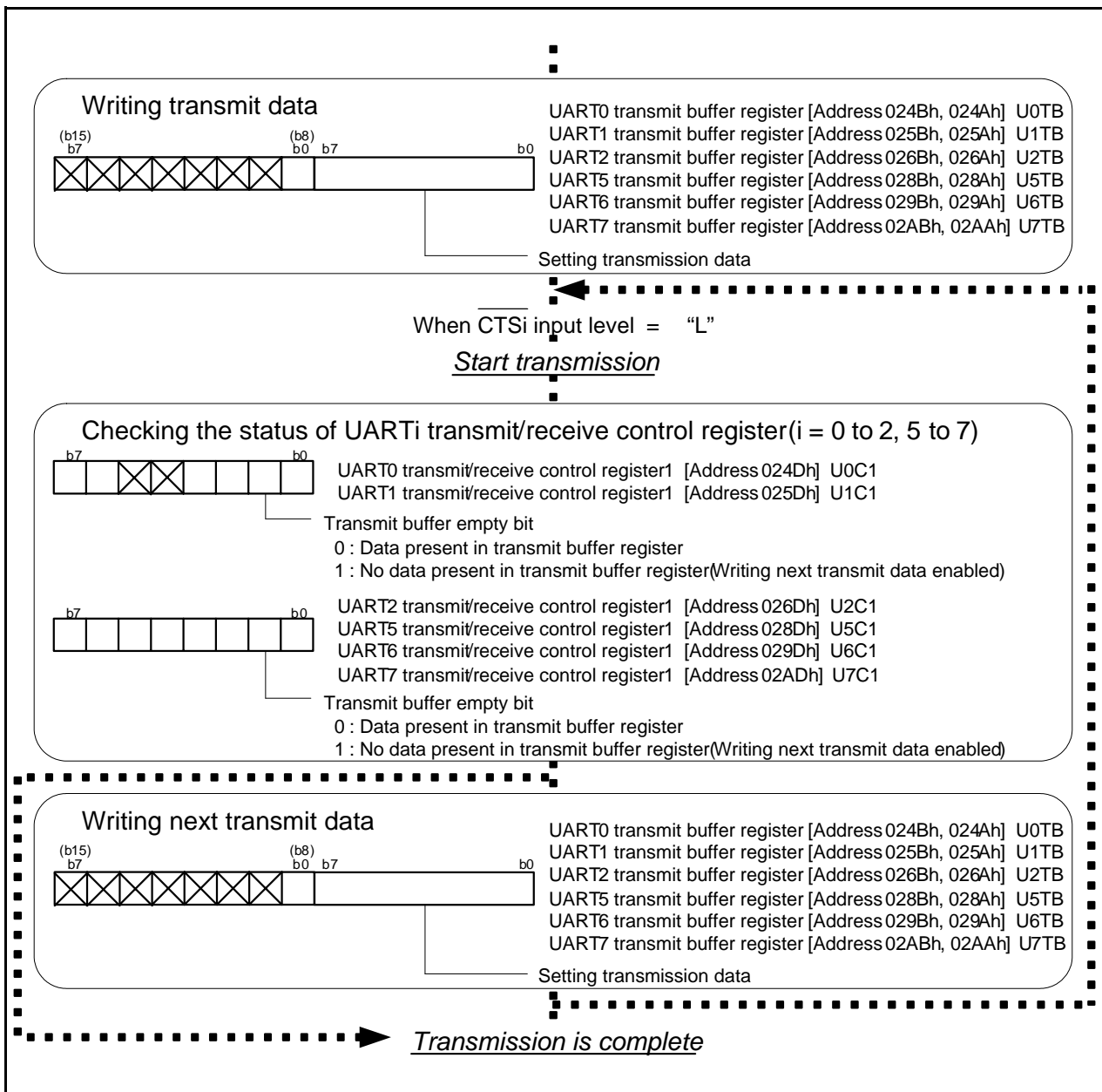
Note 1: When the PCLK1 bit in the PCLKR register is "1", the selected clock source is f_{1SIO}. When the PCLK1 bit is "0", the selected clock source is f_{2SIO}.

Note 2: Set the corresponding port direction register to '0' (input mode).

Setting UART transmit/receive control register 2



- UART transmit/receive control register 2 [Address 0250h] UCON
- UART0 transmit Interrupt cause select bit
 - 1 : Transmission completed (TXEPT = 1)
- UART1 transmit Interrupt cause select bit
 - 1 : Transmission completed (TXEPT = 1)
- Must always be "0" in UART mode
- Must always be "0" in UART mode
- Invalid in UART mode
- Must always be "0" in UART mode
- Separate UART0 CTS/RTS bit
 - 0 : CTS/RTS shared pin



6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.2.00
M16C/64A Group User's Manual: Hardware Rev.2.00
M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65 Group User's Manual: Hardware Rev.2.00
M16C/65C Group User's Manual: Hardware Rev.1.00
M16C/6C Group User's Manual: Hardware Rev.2.00
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev.1.10
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev.1.00
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

M16C Series, R8C Family C Compiler Package V.5.45

C Compiler User's Manual Rev.2.00

The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

Renesas Electronics website

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Revision History	M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups Operation of Serial I/O (Transmission in UART Mode)
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Rev.	Date	Description	
		Page	Summary
1.00	Oct. 30, 2009	—	First edition issued
1.01	Apr. 28, 2011	—	Add: M16C/63, M16C/64A, M16C/64C, M16C/65C, M16C/6C, M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/5M, and M16C/57

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-586-6000, Fax: +1-408-586-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6276-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141