M16C/63, 64A, 64C, 65, 65C Groups

Remote Control Signal Receiver Receiving Two Separate Formats

R01AN0353EC0100
Rev. 1.00
Mar. 31, 2011

Abstract

In this application note, an example of receiving two kinds of remote control signal formats is shown using pattern match mode of the remote control signal receiver.

Products

MCUs: M16C/63 Group
M16C/64A Group
M16C/64C Group
M16C/65 Group
M16C/65C Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This application note describes receiving two separate formats of remote control signals: "pattern A (with header pattern and repeat code)" and "pattern B (with special header pattern)".

Table 1.1 shows the peripheral functions and their applications.
Figure 1.1 and Figure 1.2 show the waveforms of pattern A and pattern B, respectively.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
PMC0 circuit	Receive pattern A header pattern and data (see section 4.2)
PMC1 circuit	Receive pattern B header pattern and data (see section 4.3)
Timer B2	Receive pattern A repeat code (see section 4.2)

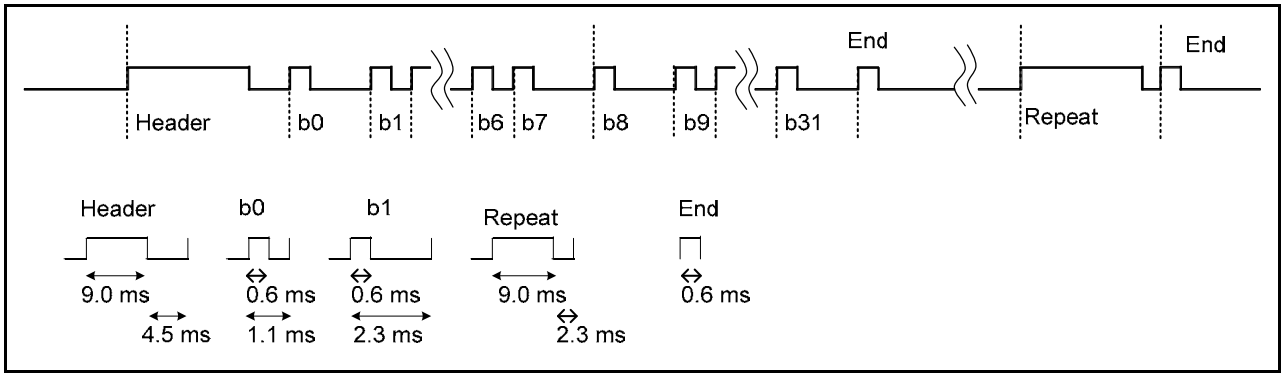


Figure 1.1 Pattern A: Remote Control Format with Header Pattern and Repeat Code

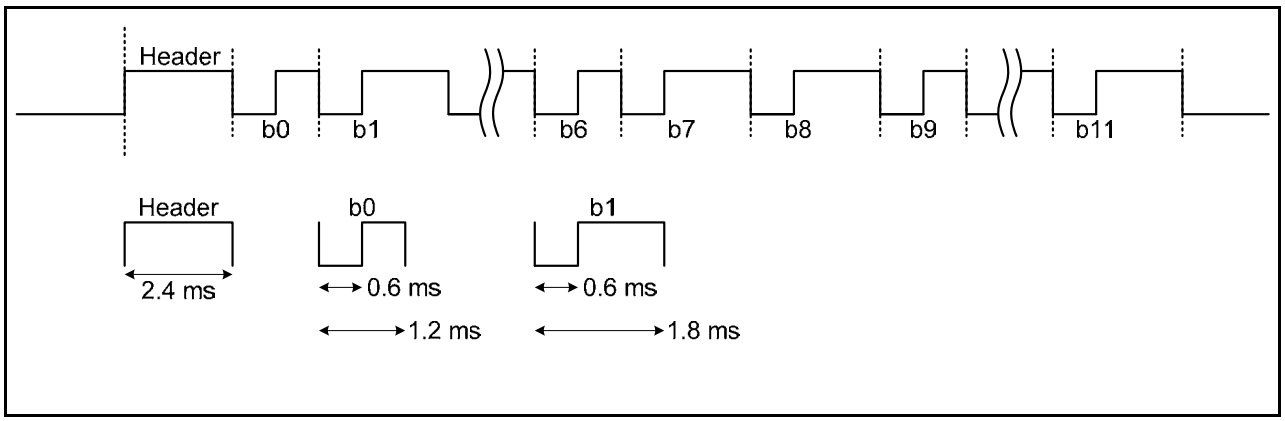


Figure 1.2 Pattern B: Remote Control Format with Special Header Pattern

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	M16C/65 Group (Program ROM 1: 256 KB)
Operating frequency	20 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics products High-performance Embedded Workshop V.4.08.00
C compiler	Renesas Electronics products M16C Series, R8C Family C Compiler V.5.45 Release 01
Operating mode	Single-chip mode

3. Reference Application Note

The application note associated with this application note is listed below. Refer to this application note for additional information.

- M16C/63, 64A, 65 Groups Remote Control Signal Receiver Setting by Format Type (R01AN0390EJ0100)

4. Hardware

4.1 Pins Used

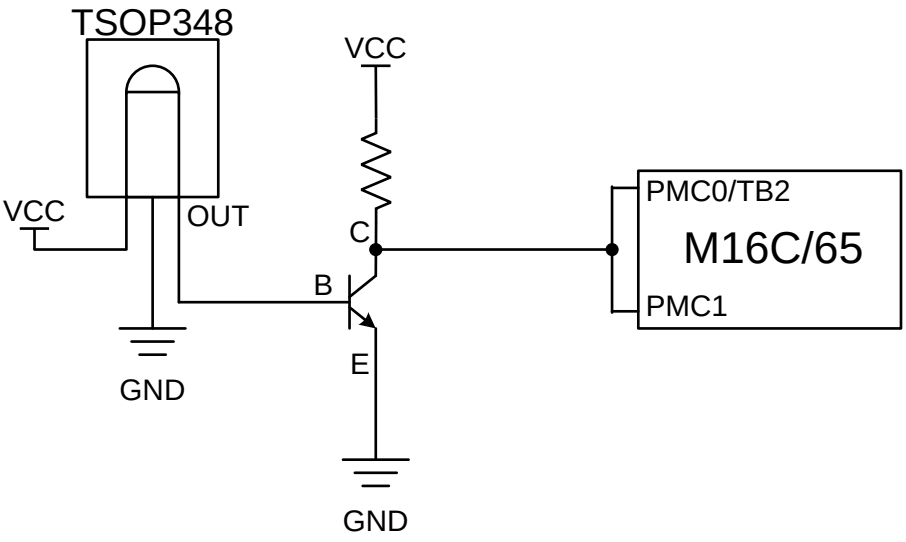
Table 4.1 lists the used pins and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P9_2/TB2IN/PMC0	Input	Input of pattern A remote control signal
P9_1/PMC1	Input	Input of pattern B remote control signal

4.2 Reference Circuits

Figure 4.1 shows a connection example.



As voltage at point B is low, connecting PMC0/TB2 directly to PMC1 may make it difficult to differentiate with a high. By connecting a transistor, point C, PMC0/TB2, and PMC1 are connected, and the signals can be distinguished. By doing this, the PMC0/TB2 or PMC1 signal is actually an inverted signal of the remote control signal.

Figure 4.1 Connection Example

5. Software

5.1 Operation Overview

5.1.1 Receiving Pattern A Format

The PMC0 circuit receives the header and data of the pattern A format.
Timer B2 receives the repeat code of the pattern A format.
The settings are listed below.

Table 5.1 PMC0 Circuit Settings

Item		Settings	
		PMC0 circuit	Timer B2
Count source	Clock source	fC	f1
	Division	No division	Divided by 64
Operating mode		Pattern match mode	Pulse period/pulse width measurement mode
Pattern match mode	Detection patterns	Header	Repeat code
		Data 0 or data 1 match	
	Interrupt	Completion of data reception	Active edge of measurement pulse
			Overflow
	Selected function	Input signal not inverted	
		Digital filter	
		Error flag hold	
Input pin		P9_2	

Operation

(1) Reception begins at the first rising edge of the header pattern.

(2) When receiving, data is sequentially stored bit by bit in the PMC0DATi register (i = 0 to 3).

(3) After 32-bit data is received, the data reception completion interrupt is generated if there is no change in the signal of time which is longer than the setting value in registers PMCiHDPMAX, PMCiD0PMAX, and PMCiD1PMAX (i = 0, 1).

(4)After reading the error flag in the PMC0 data reception complete interrupt, if the REFLG bit is 0 (no error occurs), disable the PMC0 circuit (set the EN bit in the PMC0CON0 register to 0) (1), and timer B2 starts counting after setting the initial value to timer B2. If the REFLG bit is 1 (error occurs), keep the PMC0 circuit enabled and timer B2 disabled, and exit the interrupt handler.

(5) If a repeat signal is received during the setting period, perform the following in the timer B2 interrupt routine: stop timer B2, reset the amount of time until the next repeat signal comes, and restart the timer B2 count.

(6) If there is no repeat signal during the setting period, the MCU enters the timer B2 overflow interrupt, the PMC0 circuit is reenabled (1), and timer B2 is disabled (2).

Notes:

1. The PMCi circuit starts operating by setting the EN bit to 1 (operation enabled) and the ENFLG bit becomes 1 (operating) (i = 0, 1). After setting the EN bit to 1, it takes up to two cycles of the count source before the ENFLG bit becomes 1. During this period, do not access bits or registers associated with the PMCi circuit except for the ENFLG bit. When the EN bit is set to 0 (operation disabled), the PMCi circuit stops operating and the ENFLG bit becomes 0 (operation stopped). After setting the EN bit to 0, it takes up to one cycle of the count source before the ENFLG bit becomes 0.
2. The MR3 bit (timer Bi overflow flag) is undefined after reset. The MR3 bit is cleared to 0 (no overflow) by writing to the TBiMR register (i = 0 to 5). The MR3 bit cannot be set to 1 by a program.

Figure 5.1 shows the status operation and interrupt generation timing of the PMC0 circuit remote control signal during reception.

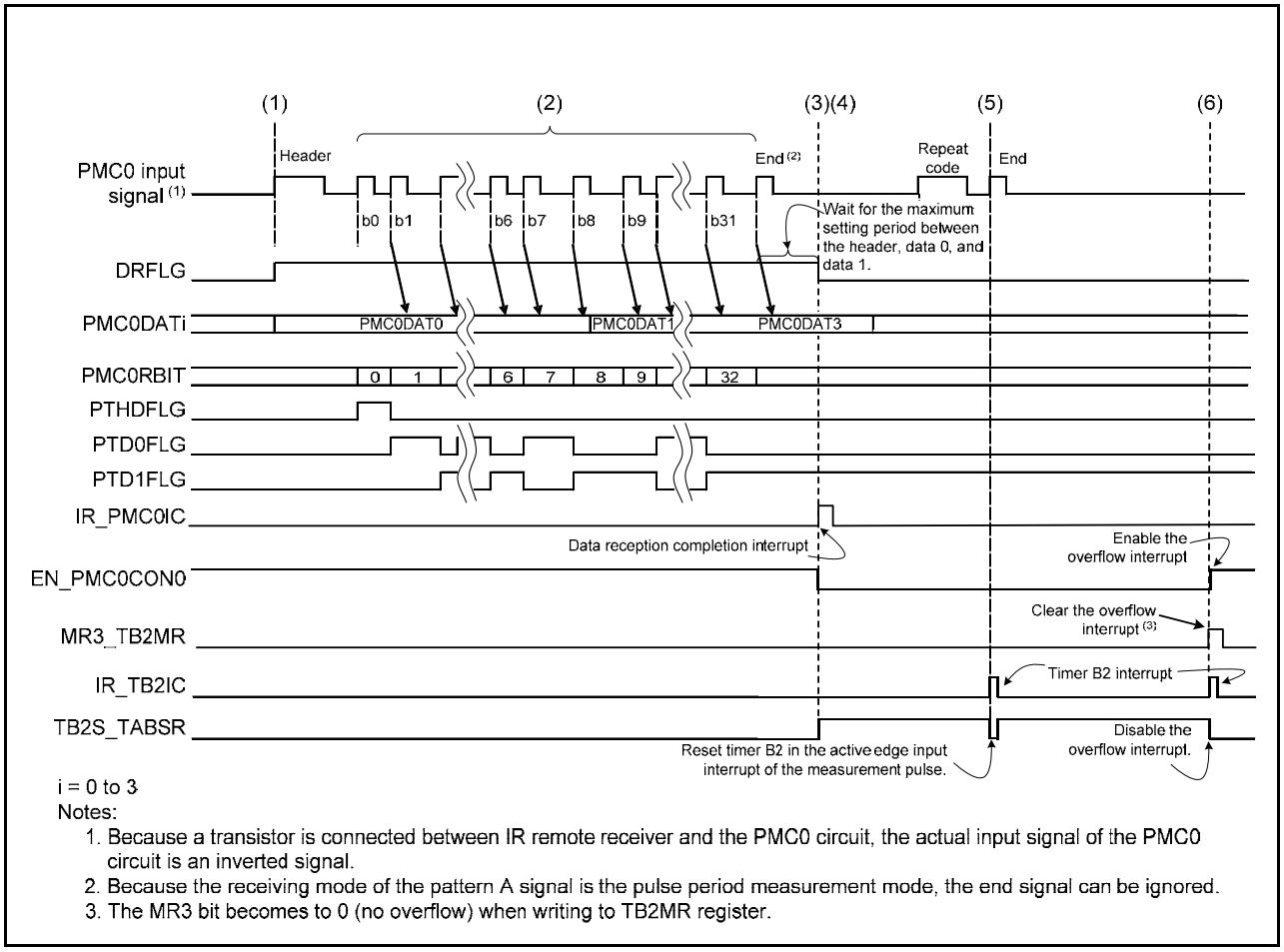


Figure 5.1 PMC0 Reception Timing of the Remote Control with Header and Repeat Code Format

5.1.2 Receiving Pattern B Format

The PMC1 circuit receives the header and data of the pattern B format.
The settings are listed below.

Table 5.2 PMC1 Circuit Settings

Item		Settings
		PMC1 circuit
Count source	Clock source	fC
	Division	No division
Operating mode		Pattern match mode
Pattern match mode	Detection patterns	Header
		Data 0 or data 1 match
	Interrupt	Header pattern match
		Data 0 or data 1 match
		Receive error
		Completion of data reception
	Selected function	Input signal not inverted
		Digital filter
		Error flag hold
Input pin		P9_1

The measurement condition of the remote control signal in pattern B is selected by setting bits TYP1 to TYP0 to 10b (pulse width measurement (between rising edge and falling edge, and falling edge and rising edge)).

The low level width and high level width of each bit are measured. Therefore, a data 0 or data 1 match interrupt is generated twice when 1 bit is received.

In this application note, the signal whose width is 0.6 ms is judged as data 0, and the signal whose width is 1.2 ms is judged as data 1.

The determination above should be performed at every data 0 and data 1 match interrupt.

The received data is encoded to bit 0 or bit 1 based on the low width and high width of each bit in the reception completion interrupt routine.

Operation

(1) Start the reception operation at the first rising edge of the header.

(2) In the header interrupt routine, enable the data 0 and data1 match interrupts, data reception completion interrupt, and reception error interrupt.

(3) In the data 0/data1 match interrupt routine, whether the data is valid or invalid is determined by the reception count value. Data is invalid at an even number of reception times, and data is valid at an odd number of reception times. When data 0/data1 is judged as valid, it is stored sequentially (1).

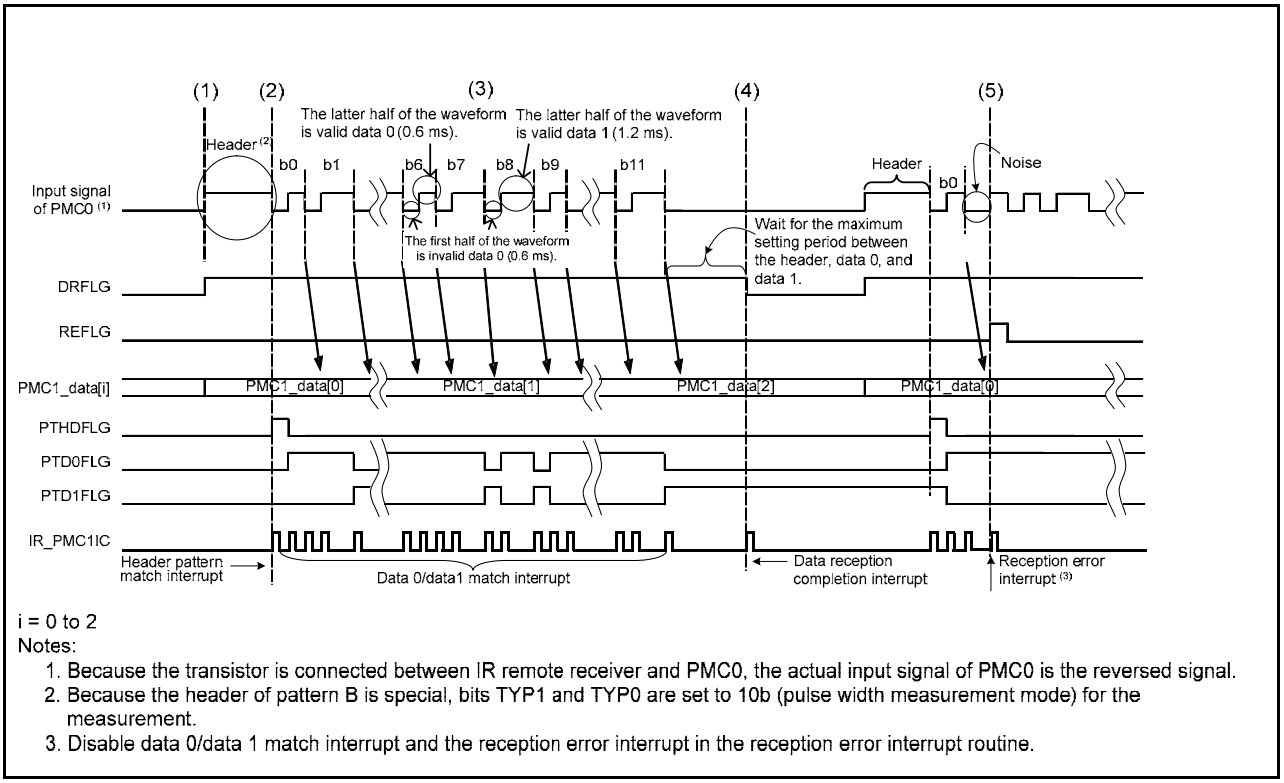
(4) In the data reception completion interrupt, received data is encoded to bit 0 or bit 1 according to the low width and high width of each bit.

(5) When a signal is affected by noise and causes an error, to prevent further data from being received, the data 0/data1 match interrupt and reception error interrupts are disabled in the error interrupt processing.

Note:

1. As there is no PMC1 receive data store register i (PMC1DATi), the user must self-define it.

Figure 5.2 shows the status operation and interrupt generation timing when the PMC1 circuit remote control signal during reception.



i = 0 to 2

Notes:

1. Because the transistor is connected between IR remote receiver and PMC0, the actual input signal of PMC0 is the reversed signal.
2. Because the header of pattern B is special, bits TYP1 and TYP0 are set to 10b (pulse width measurement mode) for the measurement.
3. Disable data 0/data 1 match interrupt and the reception error interrupt in the reception error interrupt routine.

Figure 5.2 PMC1 Reception Timing of the Remote Control with Header and Repeat Code Format

5.2 Required Memory Size

Table 5.3 lists the required memory size.

Table 5.3 Required Memory Size

Memory Used	Size	Remarks
ROM	1528 Bytes	
RAM	1543 Bytes	
Maximum user stack	23 Bytes	
Maximum interrupt stack	23 Bytes	

The required memory size varies depending on the C compiler version and compiler options.

5.3 Invariable Table

Table 5.4 lists the invariables used in the sample code.

Table 5.4 Invariables Used in the Sample Code

Invariable Name	Setting Value	Description
DISABLE	0	Disable
ENABLE	1	Enable
PMC0_HEAD_MIN	397	PMC0 header pattern set (MIN)
PMC0_HEAD_MAX	486	PMC0 header pattern set (MAX)
MEASURE_VALUE_MAX	0x0F2C	Maximum value of the pattern A special data (repeat) (MAX)
MEASURE_VALUE_MIN	0x0C6A	Minimum value of the pattern A special data (repeat) (MIN)
PMC0_DATA0_MIN	31	PMC0 data 0 pattern set (MIN)
PMC0_DATA0_MAX	39	PMC0 data 0 pattern set (MAX)
PMC0_DATA1_MIN	67	PMC0 data 1 pattern set (MIN)
PMC0_DATA1_MAX	82	PMC0 data 1 pattern set (MAX)
PMC1_HEAD_MIN	70	PMC1 header pattern set (MIN)
PMC1_HEAD_MAX	86	PMC1 header pattern set (MAX)
PMC1_DATA0_MIN	17	PMC1 data 0 pattern set (MIN)
PMC1_DATA0_MAX	21	PMC1 data 0 pattern set (MAX)
PMC1_DATA1_MIN	34	PMC1 data 0 pattern set (MIN)
PMC1_DATA1_MAX	42	PMC1 data 0 pattern set (MAX)
EN_PMC	0x01	Enable PMCi (i = 0, 1)
COUNT_TB2	0x5000	Timer B2 counts 0x5000
TB2S_EN	0x80	Enable timer B2 count
f64TIMAB	0x03	Count source of timer B2

5.4 Variable Table

Table 5.5 lists the global variables.

Table 5.5 Global Variables

Type	Variable Name	Contents	Function Used
int	odd_even_bit	Count the number of bit received from the PMC1 circuit. Use the count value to determine if the number of received bits is even or odd.	_remote_control_1
char	PMC1_data[2]	Store the received data using the PMC1 circuit.	_remote_control_1
int	bits	Offset value to store received data in PMC1_data[].	_remote_control_1
_Bool	PMC1_ERFLG	PMC1 error flag 0: No error 1: Error	_remote_control_1

5.5 Function Table

Table 5.6 lists the functions.

Table 5.6 Functions

Function Name	Description
Clock_Init	Initialize the clock
PMC_Init	Initialize PMC1 and PMC0
TB2_Init	Initialize timer B2
_remote_control_0	Interrupt function of PMC0
_remote_control_1	Interrupt function of PMC1
_timer_b2	Interrupt function of timer B2

5.6 Function Specifications

The following tables list the sample code function specifications.

Clock_Init	
Outline	Clock initialization function
Header	None
Declaration	void Clock_Init(void)
Description	Initialize the CPU clock and sub clock.
Argument	None
Returned value	None

PMC_Init	
Outline	Remote control initialization function
Header	None
Declaration	void PMC_Init(void)
Description	Initialize the PMC0 and PMC1 circuits.
Argument	None
Returned value	None

TB2_Init	
Outline	Timer B2 initialization function
Header	Nnone
Declaration	void TB2_Init(void)
Description	Initialize timer B2.
Argument	None
Returned value	None

_remote_control_0	
Outline	PMC0 interrupt function
Header	None
Declaration	void _remote_control_0(void)
Description	Receive the header and data of pattern A format.
Argument	None
Returned value	None

_timer_b2	
Outline	Timer B2 interrupt function
Header	None
Declaration	void _timer_b2(void)
Description	Receive the repeat code of pattern A format.
Argument	None
Returned value	None

_remote_control_1	
Outline	PMC1 interrupt function
Header	None
Declaration	void _remote_control_1(void)
Description	Receive the header and data of pattern B format.
Argument	None
Returned value	None

5.7 Flowchart

5.7.1 Main Processing

Figure 5.3 shows the main processing.

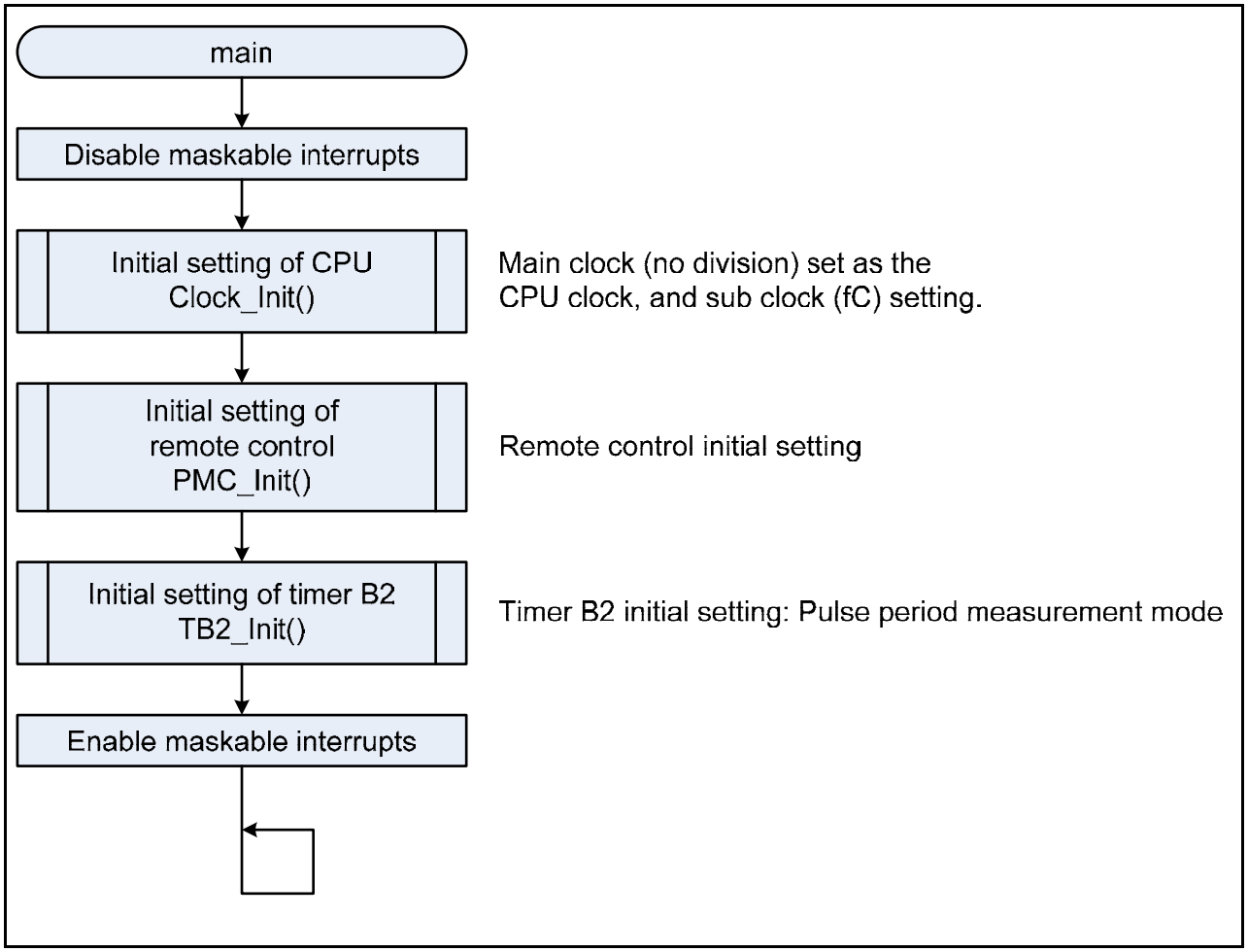


Figure 5.3 Main Processing

5.7.2 MCU Initialization Processing

Figure 5.4 shows the MCU initialization processing.

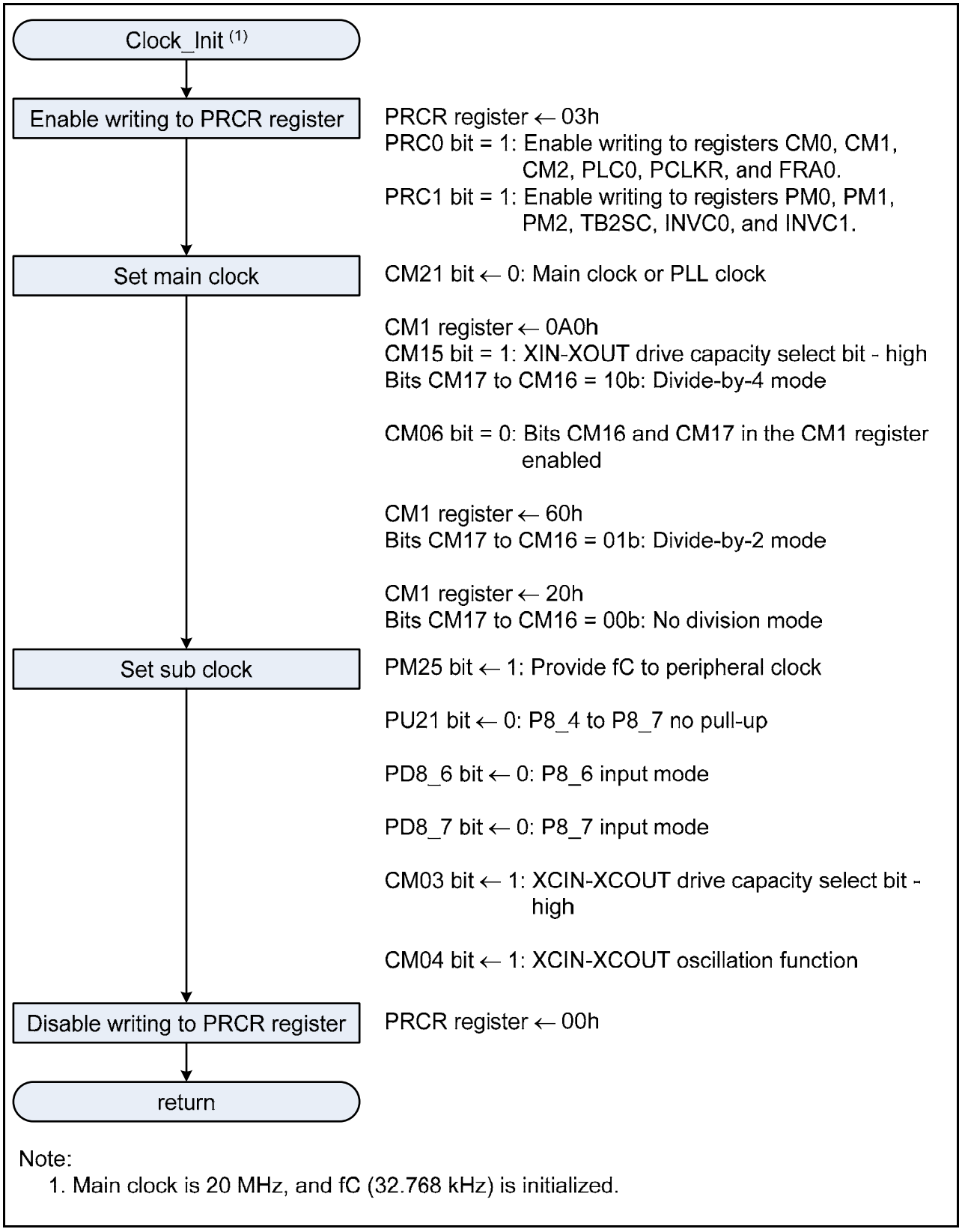


Figure 5.4 MCU Initialization Processing

5.7.3 PMCi and Timer B2 Initialization Processing

Figure 5.5 to Figure 5.7 show the PMCi and timer B2 initialization processing.

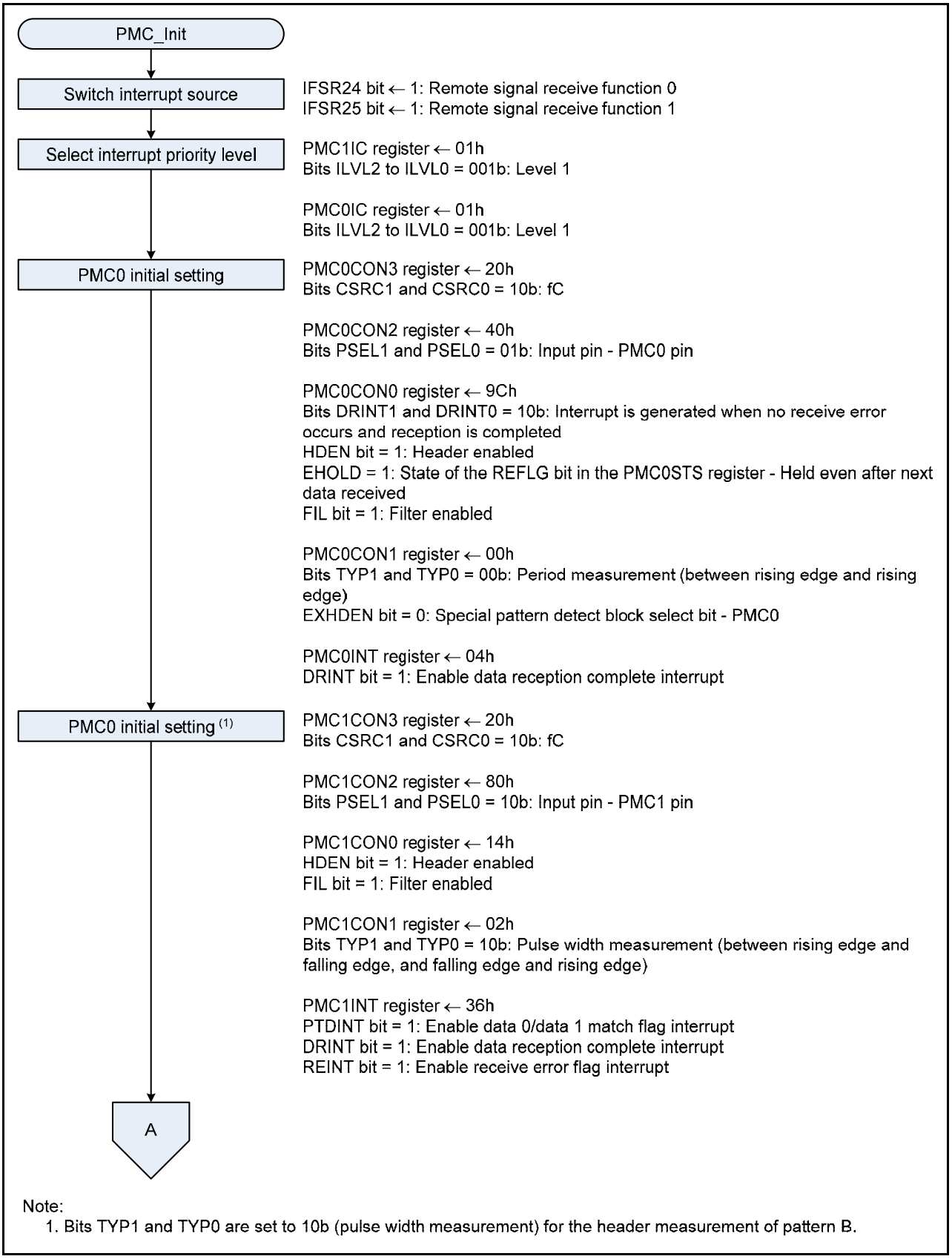
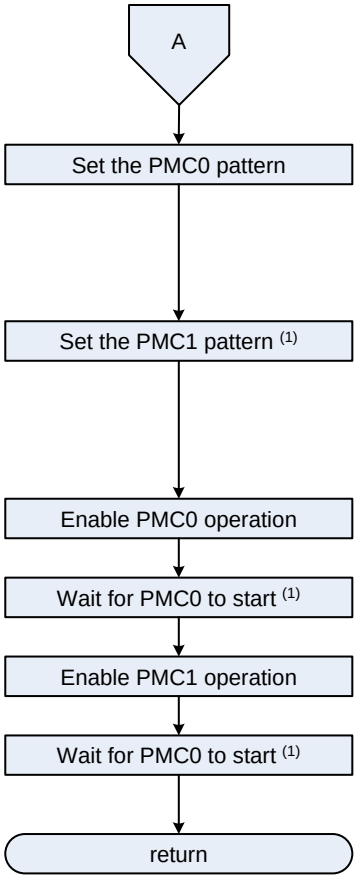


Figure 5.5 PMCi Initialization Processing (1/2)



PMC0HDPMIN register ← 397 : (9.0 + 4.5)[ms] × (1 - 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 397
PMC0HDPMAX register ← 486 : (9.0 + 4.5)[ms] × (1 + 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 486
PMC0D0PMIN register ← 31 : 1.1[ms] × (1 - 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 31
PMC0D0PMAX register ← 39 : 1.1[ms] × (1 + 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 39
PMC0D1PMIN register ← 67 : 2.3[ms] × (1 - 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 67
PMC0D1PMAX register ← 82 : 2.3[ms] × (1 + 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 82

PMC1HDPMIN register ← 70 : 2.4[ms] × (1 - 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 70
PMC1HDPMAX register ← 86 : 2.4[ms] × (1 + 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 86
PMC1D0PMIN register ← 17 : 0.6[ms] × (1 - 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 17
PMC1D0PMAX register ← 21 : 0.6[ms] × (1 + 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 21
PMC1D1PMIN register ← 34 : 1.2[ms] × (1 - 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 34
PMC1D1PMAX register ← 42 : 1.2[ms] × (1 + 0.1) ÷ (1 ÷ 32.768 [kHz]) - 1 = 42

EN bit ← 1: Enable PMC0 operation

Read PMC0CON2 register
ENFLG bit = 0: PMC0 stops
= 1: PMC0 operating

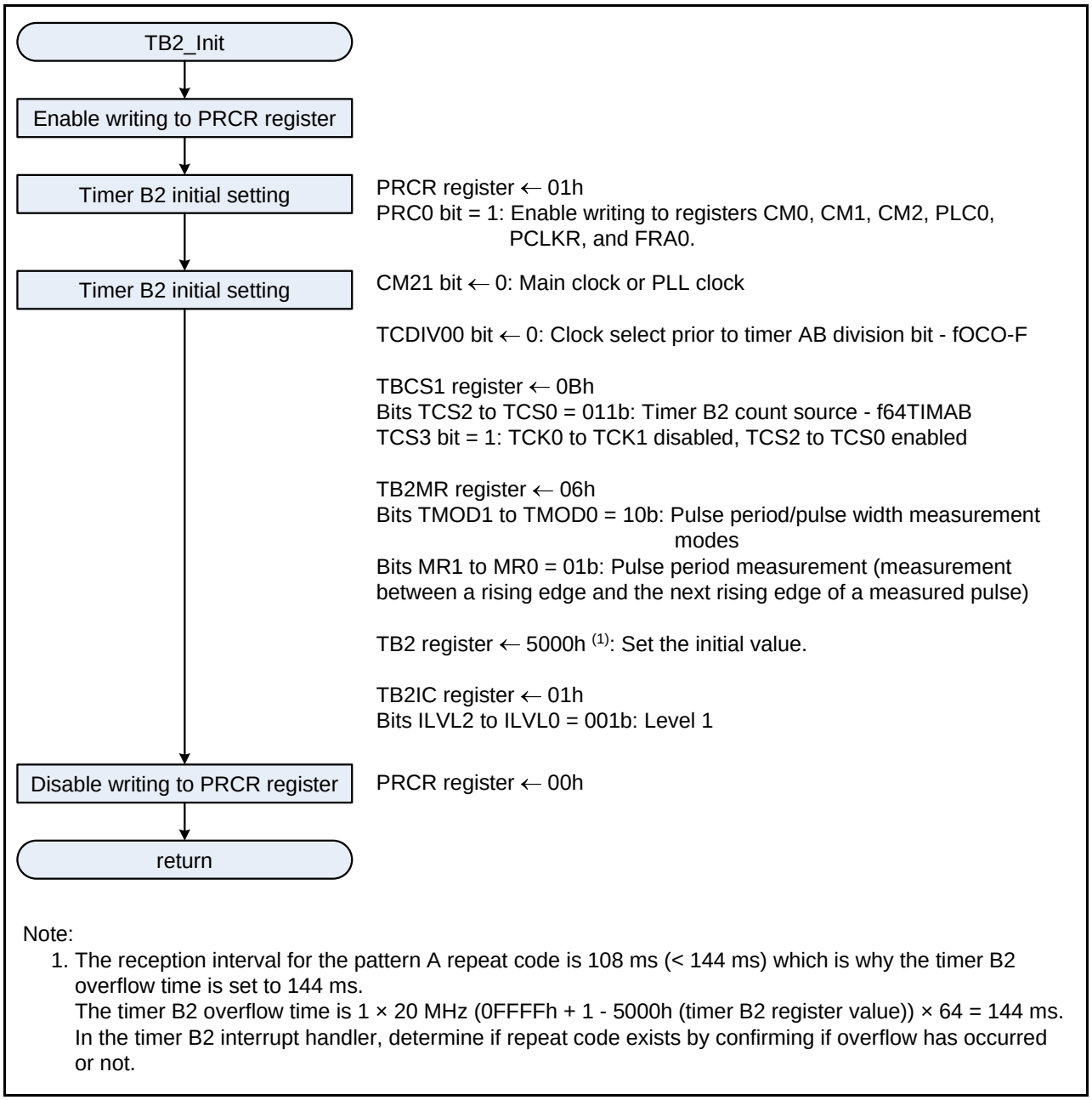
EN bit ← 1: Enable PMC1 operation

Read PMC1CON2 register
ENFLG bit = 0: PMC1 stops
= 1: PMC1 operating

i = 0, 1

Notes:
1. Pattern B takes two measurements (high width and low width) of a single waveform. The low width (an odd number of times) is determined as data 0 pattern (0.6 ms) or data 1 pattern (1.2 ms), and the data is encoded.
2. The PMCi circuit starts operating by setting the EN bit to 1 (operation enabled) and the ENFLG bit becomes 1 (operating). After setting the EN bit to 1, it takes up to two cycles of the count source before the ENFLG bit becomes 1. During this period, do not access bits or registers associated with the PMCi except for the ENFLG bit.

Figure 5.6 PMCi Initialization Processing (2/2)



Note:
1. The reception interval for the pattern A repeat code is 108 ms (< 144 ms) which is why the timer B2 overflow time is set to 144 ms.
   The timer B2 overflow time is 1 × 20 MHz (0FFFFh + 1 - 5000h (timer B2 register value)) × 64 = 144 ms.
   In the timer B2 interrupt handler, determine if repeat code exists by confirming if overflow has occurred or not.

Figure 5.7 Timer B2 Initialization Processing

5.7.4 PMC0 and Timer B2 Interrupt Handling

Figure 5.8 and Figure 5.9 show the interrupt handling of PMC0 and Timer B2, respectively.

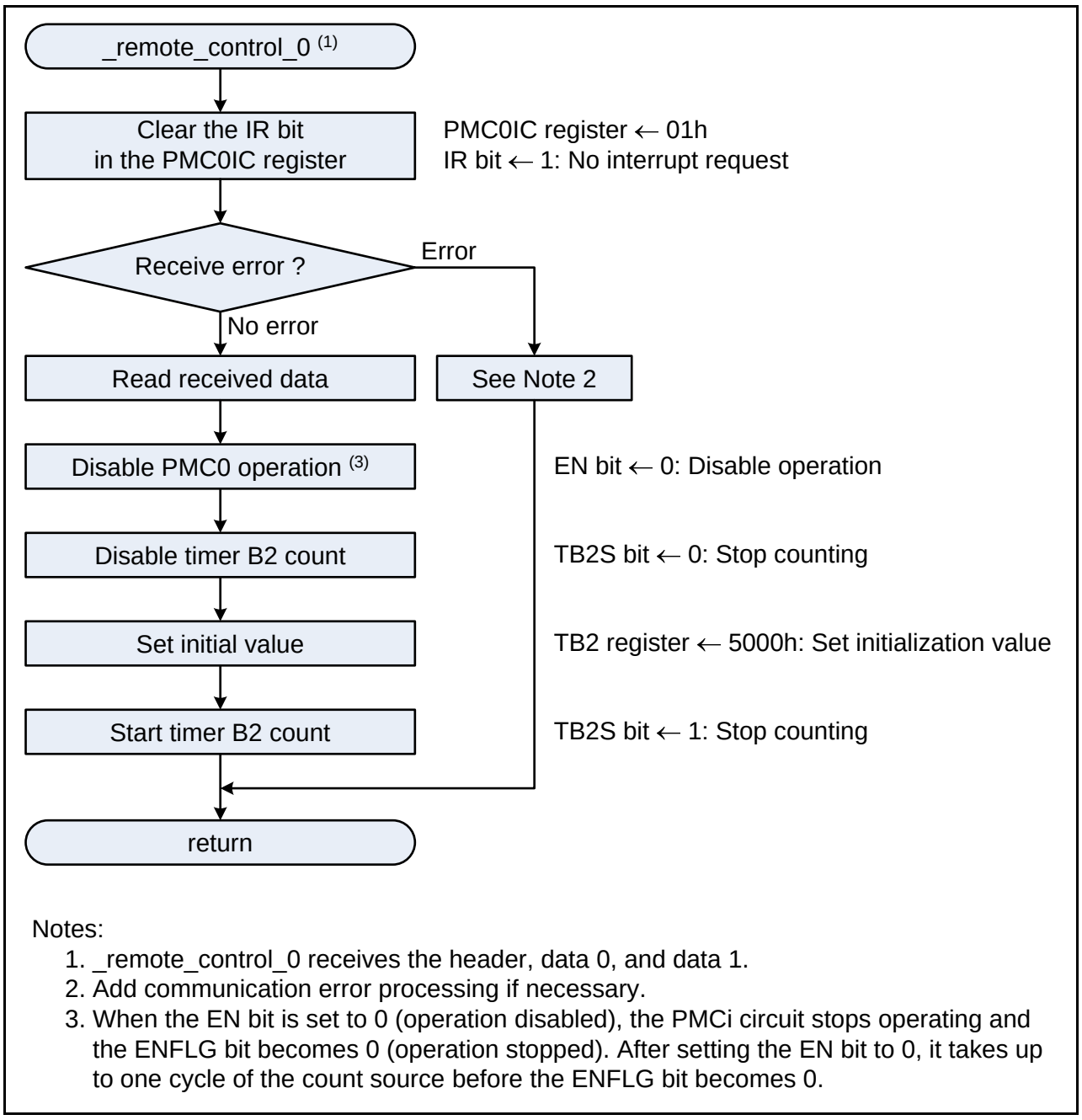
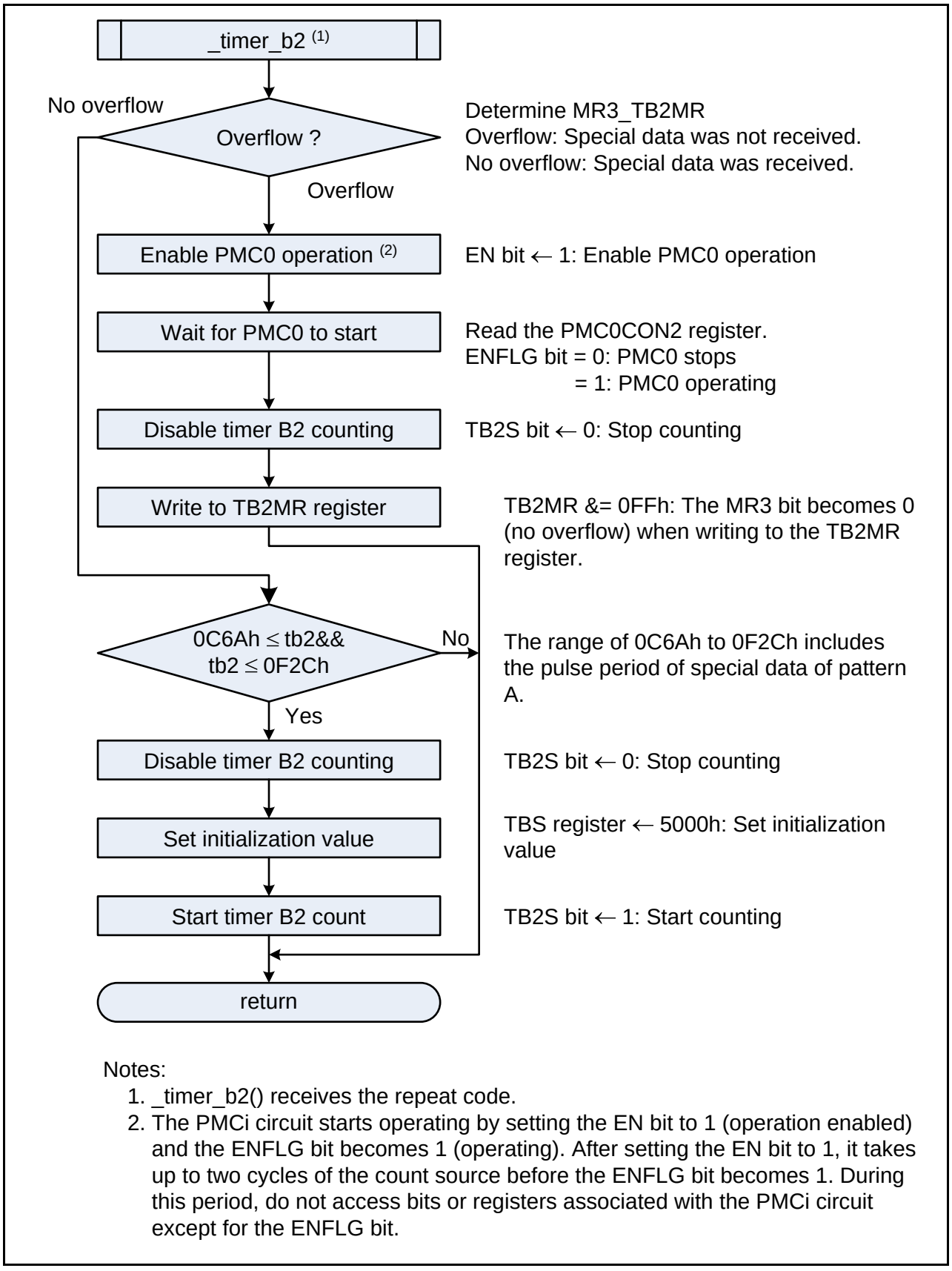


Figure 5.8 PMC0 Interrupt Handling



Notes:
1. _timer_b2() receives the repeat code.
2. The PMCi circuit starts operating by setting the EN bit to 1 (operation enabled) and the ENFLG bit becomes 1 (operating). After setting the EN bit to 1, it takes up to two cycles of the count source before the ENFLG bit becomes 1. During this period, do not access bits or registers associated with the PMCi circuit except for the ENFLG bit.

Figure 5.9 Timer B2 Interrupt Handling

5.7.5 PMC1 Interrupt Handling

Figure 5.10 shows the interrupt handling of PMC1.

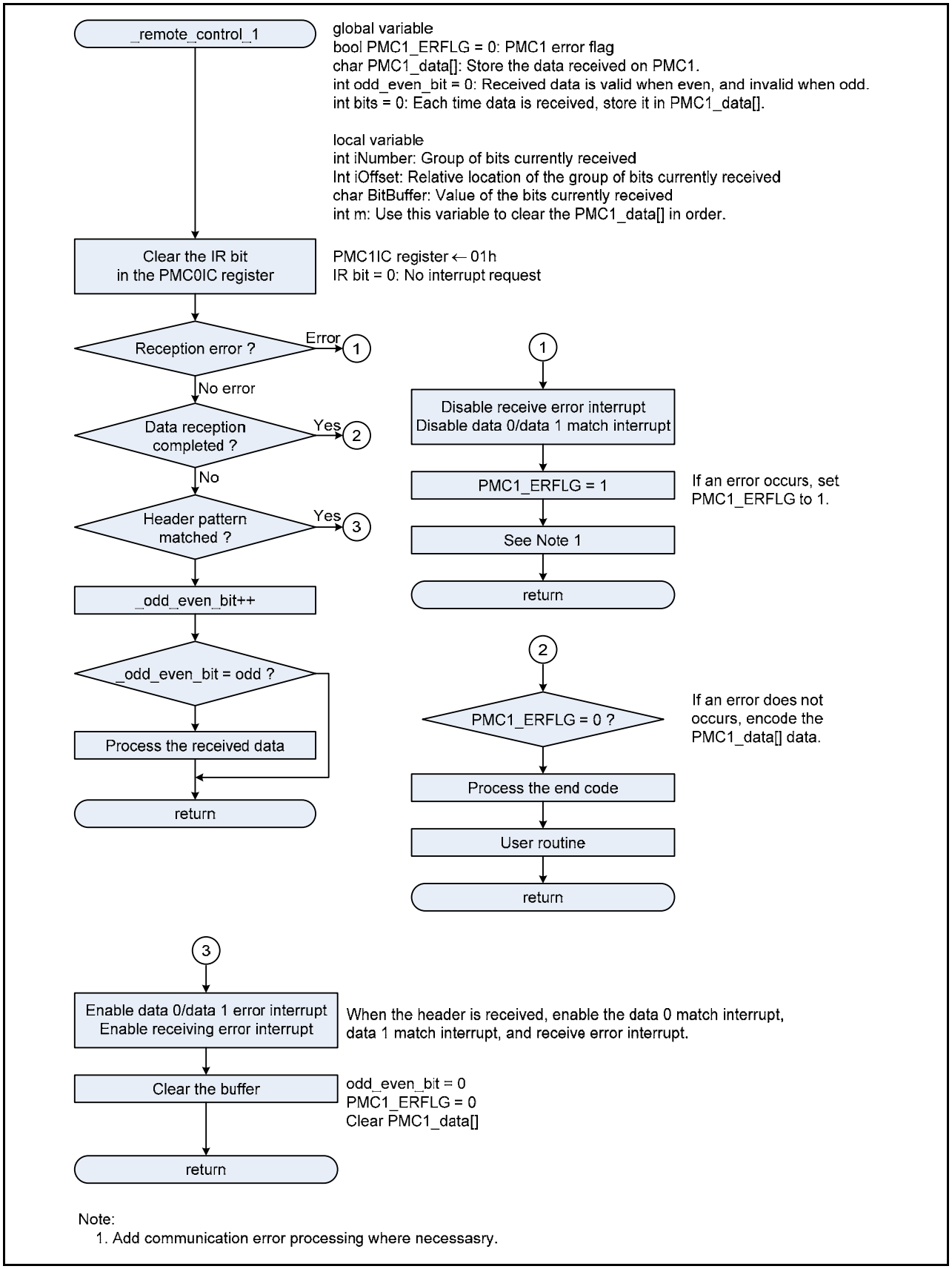


Figure 5.10 PMC1 Interrupt Handling

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.1.00
M16C/64A Group User's Manual: Hardware Rev.1.10
M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65 Group User's Manual: Hardware Rev.1.10
M16C/65C Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series and R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.3.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
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Revision History	M16C/63, M16C/64A, M16C/64C, M16C/65, M16C/65C Groups Remote Control Signal Receiver of 2 format Types

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 31, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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