M16C/63, 64, 64A, 64C, 65, 65C, 6C, 5L, 56, 5LD, 56D, 5M, and 57 Groups

Tolerance of Data Transfer Rate in Clock Asynchronous Serial I/O Mode

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Abstract

This document describes tolerance of data transfer rate in clock asynchronous serial I/O mode for the M16C/63, 64, 64A, 64C, 65, 65C, 6C, 5L, 56, 5LD, 56D, 5M, and 57 Groups. "i" in UARTi refers to a channel number. The number of channels varies according to the MCU used. Refer to the User’s Manual: Hardware for details.

Products

M16C/63, 64, 64A, 64C, 65, 65C, 6C, 5L, 56, 5LD, 56D, 5M, and 57 Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

1.1 Data Format

This section describes the data format in clock asynchronous serial I/O mode. Table 1.1 lists the Transmit/Receive Data Types and Their Functions. Figure 1.1 shows the Data Format Pattern.

Table 1.1 Transmit/Receive Data Types and Their Functions

Transmit/Receive Data Type	Function	Remarks
ST (start bit)	Low signal which is 1 bit of the character bit, and added immediately before the character bit. This bit indicates the start of data.	1 bit
DATA (character bit)	Transmit data set in the UARTi transmit buffer register.	Selectable from 7 bits, 8 bits, and 9 bits
P (parity bit)	A signal added immediately after the character bit to improve reliability of data. The signal level is changed according to whether the selection for the parity is even or odd. The total number of 1's for this bit and the character bit always becomes even or odd according to even or odd parity.	Selectable from odd, even, and none
SP (stop bit)	High signal which is 1 bit or 2 bits of the character bit, and added immediately after the character bit (parity bit when the parity is enabled). This bit indicates that data transfer is complete.	Selectable from 1 bit and 2 bits.

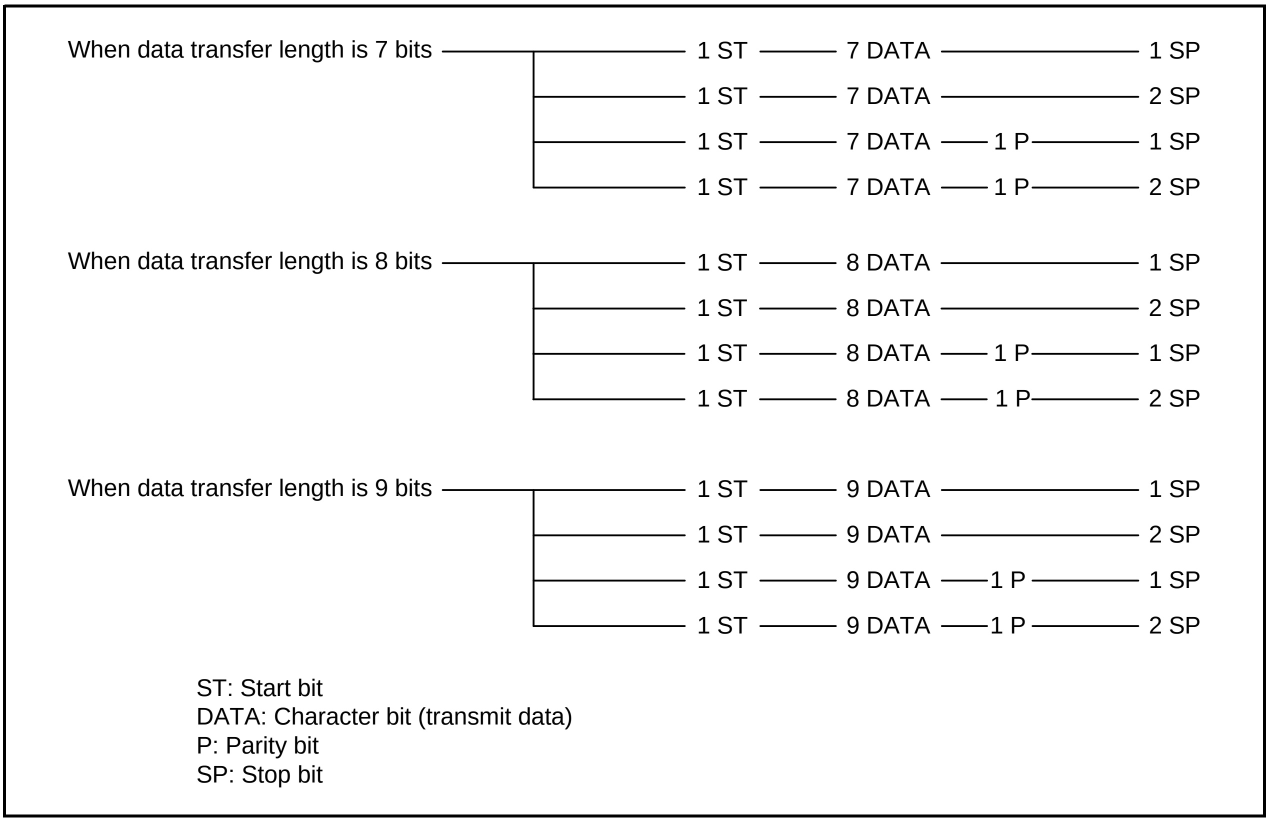


Figure 1.1 Data Format Pattern

1.2 Relation between Receiver Clock and Received Data

During reception, received data that is input to the RXDi pin is obtained at the rising edge of the receiver clock. Therefore, to receive data correctly, the stop bit must be input at the last rising edge of the receiver clock for 1 frame of data (i.e. the data from the start bit to the stop bit).
Figure 1.2 shows the Relation between Receiver Clock and Received Data.

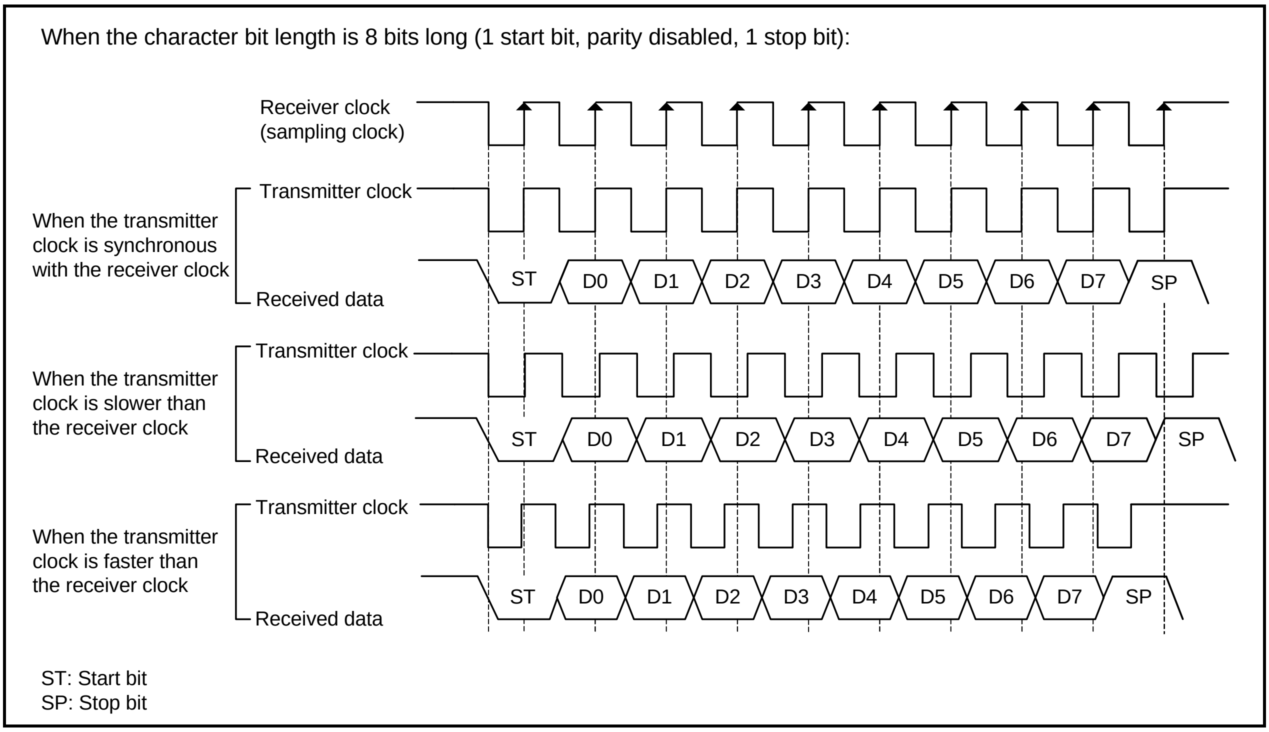


Figure 1.2 Relation between Receiver Clock and Received Data

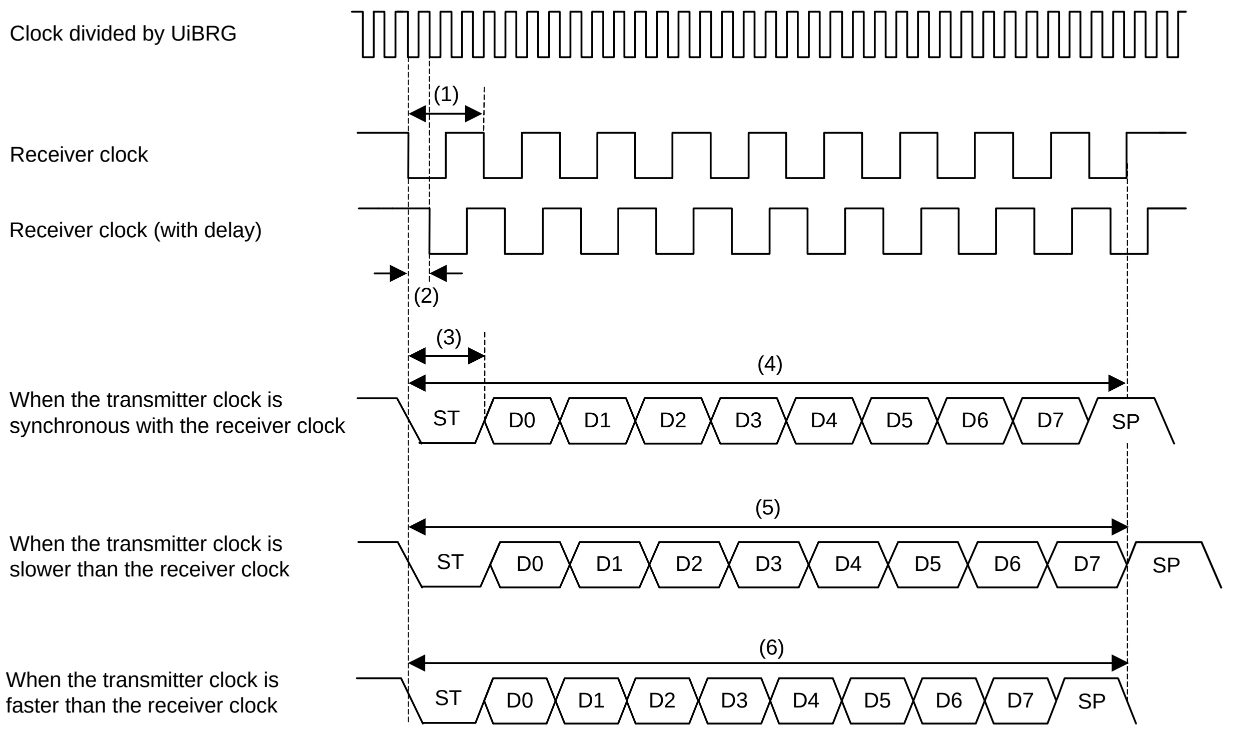
1.3 Calculating Tolerance of Data Transfer Rate

To transmit and receive data correctly, data transfer rates of the transmitter and receiver must meet the relational expression below. Make sure the relational expression is satisfied, and the value is set with an adequate margin. Perform careful evaluation with the user application.

$$\left(\frac{1}{Bt} \times (b - 1) + \frac{(UiBRG + 1)}{F}\right) < \left(\frac{1}{Br} \times (b - 0.5) + \frac{(UiBRG + 1)}{F}\right) < \left(\frac{1}{Bt} \times b\right)$$

Bt: Data transfer rate of the transmitter in bps
Br: Data transfer rate of the receiver in bps
F: Frequency of the UiBRG count source in the receiver in Hz
b: Total number of bits in 1 frame of data (however, subtract 1 from the value when using 2 stop bits)
UiBRG: UiBRG register setting value

Figure 1.3 shows the Relations between Formulas and Operations.



(1)	$\frac{1}{Br}$	Transfer time per bit when receiving
(2)	$\frac{(UiBRG + 1)}{F}$	Delay time from the start bit being detected until the receiver clock starts (a maximum of one clock cycle divided by UiBRG)
(3)	$\frac{1}{Bt}$	Transfer time per bit when transmitting
(4)	b - 0.5	
(5)	b - 1	
(6)	b	

Bt: Data transfer rate of the transmitter in bps
Br: Data transfer rate of the receiver in bps
F: Frequency of the UiBRG count source in the receiver in Hz
b: Total number of bits in 1 frame of data (however, subtract 1 from the value when using 2 stop bits)
UiBRG: UiBRG register setting value

Figure 1.3 Relations between Formulas and Operations

1.3.1 Calculating the Receiver Clock Tolerance

This section describes an example of calculating the tolerance of data transfer rate for the receiver clock with the following conditions: 1 frame of data consists of the start bit, an 8-bit character length, and the stop bit, and the data transfer rate of the transmitter clock is 9600 bps.
Figure 1.4 shows the Calculating the Receiver Clock Tolerance.

Common condition for transmitter and receiver

b: 10 (ST, 8 DATA and SP)

Condition for transmitter

Bt: 9600 bps

Conditions for receiver

F: 16,000,000 Hz
UiBRG: 103

Formula for calculating the receiver clock tolerance

Formula A

$$\left(\frac{1}{Bt}\times(b-1)+\frac{(UiBRG+1)}{F}\right) < \left(\frac{1}{Br}\times(b-0.5)+\frac{(UiBRG+1)}{F}\right) < \left(\frac{1}{Bt}\times b\right)$$

Formula B

Calculating the fastest receivable rate for the receiver clock

Use formula A to calculate the fastest receivable rate for the receiver clock.

$$\left(\frac{1}{Bt}\times(b-1)+\frac{(UiBRG+1)}{F}\right) < \left(\frac{1}{Br}\times(b-0.5)+\frac{(UiBRG+1)}{F}\right)$$

$$\left(\frac{1}{Bt}\times(b-1)\right) < \left(\frac{1}{Br}\times(b-0.5)\right)$$

$$\left(\frac{1}{9600}\times(10-1)\right) < \left(\frac{1}{Br}\times(10-0.5)\right)$$

$$Br < 10133.3 \;\cdots\cdots\; (1)$$

Calculating the slowest receivable rate for the receiver clock

Use formula B to calculate the slowest receivable rate for the receiver clock.

$$\left(\frac{1}{Br}\times(b-0.5)+\frac{(UiBRG+1)}{F}\right) < \left(\frac{1}{Bt}\times b\right)$$

$$\left(\frac{1}{Br}\times(10-0.5)+\frac{(103+1)}{16000000}\right) < \left(\frac{1}{9600}\times b\right)$$

$$9177.2 < Br \;\cdots\cdots\; (2)$$

Calculating receiver clock tolerance

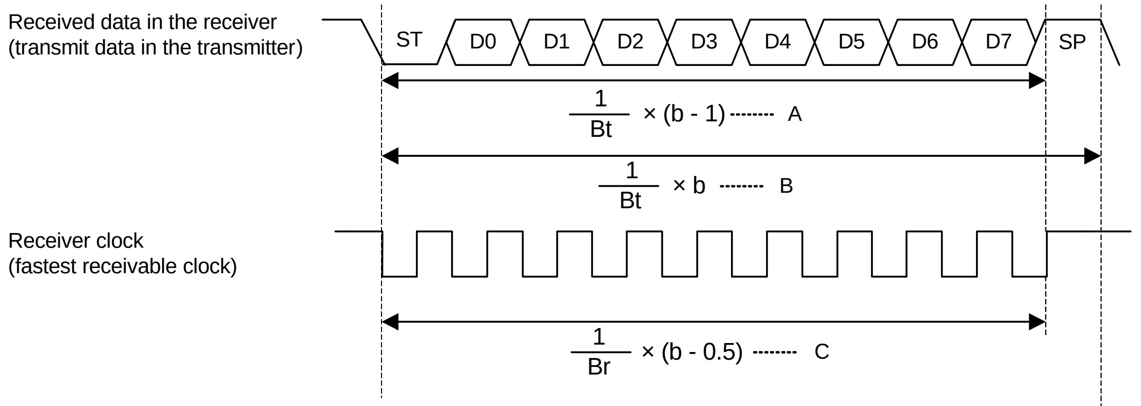
Calculation result from formulas (1) and (2) becomes 9178 < Br < 10133.
Thus, set the transfer rate within 9178 < Br < 10133 (bps) to receive the data correctly.

Figure 1.4 Calculating the Receiver Clock Tolerance

1.3.2 Calculating Tolerance of Data Transfer Rate

This section describes how to calculate tolerance of data transfer rate with or without delay time consideration.

Figure 1.5 shows the Tolerance Without Delay Time Consideration.



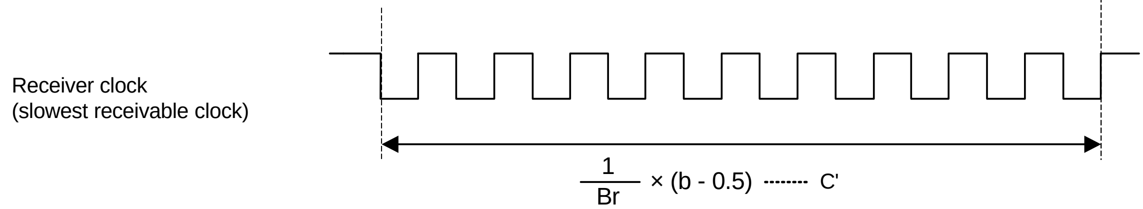
When referencing the transmitter clock, the time required by the fastest receiver clock is time C.
Time C is equal to time A which is 9 (10 - 1) clocks of the transmitter.

A = C

$$\frac{1}{Bt} \times (b - 1) = \frac{1}{Br} \times (b - 0.5)$$

Data can be received when the receiver clock is slower than the transmitter clock. Thus the relational expression becomes as follows:

$$\frac{1}{Bt} \times (b - 1) < \frac{1}{Br} \times (b - 0.5) \quad \text{-------- (1)}$$



When referencing the transmitter clock, the time required by the slowest receiver clock is time C'.
Time C' is equal to time B which is 10 clocks of the transmitter.

B = C'

$$\frac{1}{Bt} \times b = \frac{1}{Br} \times (b - 0.5)$$

Data can be received when the receiver clock is faster than the transmitter clock. Thus the relational expression becomes as follows:

$$\frac{1}{Br} \times (b - 0.5) < \frac{1}{Bt} \times b \quad \text{-------- (2)}$$

Without considering delay time, data can be received when the receiver clock is between the slowest clock (1) and the fastest clock (2). The relational expression becomes as follows:

$$\frac{1}{Bt} \times (b - 1) < \frac{1}{Br} \times (b - 0.5) < \frac{1}{Bt} \times b$$

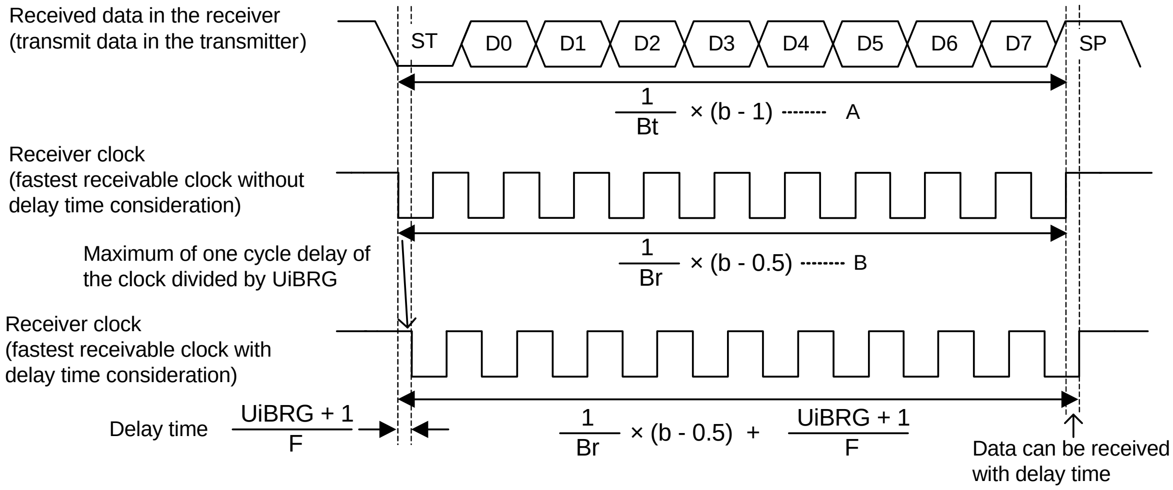
When the receiver clock operates at the highest speed

When the receiver clock operates at the lowest speed

Figure 1.5 Tolerance Without Delay Time Consideration

Although the tolerance without considering delay time is shown in Figure 1.5, actually there is a delay of up to one cycle of the clock divided by UiBRG. Therefore, the transfer rate must be set while taking delay time into consideration.

Figure 1.6 shows the Fastest Receiver Clock with Delay Time Consideration, and Figure 1.7 shows Slowest Receiver Clock with Delay Time Consideration.



When using B, the fastest receiver clock without delay time consideration, data can be received correctly even with delay time. Thus B is the highest transfer rate.
The time B is equal to time A which is 9 (10 - 1) clocks of the transmitter, and is the same as the case for the time without delay time consideration.

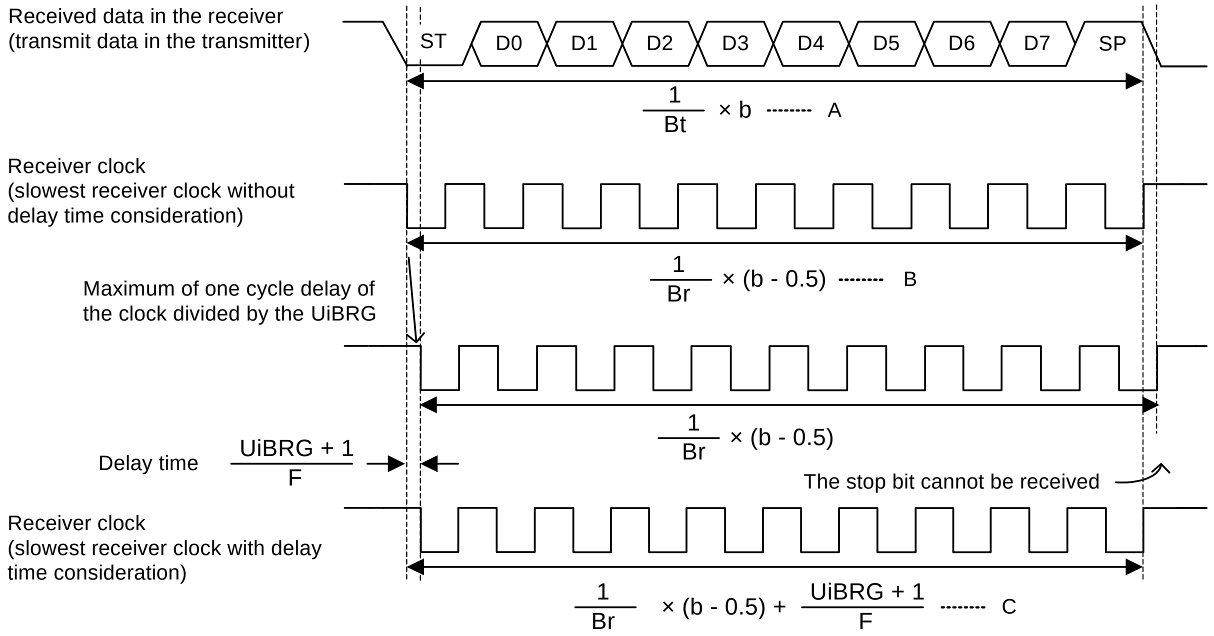
A = B

$$\frac{1}{Bt} \times (b - 1) = \frac{1}{Br} \times (b - 0.5)$$

The receiver clock should be slower than the case above. Thus the relational expression becomes as follows:

$$\frac{1}{Bt} \times (b - 1) < \frac{1}{Br} \times (b - 0.5) \quad \text{-------- (1)}$$

Figure 1.6 Fastest Receiver Clock with Delay Time Consideration



The receiver cannot receive data correctly with delay time when using B which is the slowest receivable clock without delay time consideration. Thus the delay time needs to be considered for the slowest receiver clock.
The time required by the slowest receiver clock is the time when C, the receiver clock with delay time consideration, is equal to A which is 10 clocks of the transmitter.

A = C

$$\frac{1}{Bt} \times b = \frac{1}{Br} \times (b - 0.5) + \frac{UiBRG + 1}{F}$$

Data can be received when the receiver clock is faster than the transmitter clock. Thus the relational expression becomes as follows:

$$\frac{1}{Br} \times (b - 0.5) + \frac{UiBRG + 1}{F} < \frac{1}{Bt} \times b \quad \cdots\cdots\cdots \text{(2')}$$

Figure 1.7 Slowest Receiver Clock with Delay Time Consideration

With delay time consideration, formula (1) in Figure 1.6 and formula (2') in Figure 1.7 produce the following formulas.

$$\frac{1}{Br} \times (b - 0.5) + \frac{UiBRG + 1}{F} < \frac{1}{Bt} \times b \quad \text{--------} \quad (2')$$

$$\frac{1}{Bt} \times (b - 1) < \frac{1}{Br} \times (b - 0.5) \quad \text{--------} \quad (1)$$

To merge formulas (2') and (1), add $\frac{UiBRG + 1}{F}$ to both sides of formula (1).

$$\frac{1}{Bt} \times (b - 1) + \frac{UiBRG + 1}{F} < \frac{1}{Br} \times (b - 0.5) + \frac{UiBRG + 1}{F} \quad \text{--------} \quad (1')$$

From formulas (2') and (1'):

$$\frac{1}{Bt} \times (b - 1) + \frac{UiBRG + 1}{F} < \frac{1}{Br} \times (b - 0.5) + \frac{UiBRG + 1}{F} < \frac{1}{Bt} \times b$$

When the receiver clock operates at the highest speed

When the receiver clock operates at the lowest speed

When the above formula is satisfied, data can be received correctly.

Figure 1.8 Formulas for Tolerance of Data Transfer Rate

2. Reference Documents

M16C/63 Group User's Manual: Hardware Rev. 2.00
M16C/64 Group Hardware Manual Rev. 1.05
M16C/64A Group User's Manual: Hardware Rev. 2.00
M16C/64C Group User's Manual: Hardware Rev. 1.00
M16C/65 Group User's Manual: Hardware Rev. 2.00
M16C/65C Group User's Manual: Hardware Rev. 1.00
M16C/6C Group User's Manual: Hardware Rev. 2.00
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev. 1.10
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev. 1.10
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev. 1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series/R8C Series C Compiler Package V.5.45
C Compiler User's Manual Rev. 2.00
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Revision History	M16C/63, 64, 64A, 64C, 65, 65C, 6C, 5L, 56, 5LD, 56D, 5M, and 57 Groups Tolerance of Data Transfer Rate in Clock Asynchronous Serial I/O Mode

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 30, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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